ACT5 EIT system: a multiple-source electrical impedance tomography system

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ACT5 EIT SYSTEM:
A MULTIPLE-SOURCE ELECTRICAL IMPEDANCE TOMOGRAPHY SYSTEM

by

Omid Rajabi Shishvan

A Dissertation
Submitted to the University at Albany, State University of New York
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ABSTRACT

This dissertation describes the design and implementation of Adaptive Current Tomograph 5 (ACT5) with a focus on the digital processing and data flow in the instrument. ACT5 is an electrical impedance tomography (EIT) instrument that produces images of the complex impedivity distribution within the body by injecting currents through and measuring voltages on electrodes applied to the skin. ACT5 is a parallel-drive EIT system with a dedicated current source for each electrode, capable of driving all electrodes simultaneously and measuring the induced voltages on them. It can support up to 48 electrodes with a frequency range of 5 kHz to 1 MHz with fully programmable current drive patterns. ACT5 can acquire data at a frame rate of $\approx 30$ frames per second when using 32 electrodes. For each electrode channel, a dedicated field-programmable gate array (FPGA) generates a sinusoidal burst with the help of a digital-to-analog converter (DAC) and a Howland current pump, and measures the phase and the amplitude of the induced voltage by using an analog-to-digital converter (DAC) and a matched filter. The low-level setup and synchronization of the channels is done by a controller that manages the flow of information in the system and controls the execution timings of operation. The high-level control of the system is in the hands of an operator through a graphical user interface (GUI) on a PC that communicates with the controller via a serial communication link. The last major hardware component of ACT5 is the calibration unit that is responsible for calibrating the channels so that the injected currents and the measured voltages on one channel are accurate and in agreement with the rest of the channels.

ACT5 incorporates multiple novel design ideas compared to other EIT systems. Analog circuits and processing are minimized in ACT5, and the functions are moved to the digital domain. ACT5 also can calibrate itself while it is attached to patients, making it suitable for long-term monitoring of patients. Simultaneous monitoring of heart activity through measuring and recording electrocardiogram (ECG) signals is another feature of ACT5. Lastly, one of the major benefits of ACT5 is its ability to apply optimal current patterns to provide the maximum amount of information for an arbitrary shape and distribution. This dissertation provides an overview of fundamentals of EIT systems with an extensive literature review. It
then discusses various aspects of the design of ACT5, such as the hardware, communication links, modes of operation, calibration process, and safety features in detail. Additionally, a wide variety of experimental results including image reconstructions of objects in a saline tank, three-dimensional image reconstructions of the thorax region of human subjects, ECG recordings from human subjects are presented. Additionally, the ability of ACT5 to detect small changes in the impedance network seen by the electrodes and the ability to apply optimal current patterns are presented to show the performance of ACT5.
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CHAPTER 1

Introduction

This chapter introduces the subject of the thesis and its motivation, and overviews the rest of the chapters in the thesis.

1.1 Electrical Impedance Tomography

Electrical Impedance Tomography (EIT) is a relatively new imaging technique that is used to create images of the impedance distribution of inner structures of objects from measurements made on its surface. EIT, and its variants such as Electrical Resistivity Tomography (ERT), Electrical Capacitance Tomography (ECT), and Electrical Impedance Tomography Spectroscopy (EITS), are used in wide range of applications. These techniques have been used in geophysical applications such as mapping subsurface structures [1] or imaging buried landmines [2], and in industrial applications such as imaging flow of gas and fluids in a pipe [3], detecting damages to concrete [4], or monitoring crystallization in liquid solutions [5]. It has also been used in medical applications such as imaging cancer in the breast [6, 7] or prostate [8], hand gesture recognition for human-computer interfaces [9], monitoring brain function [10, 11], and monitoring lung function [12].

For medical applications, EIT utilizes a number of electrodes (usually 8, 16, or 32 electrodes) mounted on the surface of the body around the region of interest (thorax, brain, wrist, etc.) and injects electrical current through the electrodes into the body and measures the induced voltages on the electrodes [13]. Similarly, EIT systems can apply a voltage on the electrodes and measure the current passing through them [14, 15]. In both of these cases, by taking the voltages on the electrodes and the current passing through them and knowledge of the geometry of electrode positions, the impedance distributions of the inner structure of the body can be determined through solving a mathematical inverse problem [16].

EIT has multiple advantages and disadvantages compared to other imaging techniques such as Computed Tomography (CT) and Magnetic Resonance Imaging (MRI). One of the main advantages of EIT is that it is a radiation-free tomography technology with no side
effects, hazards, or pain to the subjects. EIT is also non-invasive and portable, meaning that it can be used directly at the bedside. Another advantage of EIT is that it is relatively less expensive compared to some other medical imaging tools, with the cost of an EIT instrument being in the range of tens of thousands of dollars. One of the main advantages of EIT is its high temporal resolution where it can collect and plot images at a high frame rate compared to other imaging systems.

On the other hand, the main disadvantage of EIT is its low spatial resolution which stems from the fact that, for a system with $N$ electrodes, there are only $O(N^2)$ degrees of freedom that can be used to reconstruct images. Another disadvantage of EIT systems is that the inverse problem that must be solved to reconstruct the images is severely ill-posed. This means that significant variations of impedance deep inside the body have a minimal effect on the induced voltages on the surface, while small variation of impedance close to the surface of the body can impact the induced voltages significantly. The last drawback of EIT is related to the physical nature of electrodes where applying the electrodes and maintaining their contact to the skin can be a cumbersome task. Also, the electrodes can cause skin irritation for some subjects.

1.2 Thorax Imaging

Monitoring the thorax region of body, specifically the heart and lungs, is an area of great interest in the medical field. Determining the airflow into the lungs can help in applications such as setting mechanical ventilators [17] and determining damage to lung tissue in cystic fibrosis patients [18]. In such applications it is important to measure ventilation–perfusion (V/Q) ratio which indicates the effectiveness of gas exchange in the lungs [19]. To get regional (V/Q), we have to monitor the distribution of air in the lung during respiration and also the regional blood flow in lung tissue. Since air has higher impedance compared to the body tissue and blood has lower impedance than the body tissue, mapping the impedance variation in the thorax is a viable option to monitor both ventilation an perfusion. In addition, monitoring both the air ventilation in the lungs and blood perfusion in the body require a relatively high-speed imaging technique, which is again provided by EIT systems. These factors make EIT a suitable candidate for thorax monitoring and imaging, since it can monitor impedance variation with high temporal resolution, with frame rate of tens of images.
Figure 1.1 shows a diagram of a simplified EIT system with only 4 electrodes. The electrodes are connected around the thorax region and apply current to the body while simultaneously measuring the voltage induced on them. Some features of EIT systems such as the shunt impedance on the sources and the extra ground electrode are also shown on the figure.

1.3 ACT5

This thesis describes a new EIT system called Adaptive Current Tomograph 5 (ACT5). The main motivation behind the development of ACT5 is to be able to construct low-noise EIT images of the thorax region at a high frame rate. ACT5 has current sources and voltimeters that operate with high signal-to-noise ratios which can collect data for images at a frame rate of $\approx 30 \frac{\text{frames}}{\text{sec}}$ when using 32 electrodes. ACT5 uses long cables (1.5 m) that can connect the electronics to electrode arrays on a patient.

ACT5 is designed to be portable where the hardware fits in a 54 cm $\times$ 33 cm $\times$ 23 cm
box as shown in Fig. 1.2. The ACT5 hardware needs only a laptop computer for full functionality, and the small size of the system makes it easy to move from one place to another. The instrument weighs approximately 22.5 kg.

![Figure 1.2: Image of ACT5 hardware with a laptop.](image)

Additionally, the ACT5 hardware does not require any manual or automated analog adjustments. As long as the boards used in the system are physically and electronically sound, they can be plugged in and be ready to use immediately. Moreover, ACT5 has a modular design with a flexible configuration that makes it possible to utilize a varying number of electrodes up to 48 and gather information from objects of different geometries, whether in 2-dimensional (2-D) planes or 3-dimensional (3-D) spaces.

Another novel aspect of ACT5 is that it can calibrate itself whenever necessary, even when it is connected to a load. Being able to recalibrate without disconnecting from a patient is valuable in a long-term monitoring application. ACT5 is also able to simultaneously measure electrocardiogram (ECG) signals at all electrodes, making it possible to time align the EIT images with the cardiac cycle and perform body-surface mapping. Lastly, ACT5 has multiple safety features, which are implemented in its hardware, firmware, and software. These safety features ensure that the subject is not exposed to any possible electrical hazard.
1.4 Dissertation Overview

This document is organized as follows:

Chapter 2 provides an overview on the theoretical aspects of EIT systems, detailing the formulation of the forward and inverse problems. It also describes different possible approaches implementing EIT and delves into the current patterns used in EIT systems. Chapter 3 reviews the background of EIT by studying notable EIT systems, detailing some reasons for various design considerations. It also provides details on ACT5 specifications. The building blocks of ACT5 hardware, including the PC, the controller, the calibration board, the source boards, and the backplane are covered in Chapter 4. Chapter 5 explains the two mode of operation for ACT5, calibration mode and the imaging mode. The calibration process of ACT5 is described in detail in Chapter 6. Chapter 7 addresses the communication protocols and processes between various parts of ACT5. Chapter 8 details the digital design of the FPGAs. Safety features of ACT5 are then described in Chapter 9. Experimental results of ACT5, including results on human subjects, are shown in Chapter 10. Chapter 11 delves into the novel methods for measuring the shunt impedance values of current sources in ACT5. The contributions of this work, list of publications for ACT5, and the future work are shown in Chapter 12. At the end, Chapter 13 provides the concluding remarks.
CHAPTER 2

Electrical Impedance Tomography

This chapter introduces the fundamentals of EIT and the EIT systems, starting with the mathematical formulation of EIT in an ideal situation. It then discusses the different categories of EIT systems, including applied-voltage and applied-current systems, and pair-drive and parallel-drive systems. At the end, current patterns used in a parallel-drive applied-current system are discussed.

2.1 Fundamentals of EIT

Electrical impedance tomography systems apply sinusoidal electrical currents, typically in the kilo-Hertz frequency range to the body and measure the induced voltages on the boundary. Some systems applying current with frequencies as low as 10 Hz and some with frequencies higher than 1 MHz. The induced voltages are related to the applied currents and the complex conductivity distribution within the body. A mathematical formulation relating the voltages to the currents can be made using Maxwell’s equations.

2.1.1 Mathematical Model of EIT

In an ideal case where current density $j$ is applied to a body $B$ through its surface $S$, the induced electric potential $U$ satisfies the following two equations

$$\nabla \cdot \sigma(\vec{p}) \nabla U(\vec{p}) = 0 \quad \text{for } \vec{p} \text{ in } B$$

$$\sigma(\vec{p}) \frac{\partial U(\vec{p})}{\partial v} = j(\vec{p}) \quad \text{for } \vec{p} \text{ on } S$$

(2.1)

where $\sigma$ is the conductivity, $\vec{p}$ is a point inside the body or on its surface, and $v$ is an outward unit vector to the body. Since there are no sources inside the body, a constraint on the current is that the injected current into the body has to sum to zero, i.e.

$$\int_S j(\vec{p}) dS_p = 0.$$  

(2.2)
Considering the equations governing the physics of EIT, the mathematical problem can be considered as two separate parts, the forward problem which aims at finding the induced voltages for a given conductivity map and a given applied current, and the inverse problem which finds the conductivity distribution based on a given applied currents and their resulting induced voltages.

2.1.2 Forward Problem

The goal of the forward problem in EIT is to find the induced voltages on body given the known electrical excitation patterns and known conductivity distribution of the body. The forward problem is often solved numerically through a finite-element model of the body [20, 21].

2.1.3 Inverse Problem

The inverse problem of EIT is to find the conductivity map of the body when the induced voltages for a given set of excitation signals are given. There are numerous different methods for solving this inverse problem that are generally categorized as (i) linear methods, (ii) iterative nonlinear methods, and (iii) direct nonlinear methods [22]. These solutions vary based on factors such as the complexity of the process and the shape of the imaging target.

The ACT5 interface uses NOSER [12] which is a fast linear reconstruction algorithm for 2-D images, and ToDLeR [23, 24] which is similar to NOSER for 3-D images, for real-time demonstration of images. The collected data is also saved so that they can be further analyzed with more sophisticated reconstruction algorithms, such as D-bar [25], if desired.

2.2 EIT System Categories

EIT systems can be categorized according to various criteria. One possible categorization of EIT systems is based on the type of their sources, where they can use either voltage sources or current sources. Another possible criterion for categorizing EIT systems is the number of active sources, where some EIT systems only utilize a single source while some other use multiple sources [26].
2.2.1 Applied-Current EIT vs. Applied-Voltage EIT

EIT systems can either apply currents to electrodes and measure the induced voltages or apply voltages and measure the current passing through the electrodes. The difference between the two systems is reflected in their boundary conditions where, for the applied current EIT systems, boundary conditions are written as Neumann boundary conditions while, in applied voltage EIT systems, boundary conditions are written as Dirichlet boundary conditions. This means that for applied current systems, the reconstruction of an EIT image is done with taking the Neumann-to-Dirichlet map into account, while for an applied voltage system, the Dirichlet-to-Neumann map is considered for image reconstruction. It is shown that when there is inevitable measurement noise in an EIT system, the inverse problem is better-conditioned when the Neumann-to-Dirichlet map is used \[27, 28\]. ACT5 is an applied-current EIT system.

2.2.2 Pair-Drive vs. Parallel-Drive

The number of sources in an EIT system is another factor that is used to categorize them. The majority of the EIT systems are pair-drive systems, also known as single-source systems. These EIT systems use a single source, or dual sources with opposite polarity, to inject current at one electrode and drain it from another, while measuring the voltages on the remaining of the electrodes \[29\]. The electrodes that are used to pass the current can be connected to the source through a multiplexer.

On the other hand, parallel-drive EIT systems, also known as multiple-source EIT systems, assign a dedicated source to each electrode. These systems can inject current into the body simultaneously from all electrodes and measure the induced voltage on them at the same time \[30\]. A specific case of the parallel-drive systems is interleaved-drive EIT systems. In interleaved-drive EIT systems, the current-injecting electrodes are separated from the electrodes that read the surface voltage. This means that although there are multiple electrodes with dedicated sources in the system, these electrodes will only inject current to the body and leave the measurement of surface voltage to other passive electrodes.

Each of these types of EIT systems have their own advantages and disadvantages. Pair-drive systems are usually simpler and less expensive to implement, while parallel-drive systems require more hardware and hence are more complicated and costly. Another advan-
tage of pair-drive systems is that there is no current passing through their inactive electrodes. This eliminates the need to assume an electrode model \[31\] for the voltage measurement, since no current passing through the electrodes means that the electrode contact impedance has negligible effect on the measured voltage. In a parallel-drive system, since there is usually a current passing through the electrodes, an electrode model that takes into account the voltage drop due to the contact impedance between the body and the electrodes is needed. Note that the interleaved-drive systems have solved this issue by separating their source electrodes from their voltmeter electrodes, but this comes at the cost of electrodes taking more space than parallel-drive systems.

One of the advantages of multiple-drive systems is the omission of the multiplexer that is required in pair-drive systems \[32\]. This multiplexer is used to move the source between different electrode pairs, but it also introduces a parasitic shunt impedance to the sources and adds a transition time between the patterns. Another advantage of parallel-drive systems is that they can provide higher distinguishability, meaning that they can image smaller variations in a given excitation level \[33\]. Distinguishability will be discussed later in this chapter. Pair-drive systems also have fewer data points for each frame of image compared to their parallel-drive counterparts. For a pair-drive system with \(N\) electrodes, which applies current to adjacent electrodes and measures differential voltages between other electrode pairs, there are typically \((N-1) \times (N-3)\) data points for image reconstruction, while the parallel-drive systems have \((N-1) \times N\) number of data points. Note that some pair-drive systems have even fewer available data points and some that measure the voltage on the active electrodes and measure the absolute voltage compared to the differential voltages have more data points, equalling parallel-drive systems. Lastly, one of the main benefits of the parallel-drive systems is their ability to get higher current density in regions away from the electrodes and, as a result, higher signal-to-noise ratio (SNR) compared to pair-drive systems. This is extremely beneficial as signals with higher SNR would yield better images with less noise and artifacts.

ACT5 is a parallel-drive EIT system with each electrode having a dedicated current source.
2.3 Current Patterns

To measure the impedance of the body, EIT systems typically apply a sinusoidal current excitation burst through the electrodes. The current applied by an electrode can be written as

\[ I_S(t) = A \cos (2\pi ft + \theta), \]  

(2.3)

where \(I_S\) is the source current, \(t\) is time, \(A\) is the amplitude of the current, \(f\) is the excitation frequency, and \(\theta\) is the phase angle of the applied current. The sinusoidal current provides the opportunity to both measure the amplitude and the phase of the induced voltage on the electrode, giving information on both the real and the imaginary part of the impedance.

In a parallel-drive EIT system with \(N\) electrodes, each electrode applies a current with the same frequency but an independent amplitude and measures the induced voltage. This means that at a given time and for a given frequency of operation, the applied current from the sources can be written as

\[ I_{S_i}(t) = A_i \cos (2\pi ft + \theta_i) \]  

for \(1 < i < N\)  

(2.4)

where \(I_{S_i}\) is the current from the \(i\)th electrode, \(A_i\) is the amplitude of current on \(i\)th electrode, and \(\theta_i\) is the phase angle of the \(i\)th electrodes current.

We can bundle the applied currents together as a vector to create a current pattern which acts as a basis for an \(N\) dimensional space of current patterns. This space can be described by \(N\) linearly independent current patterns

\[ \vec{I} = (I_{S_1}, I_{S_2}, ..., I_{S_N}). \]  

(2.5)

When the current pattern \(\vec{I}\) is applied to the body, it will have a corresponding induced voltage vector \(\vec{V}\)

\[ \vec{V} = (V_{S_1}, V_{S_2}, ..., V_{S_N}). \]  

(2.6)

As described in (2.2), one constraint on the applied current to the body is that they should sum up to zero, which for a system with \(N\) discrete electrodes can be rewritten as
\[ \sum_{i=1}^{N} I_{S_i} = 0. \quad (2.7) \]

This constraint eliminates one dimension of the \( N \) dimensions in the current pattern space, leaving only \( N - 1 \) viable basis patterns that can be used to solve the inverse problem. These patterns can be written in a matrix form as

\[
I = \begin{bmatrix} \vec{I}^1 \\ \vec{I}^2 \\ \vdots \\ \vec{I}^{N-1} \end{bmatrix} = \begin{bmatrix} I^1_{S_1} & I^1_{S_2} & \cdots & I^1_{S_N} \\ I^2_{S_1} & I^2_{S_2} & \cdots & I^2_{S_N} \\ \vdots & \vdots & \ddots & \vdots \\ I^{N-1}_{S_1} & I^{N-1}_{S_2} & \cdots & I^{N-1}_{S_N} \end{bmatrix} \quad (2.8)
\]

where \( \vec{I}^j \) is the \( j \)th current pattern of \( N - 1 \) linearly independent current patterns and \( I^j_{S_i} \) is the current from the \( i \)th source during the application of \( j \)th pattern. Any other pattern \( \vec{I}' \), where the sum of its elements are zero, can be decomposed into the basis composed of these \( N - 1 \) patterns and written as a linear combination of them

\[
\vec{I}' = \sum_{j=1}^{N} \alpha_j \vec{I}^j. \quad (2.9)
\]

Since the voltages and the currents have a linear association and can related to each other through the impedance network of the body \( (Z) \)

\[
\vec{V} = Z \vec{I}, \quad (2.10)
\]

we can write the voltage \( (\vec{V}') \) resulting from \( \vec{I}' \) as

\[
\vec{V}' = Z \vec{I}' = Z \sum_{j=1}^{N} \alpha_j \vec{I}^j = \sum_{j=1}^{N} \alpha_j Z \vec{I}^j = \sum_{j=1}^{N} \alpha_j \vec{V}^j. \quad (2.11)
\]

The voltages resulting from \( \vec{I}' \) can therefore be written as a linear combination of the voltages resulting from the basis current patterns \( (\vec{V}^j) \), and \( \vec{I}' \) does not provide any additional information for the inverse problem. Note that in reality, due to the limited precision used to represent the physical values and the errors in measurements, practical patterns are not
strictly linearly independent. In high-precision systems, such as ACT5, we can assume that
the conversion of the theoretical basis values to digital values will be sufficiently accurate to
have minimal effect on the outcome.

2.3.1 Ground Electrode

One of the challenges in the practical implementation of EIT systems is that it is not
possible to ensure that the sum of the injected currents will be exactly zero. This mismatch
can have numerous causes such as digitization error in injected current, drifting of current
source elements from their calibrated values, and the shunt impedance to ground in the
sources or cables taking a portion of the current that is intended to pass through the body.
To address this issue, a ground electrode (or a virtual ground electrode as shown in Fig. 1.1)
is connected to the body to provide a path to ground for the mismatch of the injected current
to the body. This ground electrode, which is also used as a reference voltage, is also used in
ACT5 for monitoring the system operation and detecting errors that may impact safety.

2.3.2 Current Pattern Selection

Determining the basis for the current pattern is an important task in EIT applications
that should be done by taking various aspects and limitations into account. In theory, the
only limit on the current patterns is that their net sum should be zero and they should be
linearly independent from each other. In practice, one set of applied current patterns can
be more beneficial in various aspects compared to other possible current pattern sets. For
example, in pair-drive EIT systems only two of the current patterns can be active as +1 and
-1 and the rest of the current sources are set to zero creating a discrete space for the current
patterns. In this space, current can be injected from adjacent electrodes or it can be injected
by skipping some number of electrodes. Depending on the application and the subject of
the imaging, these different excitation patterns have shown to have different results for their
eventual reconstructed images where some produce images with higher quality compared to
others [34, 35].

In parallel-drive EIT systems, there are more degrees of freedom on the current patterns
that can be applied. The space for the current patterns is continuous and the current on each
of the electrodes can be adjusted to create the patterns. Hence, the current patterns should
be selected based on a criterion that would provide the maximum benefit in the resulting images. For such criteria, distinguishability factors are used [36].

2.3.2.1 Distinguishability

Given two different conductivities in a body, $\sigma_0$ and $\sigma_1$, we should have metrics that measure the ability of a given current pattern to distinguish the two conductivities from each other. One of the main properties of these metrics should be that they must provide a measure that fairly compares two different systems with each other. As an example, increasing the amount of injected currents directly increases the voltage and as a result yields more sensitivity on the voltage changes. The metric should normalize such effects to provide a fair comparison between two sets of current patterns or two different systems. The two distinguishability factors used for these are the norm distinguishability and the power distinguishability [33].

The norm distinguishability factor takes the $L^2$ norm of the voltage difference between two measurements by evaluating the expression (2.12) where $\sigma_0$ and $\sigma_1$ are the two imaged conductivities, $j$ is the current density, $N$ is the number of electrodes, $k$ is the pattern number, $I_n^k$ is the current on the $n$th electrode in the $k$th pattern, and $V_n^k$ are the induced voltages on the same electrode during the same pattern.

$$D_{Norm}^k = \sqrt{\frac{\sum_{n=1}^{N} |V_n^k(\sigma_1, j) - V_n^k(\sigma_0, j)|^2}{\sum_{n=1}^{N} |I_n^k|^2}}. \quad (2.12)$$

The power distinguishability factor looks at the power difference between two measurements as shown in (2.13) where $P$ is the power and is the real part of $I \cdot V$.

$$D_{Power}^k = \frac{\sum_{n=1}^{N} |P_n^k(\sigma_1) - P_n^k(\sigma_0)|}{\sum_{n=1}^{N} |P_n^k(\sigma_0)|}. \quad (2.13)$$

It is notable that there are other distinguishability criteria introduced in the literature, such as the ones based on $L^1$ and $L^\infty$ norm of voltage differences [37, 38], but only the norm and the power distinguishability factors are used in evaluating the performance ACT5.
2.3.2.2 Standard Trigonometric Pattern

The set of current patterns that provide the highest distinguishability for a 2-D circular shape with homogeneous conductivity is known as the standard canonical trigonometric patterns. The definition of the trigonometric pattern set is as follows

\[
I_{S_i}^i = \cos \left( \frac{2\pi ij}{N} \right) \text{ for } 1 \leq i \leq N, 1 \leq j \leq \frac{N}{2}
\]

\[
I_{S_i}^{j+\frac{N}{2}} = \sin \left( \frac{2\pi ij}{N} \right) \text{ for } 1 \leq i \leq N, 1 \leq j < \frac{N}{2}
\]

(2.14)

where \( I_{S_i}^k \) is the current from the \( i \)th source during the \( k \)th pattern and \( N \) is the number of electrodes. Although the trigonometric patterns are developed for the case of circular shapes with homogeneous conductivity, they have been widely used as the de facto patterns in parallel-drive EIT systems for imaging shapes such as the thorax region where the circumference is not a perfect circle and the conductivity inside the body is not homogeneous [39].

2.3.2.3 Adaptive Current Patterns

As an alternative to the trigonometric patterns, parallel-drive EIT systems can adapt their current patterns based on the shape and the conductivity map of the object they are imaging. The adaptive patterns are described more in detail in Section 3.1.3, but the brief explanation is that adaptive current patterns maximize a the amount of information collected by the EIT system. This means that the applied current patterns can either be optimal for a given shape, or they can be optimal for distinguishing two different distributions of impedance in a given shape.

Although the default current pattern on ACT5 is the trigonometric pattern, it supports application of any arbitrary current patterns and can find the optimal patterns. This work focuses on the adaptive current patterns that are optimal for a given shape.

2.4 Summary

This chapter covered the fundamentals of the EIT mathematical problem and introduces different categorization of EIT. It also covered some characteristics of the applied current patterns in a multiple-source EIT system. Next chapter introduces previous EIT
systems and talks about some of the ACT5 specifications.
CHAPTER 3

Background

This chapter covers the background information on EIT systems and introduces notable EIT systems that have been developed and used in clinical settings. It also covers some characteristics of the ACT5 system.

The first medical “Impedance Camera” that applies voltage to the body and reconstructs an image based on the current passing thorough it was introduced in 1978 [40]. The impedance camera could not reconstruct accurate images of thorax region, but the results indicated the feasibility of developing and using impedance tomography systems. In 1984, Applied Potential Tomography (APT) was the first successful EIT system that reconstructed an impedance image of a forearm [41]. Since then, numerous EIT systems have been developed, used, and refined. Each system was developed to address specific issues with certain requirements. These requirements, in addition to technological limitations, dictated that the systems have their own unique characteristics and capabilities.

EIT systems are designed and produced based on the various criteria that is imposed on them depending on their target application. Some characteristics of EIT systems include the region of interest (ROI), number of deployed electrodes, frame rate, frequency of excitation signals, maximum and range of SNR, voltage amplitude and phase amplitude measurement, and the drive pattern.

Some factors such as the number of electrodes and the drive pattern are directly related to the complexity of the system where a system with fewer electrodes is mostly easier and less expensive to produce, while more electrodes require more hardware and more design engineering to support other functions such as data communication. Additionally, parallel-drive systems have more sources in their architecture while pair-drive systems simplify that by using only one or two sources and a multiplexer.

Another factor that dictates certain criteria on the system is the application of the system. For example, brain imaging with EIT requires lower frequencies compared to other applications [42]. Another effect of the application is the speed of changes in the impedance.
As an example, EIT systems that are aimed to capture air ventilation and blood perfusion activity require a high frame rate to be able to capture the fast pace of changes in impedance of the lungs and heart, while systems that are designed to detect cancerous tissue do not need high a frame rate, but may need to apply multiple frequencies to yield a spectroscopic view of the tissue.

Tables 3.1 and 3.2 provide a comprehensive list of most notable EIT systems and their characteristics. The tables are broken into three main sections based on the pattern drive of the system and each section is sorted by the year of introduction. ACT5 specifications are shown at the bottom of the table.

Note that the specifications in columns of Tables 3.1 and 3.2 are mostly for best-case scenarios for each system and not their typical working specifications. As an example, the frame rates of systems are usually highest when they are using the fewest number of electrodes. Additionally, for systems that take images in multiple frequencies for spectroscopic view, the frame rate is lowered when the number of frequencies increases. The SNR of the systems also usually varies based on the frequency of the operation.
### Table 3.1: EIT Systems - I

<table>
<thead>
<tr>
<th>EIT system</th>
<th>Year</th>
<th>Drive pattern</th>
<th>ROI</th>
<th>Electrodes</th>
<th>Max. frame rate (Max. count)</th>
<th>Frequency</th>
<th>Max. SNR (dB)</th>
<th>Record phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheffield (APT) [41, 43]</td>
<td>1987</td>
<td>Pair</td>
<td>Thorax</td>
<td>16</td>
<td>10</td>
<td>51 kHz</td>
<td>12 bits</td>
<td>No</td>
</tr>
<tr>
<td>UCLH Mark 1a [44]</td>
<td>1999</td>
<td>Pair</td>
<td>Brain</td>
<td>16</td>
<td>-</td>
<td>225 Hz - 65 kHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Sheffield Mk3.5 [45, 46]</td>
<td>2001</td>
<td>Pair</td>
<td>Thorax</td>
<td>8</td>
<td>25</td>
<td>2 kHz - 1.62 MHz</td>
<td>12 bits-40 dB</td>
<td>Yes</td>
</tr>
<tr>
<td>BCDD [7]</td>
<td>2001</td>
<td>Pair</td>
<td>Breast</td>
<td>256</td>
<td>0.05</td>
<td>10 kHz</td>
<td>16 bits</td>
<td>No</td>
</tr>
<tr>
<td>UCLH Mark 1b [47]</td>
<td>2002</td>
<td>Pair</td>
<td>Brain</td>
<td>64</td>
<td>3</td>
<td>225 Hz - 77 kHz</td>
<td>50</td>
<td>-</td>
</tr>
<tr>
<td>Khul Mark 1 [48]</td>
<td>2007</td>
<td>Pair</td>
<td>Brain</td>
<td>64</td>
<td>3</td>
<td>10 Hz - 500 kHz</td>
<td>12 bit</td>
<td>Yes</td>
</tr>
<tr>
<td>Enlight - Timpel [49, 50, 51]</td>
<td>2008</td>
<td>Pair</td>
<td>Thorax</td>
<td>32</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>PulmoVista® 500 [52, 53]</td>
<td>2011</td>
<td>Pair</td>
<td>Thorax</td>
<td>16</td>
<td>30</td>
<td>80 kHz - 130 kHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Swisstom BB2 [54, 55]</td>
<td>2012</td>
<td>Pair</td>
<td>Thorax</td>
<td>32</td>
<td>50</td>
<td>150 kHz</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Dartmouth [56]</td>
<td>2014</td>
<td>Pair</td>
<td>-</td>
<td>32</td>
<td>110</td>
<td>100 Hz - 1 MHz</td>
<td>90</td>
<td>Yes</td>
</tr>
<tr>
<td>Yang &amp; Jia [57]</td>
<td>2017</td>
<td>Pair</td>
<td>-</td>
<td>32</td>
<td>546</td>
<td>10 kHz - 1 MHz</td>
<td>82.8</td>
<td>Yes</td>
</tr>
<tr>
<td>ACE1 [58, 59]</td>
<td>2018</td>
<td>Pair</td>
<td>Thorax</td>
<td>32</td>
<td>33.2</td>
<td>&lt;200 kHz</td>
<td>90</td>
<td>Yes</td>
</tr>
<tr>
<td>FMMU-EIT5 [60]</td>
<td>2018</td>
<td>Pair</td>
<td>Brain</td>
<td>16</td>
<td>-</td>
<td>1 kHz - 190 kHz</td>
<td>83</td>
<td>Yes</td>
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<tr>
<td>CRADL v2.0 [61]</td>
<td>2019</td>
<td>Pair</td>
<td>Thorax</td>
<td>16</td>
<td>122</td>
<td>45 kHz - 1 MHz</td>
<td>12 bits</td>
<td>Yes</td>
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<tr>
<td>Dartmouth [62]</td>
<td>2020</td>
<td>Pair</td>
<td>Prostate</td>
<td>20</td>
<td>26</td>
<td>500 Hz - 1 MHz</td>
<td>66-76</td>
<td>Yes</td>
</tr>
<tr>
<td>Sheffield Mk3a [63]</td>
<td>1995</td>
<td>Interleaved</td>
<td>-</td>
<td>8I + 8V</td>
<td>33</td>
<td>9.6 kHz - 1.2 MHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>OXBACT-5 [64]</td>
<td>2008</td>
<td>Interleaved</td>
<td>Thorax</td>
<td>16I + 64V</td>
<td>25</td>
<td>1 kHz - 100 kHz</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>KIT4 [65]</td>
<td>2008</td>
<td>Interleaved</td>
<td>-</td>
<td>16I + 80V</td>
<td>31.25</td>
<td>1 kHz - 120 kHz</td>
<td>97.5</td>
<td>Yes</td>
</tr>
<tr>
<td>Rapin et al. [66]</td>
<td>2018</td>
<td>Interleaved</td>
<td>Thorax</td>
<td>8I + 8V</td>
<td>-</td>
<td>49.04 Hz - 50.96 kHz</td>
<td>-</td>
<td>No</td>
</tr>
<tr>
<td>ACT2 [67]</td>
<td>1988</td>
<td>Parallel</td>
<td>Thorax</td>
<td>32</td>
<td>2</td>
<td>15 kHz</td>
<td>69.1</td>
<td></td>
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<tr>
<td>OXBACT-3 [68]</td>
<td>1994</td>
<td>Parallel</td>
<td>-</td>
<td>32</td>
<td>25</td>
<td>10 kHz - 160 kHz</td>
<td>12 bits</td>
<td>Yes</td>
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<tr>
<td>ACT3 [69, 70, 71]</td>
<td>1994</td>
<td>Parallel</td>
<td>Thorax</td>
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<td>Breast</td>
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<td>Applied current/voltage</td>
<td>Passive/Active</td>
<td>Cable type</td>
<td>Injection strategy</td>
<td>Shunt Z compensation</td>
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<td>Current</td>
<td>Passive</td>
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<td>Adjacent</td>
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<td>-</td>
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<tr>
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<td>Passive</td>
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<td>Belt</td>
<td>Current</td>
<td>-</td>
<td>-</td>
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<td>Passive</td>
<td>-</td>
<td>Programmable</td>
<td>SD + Freq. Scaling</td>
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<td>Passive</td>
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<td>Coaxial</td>
<td>-</td>
<td>SD + Sink Current Meas.</td>
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<td>Triaxial</td>
<td>Programmable</td>
<td>SD</td>
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<tr>
<td>Rapin et al.</td>
<td>Vest</td>
<td>Current</td>
<td>Active</td>
<td>-</td>
<td>Programmable</td>
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<td>-</td>
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<td>Programmable</td>
<td>SD + GIC</td>
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<td>Programmable</td>
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<td>Triaxial</td>
<td>Programmable</td>
<td>Howland + GIC</td>
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<td>-</td>
<td>Howland + NIC</td>
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<td>Programmable</td>
<td>Digital</td>
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</table>
3.1 ACT5 Specifications

As shown in Table 3.1, majority of the EIT systems fall under the category of pair-drive systems. Most of the parallel-drive systems that have been developed are also not in use anymore. ACT5 is a multiple-source EIT system, developed with novel design criteria that makes it a distinct EIT system.

3.1.1 Simplified Circuitry

A challenge for EIT systems is to compensate the effects of the shunt impedance on the output of their electrodes. This compensation has been mostly done through analog means such as using negative impedance converter (NIC) and general impedance converter (GIC) circuits that negate the effects of the shunt capacitance [83, 84]. Despite their effectiveness, these circuits tend to work well over only a narrow frequency range. This means that for an EIT system to be able to operate at multiple frequencies, there needs to be multiple compensation circuits or they need to be adjusted. For example, in KHU Mark2 system [77], each channel has 4 GIC circuits to cover the whole spectrum of operation. These circuits introduce complexity to the system, increase chances of failure, and, due to analog nature of the compensation method, require individual attention to each source for their calibration.

Another method for minimizing the effects of the shunt impedance is driving the shields of the cables with the same signal that is injected into the body. A common technique in systems with triaxial cables is to ground the outer shield to reduce the noise, while the inner shield is driven to reduce the stray capacitance [83, 84]. Despite the effectiveness of this method, it still requires additional analog circuits for the driver which introduces complexity and points of failure to the system. Additionally, a second shield adds weight to the cables that can reduce the mobility of the subject or cause the electrodes to detach from the body if their weight is not supported.

More recently, active electrodes are used where the current source is placed close to the electrode on the skin which ensures that the intended current is passed through the body, and a voltage buffer is placed at the electrode to ensure high input impedance for the voltmeter [59]. One of the main issues with the active electrodes is that for hygienic purposes, they need to be cleaned after each use. Another problem with the active electrodes is that the existence of electrical circuitry close to the body might cause discomfort for the patients.
With the adaptive current sources used in ACT5, which digitally compensate for the effects of shunt impedance (Section 4.3.1), there is no need for GIC, NIC, shield drivers, or other similar analog circuits for impedance compensation. By eliminating these components, ACT5 is able to have simplified electronics, grounded-shielded cables, and passive electrodes, removing the need for sterilizing electronic components after each use. Additionally, ACT5 is capable to switch quickly between different frequencies of operation without the need to wait for signal transients.

3.1.2 Autonomous & Fast Calibration

Another feature of ACT5 that distinguishes it from most of the other EIT systems is its ability to calibrate itself while it is attached to subjects. This feature is particularly useful for long-term monitoring purposes where certain environmental elements such as the changes in temperature, drift of electronic component values, or changes in positioning of the patient might cause the calibration values to change. In many systems, recalibration requires the system to be disconnected from the patient while ACT5 can recalibrate itself without being disconnected. Additionally, the continuous shunt impedance measurement technique implemented in ACT5 is another novel technique that helps the system maintain its integrity in long-term monitoring applications.

Another calibration feature of ACT5 is the speed of calibration. Many conventional analog circuits require component values to be adjusted either manually or electronically, such as digital potentiometers, in a nulling process which can be slow. These elements are eliminated in ACT5, so there is no need to spend time on their calibration. Furthermore, for high accuracy of measurements on shunt impedance values, more conventional systems have to spend a considerable time prior to the operation to reduce the error by making a large number of measurements to suppress the measurement noise. ACT5 can start imaging operation with estimated shunt impedance values that are not highly accurate, and then refine the impedance values during the operation of the system. This real-time calculations further reduces the time spent on the calibration of the system.
3.1.3 Adaptive Patterns

One of the main beneficial, yet least explored, aspects of parallel-drive EIT systems is their ability to adapt their current patterns for a given shape and conductivity map so that they provide maximum amount of information for image reconstruction. Although various methods to find and apply optimal patterns have been implemented and tested [85, 86], these experiments have mostly been offline and on saline tanks. To our knowledge, no previous system has computed and applied optimal current patterns based on data collected from the human body.

ACT5 is designed so that it is fully programmable where it can apply any current pattern, defining both amplitude and phase for each electrode, to any number of electrodes of up to 48 electrodes. This means that ACT5 is capable of applying optimal patterns to any given object, including humans.

Optimal patterns can be defined either defined for a given shape, or can be defined to optimally distinguish two impedance maps of a given shape. In both cases, the only requirement for applying the optimal patterns is for the EIT system to be able to apply any given valid current patterns.

The process of finding optimal patterns for a given shape is shown in Fig. 3.1. The goal of the process is to find the current patterns that are eigenvectors of the impedance network, so that the measured voltages are scalar multiple of the applied current. Initially at this process, an arbitrary set of orthogonal current patterns, e.g. the trig patterns, is applied to the body and the voltages are measured. The system checks if the voltages are scaled version of the applied currents and if not, it updates the current patterns as shown in Fig. 3.1. This process is repeated until the optimal currents are determined.

3.2 Summary

This chapter covered the previous work in the EIT by introducing previously developed EIT systems. It also discussed some of the characteristics of ACT5 that make it a distinct EIT system. Next chapter provides and overview of the hardware components in ACT5.
Figure 3.1: Proposed process of finding optimal current patterns for an arbitrary shape.

- Apply initial orthogonal current patterns
- Measure voltages
- Are voltages scalar multiple of applied currents?
  - Yes
    - Take last applied current patterns
  - No
    - Update the current patterns and apply them
- Measure new voltages
- Make voltages average to 0
- Normalize pattern amplitude
- Calculate eigenvalues and eigenvectors of $R$ matrix
- New current patterns = eigenvectors $\times$ applied currents
CHAPTER 4

ACT5 Hardware Overview

The major hardware components of the ACT5 system include the PC, the controller, the source channels, and the calibration channel. The controller is connected to the PC through a Universal Asynchronous Receiver/Transmitter (UART) connection. At the same time, the controller, the source channels, and the calibration channel are mounted on a VME backplane and communicate with each other through Serial Peripheral Interface (SPI) protocol, with the controller acting as the SPI controller and the source channels and the calibration channel acting as peripheral devices. An overview of the ACT5 system architecture is show in Fig. 4.1. This chapter reviews these hardware components, except the communication links. The communication hardware and the communication process of both the UART link between the PC and the controller, and the SPI link between the controller board and the source and calibration boards is detailed in Chapter 7.

Figure 4.1: Overview of ACT5 architecture
4.1 The PC

The PC in ACT5 is responsible for providing a GUI to the users, communicating the necessary information to/from the controller, and reconstructing the images. The GUI provides an environment for setting up the necessary parameters on the EIT hardware for its proper operation. The information set on the GUI is then transmitted to the controller through a UART communication link. The GUI also provides the necessary information to the user including the images, and safety and fault alerts.

The PC can show real-time reconstruction of images by using reconstruction algorithms with relatively low computational complexity that do not require excessive computation power. It also keeps a record of all the data that is received from ACT5 so that they can later be used to reconstruct better images through reconstruction algorithms that are too computationally intensive to carry out in real-time.

There are 2 GUIs developed for ACT5, the clinical GUI that provides high-level control for the system and is most useful for use in a clinical environment and the developer GUI that provides low-level control for the operator and is useful for debugging the system. The GUIs are created using MATLAB App Designer [87].

4.1.1 Clinical GUI

The clinical GUI of ACT5, shown in Fig. 4.2, provides a user-friendly interface to the users that is most suitable to be used in clinical environment. The boxes in dotted red highlights some of the features. The clinical GUI provides multiple functionalities to the users. The main task of the GUI is real-time image reconstruction which plots the conductance and the susceptance images. The reconstructed images are further explained in Section 10.1.2. In addition to the images, the average admittance values and the range of the change in the conductance and the susceptance images are shown to the user. User can also select to see other information such as the trace of the average admittance, and the ECG measurements. The clinical GUI also provides a real-time electrode contact status alert to the users so that in cases where an electrode either has a loose contact or is completely detached, it alerts the user by changing the status of the faulty electrode on the interface. Additionally, user has control over numerous settings in the system to best utilize the retrieved information.
It is notable that for the clinical GUI, the graphical interface components that are related to user interactions or provide information to the user have been developed by the members of Electrical Impedance Tomography lab of Colorado State University. The contributions of UAlbany have been the integration of the clinical GUI with the low-level functions that enables it to communicate and setup ACT5 correctly.

4.1.2 Developer GUI

The developer GUI, shown in Fig. 4.3, provides functionalities with more control on the hardware compared to the clinical GUI. User can set the registers on the channels individually, and manually read data from ACT5. Multiple debugging tools, functions related to the calibration process, functions related to pattern setup, and functions related to post-processing of the data and image reconstruction are also incorporated in the developer GUI.

4.2 The Controller

The controller, implemented on a Xilinx Artix 7 FPGA, relays messages to/from the PC and peripheral circuits. The messages from the PC are either intended to be relayed
to other peripheral circuits, i.e. the sources and the calibration channel, or to be received by the controller itself. In the first case, the controller forwards the message to the desired peripheral circuit through an SPI communication link and, in the second case, it takes the necessary actions depending on the message from the PC.

The controller also synchronizes the operations in ACT5 since it can manage the timings of actions taken by the peripheral circuits. The controller is also responsible for collecting measurement information from the peripheral devices and transmitting them back to the PC. Other responsibilities of the controller include safety intervention in severe cases and communicating to the PC information that shows the status of the system.

The controller board is shown in Fig. 4.4. On the board, the FPGA module, the USB-UART converter module and the connector to the backplane are shown. Although using

![Figure 4.3: A snapshot of the developer GUI used in ACT5.](image-url)
FPGA and UART chips might be more cost effective and consume less power. FPGA and the UART modules are used as a way of speeding up the implementation. The controller FPGA, in addition to the Cmod A7 FPGA module are further detailed in Chapter 8.

4.3 The Source Channels

Source channels are the current sources that apply the current to the body and measure the resulting voltage. Each source channel consists of a Xilinx Artix-7 FPGA acting as a Direct Digital Synthesis (DDS) signal generator, a 16-bit DAC, an 18-bit ADC, and the analog circuits for the current source and voltmeter. The DDS generates digital sinusoidal waves at the frequency of operation in the range from 5 kHz to 1 MHz. Each source can supply up to 2 mA of peak-to-peak current and can measure voltages of signals with 1 V of maximum peak-to-peak amplitude. The analog circuits use 0.1% precision, low temperature coefficient resistors and, under maximum swing of voltage, each channel has a signal-to-noise ratio of over 96 dB. The inner structure of the channel FPGA is detailed in Chapter 8.
4.3.1 Adaptive Current Sources - Voltmeter

ACT5 uses a Howland voltage-to-current converter as its current source. To pump the current, the FPGA outputs digital values for the voltage on its DAC bus which is fed to an LTC1668, 16-bit, 50 MSPS DAC that is clocked at 24 MHz. The analog output of DAC is then used to drive the Howland current source, which uses an AD8033 OpAmp and 0.1% precision resistors.

Voltage measurement on the channels is done through an AD4002, 18-bit, 2 MSPS ADC that is used at 1.2 MSPS and converts the voltages and inputs them serially to the FPGA through ADC_Data pin.

To compensate for the lost current through the shunt impedance of the current sources, ACT5 uses adaptive current sources [88, 89]. The adaptive current sources in ACT5 output a current that is equivalent to the sum of the desired current that is supposed to pass thorough the body and the lost current on the shunt impedance. A simplified diagram of the adaptive current sources is shown in Fig. 4.5.

\[
I_S = I_D + \frac{V_o}{Z_o}.
\] (4.1)

For proper operation, the adaptive current sources require the value of shunt impedance \((Z_o)\) and the desired current that is supposed to be injected to the body \((I_D)\). The adaptive sources monitor the output voltage \((V_o)\) and set their output current \((I_S)\) as

Figure 4.5: Adaptive current source

Ideally, with this adaptation technique, the current injected to the body will be the desired current and the lost current through the shunt impedance will be compensated by
the source outputting extra current.

The functionality of adaptive current sources depend on correct measurement of the shunt impedance and real-time voltage measurement. Shunt impedance measurement is discussed in Section 6.4.3 and Chapter II. The complex baseband representation of the real-time voltage is created with the help of a Hilbert transform. The Hilbert transform introduces a $90^\circ$ phase shift on the measured voltage. The original received voltage and the phase-shifted value are used to create the instantaneous voltage measurement that is used to adjust the output current. The structure and processing of the adaptive current source is further detailed in Section 8.3.

4.3.2 Cables

The cables used in an EIT system affect the shunt impedance values. The adaptive current sources of ACT5 provide the opportunity to use a wide variety of cables with various lengths. Each source has an SMB connector that a cable can be plugged into. The default cables used in ACT5 are single-shielded cables with length of 1.5 m with an SMB connector at one end and a snap connector at their other end.

4.3.3 Source Boards

One of the source boards is shown in Fig. 4.6. To minimize the footprint of source channels and maximize the shared resources for communication, 4 source channels are implemented on a single PCB. These source boards have 5 cable connectors on their front end, 4 of which are used to connect each individual source to the load (an electrode) and one of the connectors is used to connect the sources to the calibration channel on the analog side.

Since all the source boards are similar both in hardware and FPGA firmware, physical jumpers are used to give an address to each board. Each source board has a set of 4 pins that can be connected to a 0 V pin or a 3.3 V pin through jumpers, creating a 4-bit address for each board, ranging from $4'b0000$ to $4'b1011$. By setting these jumpers properly, each board can be electronically differentiated from others through the 4-bit address that is assigned to it.
4.4 The Calibration Channel

Calibration channel, implemented on a separate calibration board, is responsible for calibrating the system. It can act as a voltmeter, a current-meter, and a voltage supply during the calibration process. It also acts as a virtual ground electrode for the operation of the system and monitors the safety of the operation. Since the calibration board is unique, the address is hardcoded on the FPGA as 4’b1100.

The calibration board is shown in Fig. 4.7. The calibration FPGA is further detailed in Chapter 8.
4.5 Backplane and Signals

The controller board, the source boards, and the calibration board must share resources such as the power supplies, must be synchronized with a common clock, and must communicate with each other through communication channels. In ACT5, the boards are mounted on a VME64 J1 backplane [90] (IEEE 1014) which provides these functionalities, as shown in Fig. 4.8. The backplane is installed on a CCK220-3U subrack [91]. There are 96 available lines on the backplane bus in three rows of A, B, and C where each row has 32 lines numbered from 0 to 31.

![VME backplane of ACT5, mounted on subrack.](image)

Some of the backplane lines are dedicated to certain signals and the rest of the lines can be used for general purposes. Table 4.1 lists the lines with set roles.

Table 4.1: Backplane lines with specific roles

<table>
<thead>
<tr>
<th>Role</th>
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<tbody>
<tr>
<td>Clock</td>
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</tr>
<tr>
<td>+5 V</td>
<td>A32, B32, C32</td>
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<tr>
<td>+12 V</td>
<td>C31</td>
</tr>
<tr>
<td>-12 V</td>
<td>A31</td>
</tr>
<tr>
<td>Ground</td>
<td>A09, C09, A11, A15, A17, A19, B20, B23</td>
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4.5.1 Clock Distribution

In ACT5, the controller generates a 24 MHz clock signal and distributes this signal through the backplane to all the peripheral units. The clock available on the FPGA modules have an accuracy of 50 ppm, meaning that there is a possibility of up to 1.2 kHz deviation from the 24 MHz clocks if they are generated separately by each FPGA. In the worst-case
scenario, one FPGA could operate at 1.2 kHz above the nominal value and another FPGA could operate at 1.2 kHz below the nominal value. In a $\approx 1\text{ ms}$ burst with a synchronous start, the two sinusoidal waves by the two FPGAs will have a mismatch of $\approx 85\text{ ns}$ for the burst ending time. Since the accuracy of individual clocks depend on the temperature and their age, this deviation can only increase through time and under different operational conditions.

On the other hand, by sharing the clock signal among all the FPGA through the backplane, ACT5 ensures that all the current bursts with a synchronous start will end in sync with each other. Under this scenario, The only possible difference between the bursts can be due to phase difference in clock due to the different distances of source boards from the controller board on the backplane. This possible phase difference is going to be minimal and will not pose any problem as its effects will be measured and compensated for during the calibration process. Further, deviation of the clock frequency due to temperature changes and aging also would not cause any difference in the burst length among various channels. Additionally, there are digital hazards of miscommunication of data when it is moved between two different clock domains. Sharing the clock through the backplane to all FPGAs eliminates this hazard.

4.5.2 Command Signals

Certain commands in the system which are shared between all the channels, have dedicated physical lines on the backplane. Table 4.2 lists these command signals, their roles, the backplane lines they use, and the initiator device. Activation of these signals depends on the mode of operation and/or the detection of faults in the system.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Role</th>
<th>Backplane Lines</th>
<th>Initiator Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Go</td>
<td>Initiates the sinusoidal burst</td>
<td>B19</td>
<td>Controller</td>
</tr>
<tr>
<td>Reset</td>
<td>Resets all the peripheral devices</td>
<td>C19</td>
<td>Controller</td>
</tr>
<tr>
<td>STOP</td>
<td>Halts all actions on peripheral devices</td>
<td>C30</td>
<td>Calibrator</td>
</tr>
</tbody>
</table>
4.5.3 Communication Signals

The controller communicates with the peripheral devices through SPI communication protocol. The communication signals and their dedicated backplane lines are listed in Table 4.3. Since each source board has 4 channels on them, there is a dedicated SPI link for each of these channels, consisting of an SPI_CLK line which clocks the communication link, a chip_select line which indicates if the link is active, two parallel paths for controller out/peripheral in (COPI) signal through COPI[1:0] lines which transfers data from controller to peripheral devices, and a two parallel paths controller in/peripheral out (CIPO) signal through CIPO[1:0] lines which transfers data from the peripheral devices to the controller. The reason for assigning two bits for COPI and CIPO signals is that the data transferred between the devices largely consists of real and imaginary parts. By using two physical lines, the complex values can be transferred in one burst of communication. Besides these lines, there is a 4-bit board_select signal which indicates the board that the controller is communicating with. In cases where the controller is sending data to all peripheral devices, it uses the global_chip_select line which overrides individual chip_select and board_select signals. The signals and the protocols are further detailed in Chapter 7.

4.6 Summary

This chapter covered the major hardware components in ACT5, including the PC, the controller board, the source boards, the calibration board, and the backplane. Next chapter talks about the modes of operation in ACT5.
### Table 4.3: Communication signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Role</th>
<th>Backplane Lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>global_chip_select</td>
<td>Indicates message is intended for all peripheral devices</td>
<td>B25</td>
</tr>
<tr>
<td>board_select[3:0]</td>
<td>Selects the board that controller is communicating with</td>
<td>{C08,A08,C07,A07}</td>
</tr>
<tr>
<td>SPI_CLK_1</td>
<td>12 MHz clock distributed from the controller</td>
<td>C27</td>
</tr>
<tr>
<td>chip_select_1</td>
<td>indicates if the SPI line is active or inactive</td>
<td>C26</td>
</tr>
<tr>
<td>COPI_1[1:0]</td>
<td>Controller Out, Peripheral In.</td>
<td>{C28,C29}</td>
</tr>
<tr>
<td>CIPO_1[1:0]</td>
<td>Controller to peripheral devices data transmit</td>
<td>{A03,A04}</td>
</tr>
<tr>
<td>SPI_CLK_2</td>
<td></td>
<td>B16</td>
</tr>
<tr>
<td>chip_select_2</td>
<td></td>
<td>C15</td>
</tr>
<tr>
<td>COPI_2[1:0]</td>
<td></td>
<td>{B17,B18}</td>
</tr>
<tr>
<td>CIPO_2[1:0]</td>
<td></td>
<td>{A01,A02}</td>
</tr>
<tr>
<td>SPI_CLK_3</td>
<td></td>
<td>C05</td>
</tr>
<tr>
<td>chip_select_3</td>
<td></td>
<td>A05</td>
</tr>
<tr>
<td>COPI_3[1:0]</td>
<td></td>
<td>{A06,C06}</td>
</tr>
<tr>
<td>CIPO_3[1:0]</td>
<td></td>
<td>{A30,A29}</td>
</tr>
<tr>
<td>SPI_CLK_4</td>
<td></td>
<td>C02</td>
</tr>
<tr>
<td>chip_select_4</td>
<td></td>
<td>C01</td>
</tr>
<tr>
<td>COPI_4[1:0]</td>
<td></td>
<td>{C03,0C4}</td>
</tr>
<tr>
<td>CIPO_4[1:0]</td>
<td></td>
<td>{A28,A27}</td>
</tr>
</tbody>
</table>
CHAPTER 5
Modes of Operation

ACT5 has two modes of operation. The first mode of operation is the calibration mode where the system measures its unknown parameters. The second mode of operation is the imaging mode where the system collects the necessary data to reconstruct images by applying currents to the body and measuring voltages on the electrodes.

5.1 Calibration

In order for the system to work correctly, the variables that are sent to the FPGAs must be set properly and the variables that are returned from the FPGAs must be interpreted in a meaningful way. As an example, if a channel must apply a current with certain amplitude, this amplitude must be translated accurately to digital values that are set on the channel FPGA, and if a channel is measuring its voltage and returning the digital value of the voltage to the PC, those digital values should be converted to the correct, interpretable voltage measurements. Additionally, all channels need to be calibrated to the same standard so that even if there is an error in the calibration, it is applied equally to all the channels.

To find factors that do these conversions, ACT5 goes through a calibration process. At the first step of the calibration process, the calibration board has to calibrate its own voltmeter and ammeter. This helps with establishing the common standard for the source channels. At the next step, the calibration board applies a voltage to all the channels. The measured digital voltage on the channels and the measured voltage on the calibration board calibrates the voltmeter on the channels. During the next step, each channel individually applies a current to the calibration board. Since the ammeter on the calibration board is already calibrated, this step results in the current sources on the channels to be calibrated. Finally, since at this stage the current sources and the voltmeters on the channels are calibrated, certain impedance elements on the channels, that affect the performance of the system, are measured and their effects are taken into account. The calibration operation is explained in detail in Chapter 6.
5.2 Imaging

Another mode of operation for ACT5 is the imaging mode which collects the voltage data and sends it back to the PC. This mode can be broken down to two phases where, in the first phase, the patterns are set up on the channels and, in the second phase, currents are applied and the data is collected.

5.2.1 Pattern Setup

During the pattern setup phase, the variables that are necessary for operation of ACT5 are set on the peripheral devices and on the controller. The flow of the process is shown in Fig. 5.1. Some parameters are shared among all devices, including number of patterns, frequency, length of the burst, and the Hilbert scale. The parameters on the controller that are set include the frame rate, number of channels, and total number of frames. The calibration board parameters include the safety parameters and switches. On the channels, the gains for the patterns, the scale values related to the shunt impedance, and the switches are set. Setting patterns as ready on all the devices is the last step in this process which indicates that the system is ready to start the imaging process.

![Diagram of the pattern setup process](image)

Figure 5.1: Process of setting up the patterns on ACT5 at the beginning of the imaging process

5.2.2 Data Collection

At the time of data collection, ACT5 applies current to the body and measures the induced voltages. These voltages are transferred from the channels to the controller and to the PC. The controller, the channels, and the calibration board go through their own processes for this phase.
5.2.2.1 Controller Data Collection

The flow of actions on the controller during the imaging process is shown in Fig. 5.2. The controller signals the channels to apply current bursts to their load by activating the Go signal. In the rare case of the current burst being the first burst of the imaging process, the controller waits for the burst to end, otherwise the controller collects the voltage and the ECG data of the previous burst from the channels and the ground current data from the calibration board after activating the Go signal. The controller then checks the data for any safety issues and, if there are no detected hazards, it sends the data to the PC.

The process of activating the burst, collecting the data from peripheral devices, and sending the data to the PC repeats until the controller reaches the end of the imaging process, i.e. it collects the required number of image frames. When the imaging process is done, the controller stops activating the Go signal, and collects the data from the peripheral devices for the last time and sends the data to the PC. The controller then enters an idle state and waits for further instructions from the PC.

It is notable that the controller continuously monitors the STOP signal on the backplane and when the signal is activated, it halts all process. Safety features are explained more in Chapter 9.

Figure 5.2: Process on the controller that collects data from peripheral devices and forwards them to the PC.

5.2.2.2 Channel Data Collection

Figure 5.3 shows the imaging process on the channels. Upon receiving the Go signal, channels select the gain that should be applied during the pattern and apply their current
burst to the load. During the burst, channels measure the induced voltage and record the ECG measurements. The channels save the measured voltage and ECG values at the end of the burst.

Simultaneous to the current burst being active, the channels monitor the communication link on the backplane and whenever the controller activates the communication links, channels transfer the saved data to the controller.

On the channels, in addition to the STOP signal, the voltages are also checked for safety issues such as overflow and, in case of a fault, safety protocols are activated (Chapter 9).

![Diagram]

Figure 5.3: Process on the channels that applies current bursts and saves the voltage. A communication module sends back the last saved voltage values back to the controller.

5.2.2.3 Calibration Data Collection

The imaging process on the calibration channel is shown in Fig. 5.3. Upon receiving the Go signal, calibration channel measures and monitors the ground current during the burst. It then checks the measured ground current for any possible fault and, if there is no fault detected, it saves the measured ground current. In case of a fault, the STOP flag is raised and the safety protocols are activated (Chapter 9).

As the burst is active, the calibration channel monitors the backplane communication link and whenever the communication link is activated by the controller, the calibration channel returns the saved current values back to the controller.

5.3 Summary

This chapter talked about the modes of operation in ACT5 and covered the process of the imaging mode. Next chapter details the calibration mode of ACT5.
Figure 5.4: Process on calibration board that measures and saves the ground current. A communication module sends back the last saved current value back to the controller.
CHAPTER 6
Calibration

This chapter describes the calibration process in ACT5. In the calibration process, the factors and scales that relate the digital variables and the digital measurements to real physical values are measured. The factors that are measured during the calibration process are shown in Table 6.1.

Table 6.1: Calibration Factors

<table>
<thead>
<tr>
<th>Factor</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calibration board</td>
<td>$V_{\text{factor}}$ Converts the digital values of voltage sensed on the calibration board to physical values of voltage</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{factor}}$ Converts the digital values of current sensed on the calibration board to physical values of current</td>
</tr>
<tr>
<td>Channels</td>
<td>$V_{\text{correct}}$ Converts the digital values of voltage sensed on channel to physical values of voltage</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{scale}}$ Converts the physical values of intended current to the digital values that are set on FPGAs</td>
</tr>
</tbody>
</table>

The calibration process of the system is done in multiple phases. In each phase, the PC and the controller cooperate to measure the calibration factors autonomously.

In the initial phases, the calibration board factors are found. For this, calibration board applies voltages to a 2 kΩ precision resistor. By changing the switch configurations, first the voltage on the resistor is measured, then the current passing through the resistor is measured and, at the end, since the resistor is terminated with a virtual ground as opposed to a real ground, the voltage of the virtual ground is measured so that the true current passing through the resistor can be determined.

During the later phases, the factors related to the channels are measured where once the calibration board applies a voltage to all the channels and then each channel applies a current to the calibration board which is measured.

To correct the effects that some impedance values in the circuit network have on the calibration values, these impedance values are also measured in the calibration process and
their effects are taken into account.

It is important to note that although individual channels of ACT5 can operate in the frequency range of 5 kHz to 1 MHz, for practical reasons, ACT5 is only calibrated between the frequencies of 11 kHz to 375 kHz, and when it is tested on human subjects it shows the best results from 11 kHz to 150 kHz.

6.1 Preparation Phase

The first step of calibration process is preparing the system by setting the constant variables of the system as shown in Fig. 6.1. These constants include the frequency of operation, the length of bursts, and the number of measurements that should be done in each of the consecutive calibration phases.

![Figure 6.1: Preparation phase of calibration process](image)

6.2 Calibrating the Calibration Circuit

After the preparation process, ACT5 calibrates the calibration circuit. This step requires a flexible calibration circuit that can measure both voltage and current. By using these two modes of operation, ACT5 determines the factors that convert the digital measurements of voltage and current on the calibration board to the physical values of voltage and current.

6.2.1 Calibration Board Circuit

The calibration process requires specific hardware support with flexible switch configurations. Figure 6.2 shows the calibration board circuit diagram. The circuit is consisted of a voltmeter, a current source, a current-to-voltage converter, and a 2 kΩ precision resistor. There are also 7 switches (SW) on the calibration board. Depending on how the switches are connected on the calibration board, the calibration board can either sense voltages to either
calibrate its own voltmeter and the voltmeter of the channels, or it can sense current by passing them through the current-to-voltage converter and calibrate its own current source and the current source of the channels. All these processes are done through consecutive phases of calibration.

![Diagram of calibration board](image)

**Figure 6.2: Overview of circuit diagram of the calibration board**

### 6.2.2 Phase I - Measuring $v_{\text{factor}}$

The first phase of calibration is measuring the $v_{\text{factor}}$ that converts the digital voltage readings on the calibration board to physical voltage values. For this purpose, the calibration board is set to apply the maximum amplitude of signal which is 0.5 V on the precision resistor and the calibration bus is disconnected. The switches are set as shown in Table 6.2. In this configuration, current is passed through the precision resistor to the virtual ground. At the same time, the voltage on the precision resistor is measured.

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 6.2: Switch connections on calibration board during phase I of calibration**

The processes of this calibration phase are shown in Fig. 6.3 and Fig. 6.4. The PC sets up the variables on ACT5 and orders the controller to execute phase I of calibration. The
controller measures the needed values and returns the data back to the PC where the data is processed and the $V_{\text{factor}}$ is calculated using expression 6.1.

$$V_{\text{factor}} = \frac{V_{\text{cal actual}}}{V_{\text{cal phase I}}} = \frac{0.5}{V_{\text{cal phase I}}}$$

(6.1)

where $V_{\text{cal phase I}}$ is the digital voltage reading.

Figure 6.3: PC phase I of calibration process

The amplitude and the phase of $V_{\text{factor}}$ plotted against frequency are shown in Fig. 6.5.

### 6.2.3 Phase II - Measuring $I_{\text{factor}}$

The second phase of calibration measures the $I_{\text{factor}}$ that converts the digital values of current measured on the calibration board to the physical values of current. This phase is broken down to two sections, one for measuring the current passing through the resistor and one for measuring the virtual ground voltage that terminates the resistor. Both of these phases are similar to Phase I with the difference being the switch configuration.
Figure 6.5: (a) Amplitude, and (b) phase of $V_{\text{factor}}$ in frequency range of 11 kHz to 375 kHz.

6.2.3.1 Phase II-I - Measuring Current

To measure the current, the switches on the calibration are set as shown in Table 6.3. The calibration board applies the same signal as phase I to the precision resistor. The current passes through the current-to-voltage converter circuit and the converted voltage ($I_{\text{cal phase II-I}}$) is sensed.

Table 6.3: Switch connections on calibration board during phase II-I of calibration

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The PC steps for this phase are shown in Fig. 6.6 while the controller process is the same as phase I as shown in Fig. 6.4.
Set the gain on calibration board as max_calibration_amp
Set switches so that the load current is measured
Command controller to execute Phase II-I of calibration

Save I_{Cal}
Average the returned data
Wait for data from controller

Figure 6.6: PC phase II-I of calibration process

6.2.3.2 Phase II-II - Measuring Ground Voltage

The current passing through the precision resistor is drained at a virtual ground node which is the input to the current-to-voltage-converter. To accurately measure the ground current, the switches are set such that the voltage of the virtual ground node ($V_{\text{cal gnd phase II-II}}$) is measured while the current of previous phases is applied to it as shown in Table 6.4. The PC process of this phase is shown in Fig. 6.7 and the controller process is the same as phase I as shown in Fig. 6.4.

Table 6.4: Switch connections on calibration board during phase II-II of calibration

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
</table>

Figure 6.7: PC phase II-II of calibration process

To measure $I_{\text{factor}}$, first the impedance of the precision resistor is set according to the following expression where $f$ is the frequency of the excitation signals

$$\text{Precision Impedance} = \frac{1}{\frac{1}{2000.15\Omega} + (j2\pi f \cdot (0.1\,\text{pF}))}.$$ (6.2)
Note that although the precision resistor is exactly 2 kΩ, since it is connected in series with switches, an extra 0.15 Ω resistance and a 0.1 pF capacitance are added to the resistor value. We then use this impedance value to determine the actual current passing through the resistor by taking the voltage difference between its two terminals which are measured in phase I and phase II-II, and $V_{\text{factor}}$ as shown below

$$I_{\text{actual}} = \frac{(V_{\text{cal phase I}} - V_{\text{cal gnd phase II-II}}) \cdot V_{\text{factor}}}{\text{Precision Impedance}}.$$  \hspace{1cm} (6.3)

At the end, $I_{\text{factor}}$ is calculated by using the following expression

$$I_{\text{factor}} = \frac{I_{\text{actual}}}{I_{\text{cal phase II-I}}}.$$  \hspace{1cm} (6.4)

The amplitude and the phase of $I_{\text{factor}}$ vs. frequency are shown in Fig. 6.8.

### 6.3 Calibrating the Source Channels

Next step in calibrating ACT5 is to calibrate the source channels. The components of source channels that require calibration are the current source and the voltmeter, depicted in Fig. 6.9. All the source channels are connected to the calibration board through the calibration bus and it is through this bus that all the channels are calibrated with respect to the calibration board. To calibrate the channels, first the calibration board applies a voltage to all the channels and this voltage is measured on the channels and on calibration board. The values are used to calibrate the voltmeters on the sources. During the next step of calibration, each channel individually applies a current to the calibration board. The sensed current in the calibration board in addition to the sensed voltage on the channels yield the calibration factor for the current sources.

One note for calibration of the channels is that certain impedance values on the sources’ impedance network play a role in determining the calibration factors, so it is vital to measure these impedance values and incorporate them into the calibration process.
Figure 6.8: (a) Amplitude, and (b) phase of $I_{\text{factor}}$ in frequency range of 11 kHz to 375 kHz.

6.3.1 Channel Circuit

The circuit on the sources is consisted of a Howland current source, a voltmeter, and two switches that connect the channel to either the calibration bus or the load cable. The complete circuit diagram for the channels, including parasitic impedances, is shown in Fig. 6.9.

The value of some elements in the circuit are chosen at the design time. These elements include the blocking capacitor, the output resistor, and the voltmeter resistor and capacitor. The value of some other elements in the system can be extracted from the data sheet of their components. These values include the capacitance value of the switches, the series resistance value of switches, and the series resistance and inductance value of the cables.
Table 6.5: Known Impedance Values on the Source Circuits

<table>
<thead>
<tr>
<th>Component</th>
<th>Impedance Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{Blocking}}$</td>
<td>$10 \text{nF}$</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{output}}$</td>
<td>$100 \text{k}\Omega$</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{Volmeter}}$</td>
<td>$1 \text{M}\Omega$</td>
<td></td>
</tr>
<tr>
<td>$C_{\text{Volmeter}}$</td>
<td>$1 \text{pF}$</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{Switch-Series}}$</td>
<td>$0.15 \Omega$</td>
<td></td>
</tr>
<tr>
<td>$C_{\text{Switches}}$</td>
<td>$3.5 \text{pF} - 4.2 \text{pF}$</td>
<td>Depends on switch configuration</td>
</tr>
<tr>
<td>$R_{\text{Cable-Series}}$</td>
<td>$0.32 \Omega \text{m}^{-1}$</td>
<td>Depends on length of the cable</td>
</tr>
<tr>
<td>$L_{\text{Cable-Series}}$</td>
<td>$1.77 \text{mH} \text{m}^{-1}$</td>
<td>Depends on length of the cable</td>
</tr>
</tbody>
</table>

![Circuit diagram of a source channel](image)

Figure 6.9: Circuit diagram of a source channel.

### 6.3.2 Phase III

During phase III of calibration, the conversion factor to determine channel voltages from their digital values to their physical values, $V_{\text{correct}}$, is measured. For this purpose, all the channels are connected to the calibration bus with their switches set as shown in Table 6.6. The calibration board is also connected to the calibration bus and switches are configured as shown in Table 6.7. During this step, the calibration board outputs its maximum amplitude current and the channels are set to output zero current. The current passes through the precision resistor to the ground and the induced voltage on the resistor
is measured on the calibration board and on all the channels through the calibration bus. The applied voltage can be calculated by using $V_{\text{factor}}$ and the calibration board voltages as

$$V_{\text{applied}} = V_{\text{cal phase III}} \cdot V_{\text{factor}},$$  \hspace{1cm} (6.5)

where $V_{\text{cal phase III}}$ is the digital voltage measured on the calibration board. In turn, $V_{\text{correct}}$ of $i$th channel can be calculated as following

$$V_{\text{correct channel } i} = \frac{V_{\text{applied}}}{V_{\text{channel } i}},$$  \hspace{1cm} (6.6)

where $V_{\text{channel } i}$ is the digital voltage measured on the $i$th channel. The processes shown in Fig. 6.10 and Fig. 6.11 depict the steps that the PC and controller go through to execute this phase of calibration.

Table 6.6: Switch connections on all source channels during phase III of calibration

<table>
<thead>
<tr>
<th>Calibration Bus SW</th>
<th>Load SW</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.7: Switch connections on calibration board during phase III of calibration

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 6.10: PC process for phase III of calibration.

The amplitude and the phase of $V_{\text{correct}}$ vs. frequency for all 32 channels are shown in Fig. 6.12
6.3.3 Phase IV

The last factor of the system is the $I_{\text{scale}}$ which converts the intended physical current values to their digital representation so that they can be sent to the current sources. For this phase, the calibration gain is set to be zero and the switches are set as shown in Table 6.8. With this switch configuration, the current injected from the calibration bus is passed through the current-to-voltage converter and is sensed and measured on the calibration board.

Table 6.8: Switch connections on calibration board during phase IV of calibration

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Since only one channel should be applying a current at a time during this phase of calibration, channel switches are set to connect to the calibration bus individually as shown in Table 6.9.

Table 6.9: Switch connections on one source channel during phase IV of calibration

<table>
<thead>
<tr>
<th>Calibration Bus SW</th>
<th>Load SW</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Channels are then set to apply the maximum amplitude of current when it is their turn to be calibrated. Since channels have 16-bit output signals in two’s complement representa-
Figure 6.12: (a) Amplitude, and (b) phase of $V_{\text{correct}}$ in frequency range of 11 kHz to 375 kHz.

The digital value of this maximum signal, $i_{\text{digital}}$, can be written as

$$i_{\text{digital}} = 2^{15} - 1. \quad (6.7)$$

During the burst of each channel, the current on the calibration bus is measured on the calibration board, and the voltage on the calibration bus is measured on the channel. Hence, the applied current from $i^{th}$ channel can be written as

$$I_{\text{applied}} i = I_{\text{cal phase IV i}} \cdot I_{\text{factor}} + V_{\text{correct channel i}} \cdot V_{\text{channel phase IV i}} \cdot G_{\text{cal bus i}} \quad (6.8)$$

where $I_{\text{cal phase IV i}}$ is the current sensed on the calibration bus by the calibration board for the $i^{th}$ channel, $V_{\text{channel phase IV i}}$ is the voltage of the calibration bus on the channels side...
sensed by the $i$th channel, and $G_{\text{cal bus } i}$ is the admittance of the calibration bus seen from the $i$th channel which is measured separately as explained in Section 6.4. Using the final value of the applied current from the channel, $I_{\text{scale}}$ can be calculated for the $i$th channel as

$$I_{\text{scale chnl } i} = \frac{i_{\text{digital}}}{I_{\text{applied } i}}. \quad (6.9)$$

Figures 6.13 and 6.14 depict the process of this phase of calibration on the PC and the controller.

![Figure 6.13: PC phase IV of calibration process](image)

![Figure 6.14: Controller phase IV of calibration process](image)

6.4 Measuring the Impedance Values

During the last phase of the calibration process, various impedance values in ACT5 electric circuits are measured. These impedance values are the Howland shunt impedance, calibration bus shunt impedance, and the cable shunt impedance.
A straightforward method of measuring an impedance is to apply a current \(I\) and measure the resulting voltage \(V\). This complex voltage, in conjunction with the frequency of operation, is used to measure the impedance values \(Z\), where

\[
Z = \frac{V}{I}. \tag{6.10}
\]

The shunt impedance \(Z\), at frequency \(f\), can then be decomposed into parallel resistance \((R)\) and capacitance values \((C)\)

\[
R = \Re(Z) \tag{6.11}
\]

\[
C = \frac{\Im(Z)}{2\pi f}, \tag{6.12}
\]

where \(\Re()\) is the real part and \(\Im()\) is the imaginary part.

ACT5 utilizes this method to measure various impedance values. The only limit in this strategy is that if the impedance of the load is significant enough to cause a voltage overflow for the voltmeter, the measurements will not be correct. Hence, the main consideration for impedance measurement is to apply a current small enough to not cause a voltage overflow.

### 6.4.1 Howland Shunt Impedance

First impedance value measured during the calibration process is the Howland shunt impedance value \((Z_{\text{Howland}})\) shown in Fig. 6.9. For this purpose, both switches on the channel are opened as shown in Table 6.10 a small current is applied and the voltage is measured.

Table 6.10: Switch connections on source board for Howland shunt impedance measurement.

<table>
<thead>
<tr>
<th>Calibration Bus SW</th>
<th>Load SW</th>
</tr>
</thead>
</table>

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
</table>

Based on the measured voltage and the applied current, the impedance of the channel before the switches \((Z_{\text{before SWs}})\) is measured. The Howland impedance is then calculated as

\[
Z_{\text{Howland}} = Z_{\text{before SWs}} \cdot \frac{Z_{\text{blocking}} + Z_{\text{board}}}{Z_{\text{board}} - Z_{\text{before SWs}}} \tag{6.13}
\]
where $Z_{\text{Cblocking}}$ is the impedance of the blocking capacitor and $Z_{\text{board}}$ is

$$Z_{\text{board}} = Z_{\text{ROutput}} \parallel Z_{\text{Voltmeter}} \parallel Z_{\text{Switches}}$$

(6.14)

where the impedance values of each of the components are given in Table 6.5 with $Z_{\text{Switches}}$ equal to 4.2 pF in this configuration.

### 6.4.2 Calibration Bus Shunt Impedance

Measuring the shunt impedance on the calibration bus is an important step, specifically for phase IV of the calibration. For this step, the switches on one channel are set as shown in Table 6.11 and the switches on the calibration board are set as shown in Table 6.12.

Table 6.11: Switch connections on one channel for calibration bus shunt impedance measurement.

<table>
<thead>
<tr>
<th>Calibration Bus SW</th>
<th>Load SW</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image.png" alt="Switch Configuration" /></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.12: Switch connections on calibration board for calibration bus shunt impedance measurement.

<table>
<thead>
<tr>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image.png" alt="Switch Configuration" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

By this switch configuration, when the source applies a small current to the output, it passes through all the impedance parallel to the source in the calibration bus branch ($Z_{\text{calBus-Branch}}$). The parallel impedance of the calibration bus ($Z_{\text{CalBus-Parallel}}$), consisting of $R_{\text{CalBus-Parallel}}$ and $C_{\text{CalBus-Parallel}}$ shown in Fig. 6.9, is then calculated as

$$Z_{\text{CalBus-Parallel}} = \frac{1}{Z_{\text{Howland}} - Z_{\text{calBus-Branch}}} \cdot \frac{1}{Z_{\text{calBus-Branch}} - Z_{\text{board}}} - R_{\text{Switches-Series}}$$

(6.15)

where $Z_{\text{Howland}}$ is given through (6.13), $Z_{\text{Cblocking}}$ is the impedance of the blocking capacitor, $R_{\text{Switches-Series}}$ is the series resistor of the switches, and $Z_{\text{board}}$ is given in (6.14) with $Z_{\text{Switches}}$.
equal to 3.5 pF.

### 6.4.3 Open Circuit Output Impedance

Last step of measuring the impedance values in ACT5 is measuring the shunt impedance of the channels when cable is connected to them. For this step, the switches on the channels are set as shown in Table 6.13 and a small current is applied to the output. The measured voltage yields the value for the shunt impedance. This shunt impedance value is known as the Open-Circuit (OC) impedance value ($Z_{OC}$). The OC impedance values are the ones used in the adaptive current sources introduced in Section 4.3.1. The OC resistance and capacitance measurements are shown in Fig. 6.15.

Table 6.13: Switch connections on source board for channel shunt impedance measurement.

<table>
<thead>
<tr>
<th>Calibration Bus SW</th>
<th>Load SW</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Switch Connections" /></td>
<td><img src="image" alt="Switch Connections" /></td>
</tr>
</tbody>
</table>

### 6.5 Calibration Post-Processing

Last step of the calibration process is incorporating the circuit model and the impedance measurement in the calibration values. This step is specifically important due to the fact that the voltmeter and the current source on each channel are separated by the blocking capacitor, $C_{\text{blocking}}$, and are not truly parallel to each other. In the post-processing phase of the calibration, the measured impedance values and $I_{\text{scale}}$ are updated through an iterative process. The schematic of the circuit and its components are shown in Fig. 6.16.

To correct the measured impedance values and $I_{\text{scale}}$, the current that passes through the calibration bus switch ($I_{\text{CalBus-SW}}$) during phase IV of the calibration is written as

$$I_{\text{CalBus-SW}} = \frac{1}{Z_{\text{CalBus-Parallel}} + R_{\text{Switch-Series}} \cdot (V_{\text{channel phase IV}} + Z_{\text{CalBus-Parallel}} \cdot I_{\text{cal phase IV}})}.$$  \hspace{1cm} (6.16)

The current through the calibration bus switch is then used to calculate the voltage on the current source ($V_{\text{Source}}$) during phase IV of calibration as

$$V_{\text{Source}} = V_{\text{channel phase IV}} \cdot \frac{Z_{\text{Board}} + Z_{\text{Cblocking}}}{Z_{\text{Board}}} + I_{\text{CalBus-SW}} \cdot Z_{\text{Cblocking}}.$$  \hspace{1cm} (6.17)
Figure 6.15: (a) Resistive, and (b) capacitive components of OC shunt impedance measurement of channels in frequency range of 11 kHz to 375 kHz for all 32 channels.
The total applied current from the source is then calculated as

\[ I_{\text{applied}} = I_{\text{CalBus-SW}} + \frac{V_{\text{channel phase IV}}}{Z_{\text{Board}}} + \frac{V_{\text{Source}}}{Z_{\text{Howland}}} \]  

(6.18)

The applied current is used to update the value of \( I_{\text{scale}} \) as

\[ I_{\text{new scale}} = \frac{i_{\text{digital}}}{I_{\text{applied}}} \]  

(6.19)

The updated \( I_{\text{scale}} \) is then used to update the measured impedances in the system (\( Z_{\text{before SWs}} \) and \( Z_{\text{calBus-Branch}} \)) as following

\[ Z_{\text{New before SWs}} = Z_{\text{before SWs}} \cdot \frac{I_{\text{new scale}}}{I_{\text{scale}}} \]  

(6.20)

\[ Z_{\text{New calBus-Branch}} = Z_{\text{calBus-Branch}} \cdot \frac{I_{\text{new scale}}}{I_{\text{scale}}} \]  

(6.21)

These updated impedance values are then used in (6.16) and the process is repeated until \( I_{\text{scale}} \) converges to its final value. The final amplitude and the phase of \( I_{\text{scale}} \) vs. frequency for all 32 channels are shown in Fig. [6.17]
Figure 6.17: (a) Amplitude, and (b) phase of $I_{scale}$ in frequency range of 11 kHz to 375 kHz.

### 6.6 Summary

This chapter discussed the calibration process in ACT in detail. This process includes calibrating the calibration board, calibrating the channels, and post-processing of the data to refine the calibration factors. Next chapter covers the communication protocols and data processing in the ACT5 system.
CHAPTER 7
Communication

There are two main directions of data flow in ACT5, from the PC to ACT5, and from ACT5 to the PC. The data flow from the PC to ACT5 mostly consists of setting the variables on the channels. The flow of data from ACT5 to the PC is mostly made up of voltage and ECG readings from the sources. This chapter describes the communication system in ACT5 by introducing the hardware backbone and then explaining the protocols of data transmissions.

7.1 Communication Hardware

There are two main communication paths for data to flow in ACT5 as shown in Fig. 7.1. A UART link between the PC and the controller, and multiple SPI links between the controller and the peripheral devices build the backbone of the communication hardware.

![Overview of ACT5 architecture](image)

Figure 7.1: Overview of ACT5 architecture
7.1.1 PC and Controller

The PC is connected to the controller FPGA through a UART link. The PC uses an FT232H USB-to-UART converter chip for the link and, on the controller side, the UART logic is written in Verilog and implemented on the FPGA. UART transactions are done one byte at a time from both the PC side and the controller side. The speed of the data transmission is set at 6 Mbit/sec. Each UART byte transmission consists of 1 start bit and 1 stop bit. This means that each 8-bit packet of data is transmitted through 10 bits on the UART channel. At full capacity, the UART link provides a bandwidth of 4.8 Mbit/sec or 600 kB/sec for data communication. A sample waveform of a UART packet is shown in Fig. 7.2, where the idle logic is set at high and a start bit of 0 indicates the beginning of the packet. The 8-bit packet is then transmitted sequentially and at the end, the line goes back to high value to indicate the end of the packet.

![UART Packet](image)

Figure 7.2: UART Packet waveform

7.1.2 Controller and Peripheral Devices

The communication link between the controller and the peripheral devices, including the sources and the calibration board, is done through the backplane links and follows the SPI protocol. The timing diagram of the SPI protocol waveform used in ACT5 is shown in Fig. 7.3.

There are 4 channels on each source board, hence for the controller to talk to a channel, it needs to first select the board, and then communicate with the specific channel. The controller uses board_select[3:0] and chip_select signals to select the target device and then communicates with the peripheral device through the COPI[1:0] and CIPO[1:0] lines. Note that each of the 4 sources have a dedicated chip_select line, so the controller can simultaneously communicate with all 4 sources on a board.
7.2 Communication Protocols

The commands sent from the PC are either targeted at the controller or at the peripheral devices.

7.2.1 PC to Controller

In some cases, the PC sends commands directed at the controller. These commands invoke an action on the controller that might, or might not, affect other peripheral devices. Additionally, these commands have variable length, based on the information that is needed to be sent to the controller, with most of them being only 1 byte. Table 7.1 lists the commands that are sent from the PC with the controller being their target device. The first transmitted byte is the command code. The controller either takes action on the received code or waits for the rest of the information to be transmitted from the PC to complete its action.

7.2.2 PC to Peripheral

PC also sends data to the sources and the calibration board. For this, the controller acts as a relay of information where it receives the data from the PC and in turn sends it to the target device. The structure of these messages is shown in Fig. 7.4. At first PC sends the command code to the controller. A list of these codes are shown in Table 7.2. The commands that are directed at the controller have numerical values greater than 127 and the commands that are directed to the peripheral devices have a numerical value of less than 128. This threshold directs the controller on whether it should forward the message to the
### Table 7.1: Command list from PC to controller

<table>
<thead>
<tr>
<th>Command</th>
<th># Bytes</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Go</td>
<td>1</td>
<td>128</td>
<td>Activates the Go signal once</td>
</tr>
<tr>
<td>Reset</td>
<td>1</td>
<td>255</td>
<td>Activates the Reset signal once</td>
</tr>
<tr>
<td>Set channel count</td>
<td>2</td>
<td>129</td>
<td>Sets maximum number of channels</td>
</tr>
<tr>
<td>Set frame rate</td>
<td>3</td>
<td>130</td>
<td>Sets the frame rate of imaging</td>
</tr>
<tr>
<td>Patterns ready/Stop patterns</td>
<td>1</td>
<td>131</td>
<td>Sets patterns ready/Stops imaging</td>
</tr>
<tr>
<td>Set calibration address</td>
<td>2</td>
<td>132</td>
<td>Sets the calibration board address</td>
</tr>
<tr>
<td>Set max Go counter</td>
<td>4</td>
<td>133</td>
<td>Sets the number of Go signals</td>
</tr>
<tr>
<td>Set max Go enabled</td>
<td>1</td>
<td>134</td>
<td>Toggles the Go counter enable</td>
</tr>
<tr>
<td>Execute phase I, II-I, II-II</td>
<td>1</td>
<td>135</td>
<td>Calibration Codes</td>
</tr>
<tr>
<td>Execute phase III</td>
<td>1</td>
<td>136</td>
<td>Calibration Codes</td>
</tr>
<tr>
<td>Execute phase IV</td>
<td>1</td>
<td>137</td>
<td>Calibration Codes</td>
</tr>
<tr>
<td>Set phase IV target device</td>
<td>2</td>
<td>138</td>
<td>Calibration Codes</td>
</tr>
<tr>
<td>Burst one channel</td>
<td>1</td>
<td>139</td>
<td>Apply a burst for testing purposes</td>
</tr>
<tr>
<td>Execute Imaging Process</td>
<td>1</td>
<td>140</td>
<td>Start imaging process</td>
</tr>
<tr>
<td>Set number of patterns</td>
<td>2</td>
<td>141</td>
<td>Sets number of patterns per image</td>
</tr>
<tr>
<td>Pause/Resume imaging</td>
<td>1</td>
<td>142</td>
<td>Pauses/Resumes the imaging process</td>
</tr>
</tbody>
</table>

After the command code is sent, PC sends the address of the target device to the controller. This address can be for an individual target device, or it can be for *all* peripheral devices. For example, when the PC is setting the frequency of operation which is the same for all the sources, it is more beneficial to send it once to all the channels rather than sending it individually. At the same time, when setting up the current gains for patterns, each channel has a unique series of gains which means that data should be transferred to one specific target rather than all of the channels. The last two bytes that are sent from the PC are the data information that is needed to be set on channels. These variables, such as the frequency, the current gain values, length of the burst, etc. are converted to their 16-bit values and then broken into two bytes, the 8 most significant bits ($MSB$), and the 8 least significant bits ($LSB$). The MSB and the LSB bytes are then transferred to the controller. In cases where the command from the PC does not contain any information for the variables, such as telling the sources to activate or deactivate their safety features, these two bytes of data are set as 0.
7.2.3 Controller to Peripheral

The messages from the controller to the peripheral devices is sent through a 32-bit data packet as shown in Fig. 7.5. The first 5 bits of the message is the command. In cases where the controller is relaying data to the peripheral devices from the PC, the command is equal to the command sent from the PC (Table 7.2). In other cases, such as when the controller is automatically reading voltages from the channels during the imaging process, the command is set as 5’b11111 which peripheral devices will ignore.

The next three bits are for reading back registers from the peripheral devices. By default, peripheral devices return back their matched filter output which, for the channels, translates to their sensed voltages. In case the controller needs to read a value besides the matched filter output, it can request it via changing the “read address” section of the packet. The peripheral devices will transmit the requested value at the time of the next communication data transfer.

The next 16 bits of the message are dedicated to data that is used to set the values of registers on the peripheral devices. The last 8 bits of the packet do not contain useful information and are reserved. Additionally, under current architecture of ACT5 only one of the COPI lines is used and the second one is reserved. These reserved communication spaces can be used for future expansion of the system.
Table 7.2: Command list from PC to source

<table>
<thead>
<tr>
<th>Command</th>
<th>Code (First Byte)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>0</td>
<td>Sets frequency</td>
</tr>
<tr>
<td>Gain real</td>
<td>1</td>
<td>Sets single real gain</td>
</tr>
<tr>
<td>Gain imag</td>
<td>2</td>
<td>Sets single imaginary gain</td>
</tr>
<tr>
<td>Length</td>
<td>3</td>
<td>Sets burst length</td>
</tr>
<tr>
<td>Switches</td>
<td>4</td>
<td>Sets switches &amp; Adaptation</td>
</tr>
<tr>
<td>-</td>
<td>5</td>
<td>-Reserved-</td>
</tr>
<tr>
<td>Scale real</td>
<td>6</td>
<td>Sets real scale</td>
</tr>
<tr>
<td>Scale imag</td>
<td>7</td>
<td>Sets imaginary scale</td>
</tr>
<tr>
<td>Hilbert scale</td>
<td>8</td>
<td>Sets Hilbert scale</td>
</tr>
<tr>
<td>Gain real queue</td>
<td>9</td>
<td>Sets patterns real gain</td>
</tr>
<tr>
<td>Gain imag queue</td>
<td>10</td>
<td>Set patterns imaginary gain</td>
</tr>
<tr>
<td>Patterns ready</td>
<td>11</td>
<td>Sets patterns as ready</td>
</tr>
<tr>
<td>Gain address limit</td>
<td>12</td>
<td>Sets number of patterns</td>
</tr>
<tr>
<td>Gain real step</td>
<td>13</td>
<td>Sets transition step of real gain of patterns</td>
</tr>
<tr>
<td>Gain imag step</td>
<td>14</td>
<td>Sets transition step of imaginary gain of patterns</td>
</tr>
<tr>
<td>Smooth transition</td>
<td>15</td>
<td>Activates smooth transition of signals</td>
</tr>
<tr>
<td>-</td>
<td>16-18</td>
<td>-Reserved-</td>
</tr>
<tr>
<td>Toggle safety</td>
<td>19</td>
<td>Activates/Deactivates the safety</td>
</tr>
<tr>
<td>Max current</td>
<td>20</td>
<td>Sets maximum current on calibration board</td>
</tr>
<tr>
<td>Min current</td>
<td>21</td>
<td>Sets minimum current on calibration board</td>
</tr>
<tr>
<td>Broadband limit</td>
<td>22</td>
<td>Sets maximum broadband limit on calibration board</td>
</tr>
<tr>
<td>-</td>
<td>23-31</td>
<td>-Reserved-</td>
</tr>
<tr>
<td>Read MF out</td>
<td>32</td>
<td>Sends real and imag MF on SPI lines</td>
</tr>
<tr>
<td>Read MF out</td>
<td>33</td>
<td>Sends real and imag MF on SPI lines</td>
</tr>
<tr>
<td>-</td>
<td>34-35</td>
<td>-Reserved-</td>
</tr>
<tr>
<td>Read DC Latch</td>
<td>36</td>
<td>Sends DC value on real SPI line</td>
</tr>
</tbody>
</table>

7.2.4 Peripheral to Controller

Peripheral devices send data, and in some cases error messages, back to the controller. Since the communication between the controller and the peripheral devices is done through the SPI protocol, the messages from the peripheral devices are 32-bit messages. The two CIPO lines allow the peripheral devices to transfer both the real and the imaginary parts of the measurements back to the controller as shown in Fig. 7.6. Since the voltage measurements on channels is only 24 bits of data, the ECG measurement is broken to two 8-bit parts and are appended to the voltage measurements to finalize the 32-bit data packet. In some occasions, such as measuring the DC values on channels, the peripheral circuits only need to use one of
the two messages to return the data. In such cases, the data is returned on the Real line and the Imaginary line is set as 32'b0. Another exception for the messages is when the channels have encountered an error, such as overflow of voltages. In this case, channels return the maximum possible values of 32'b011...111 on both lines.

Figure 7.6: Structure of 32-bit SPI message from peripheral devices to the controller. The 24-bit real and imaginary parts of the data are transmitted simultaneously on separate lines. The 16-bit ECG signal is broken to two 8-bit sections and added to the end of the SPI packet.

7.2.5 Controller to PC

The controller mostly acts as a relay in sending the data it has collected from the peripheral devices back to the PC. This means that the controller has to break down the two 32-bit messages in 8 byte segments of data and transmit them back to the PC as shown in Fig. 7.7.

Figure 7.7: Breaking down each of the two 24-bit peripheral messages to two 3-byte sections and the 16-bit ECG signal to two separate bytes to be transmitted back to the PC from the controller.

7.3 Flow Control

The data is streaming from the controller to the PC at high speed, especially during the imaging operation. This makes flow control an essential component to guarantee the integrity and correctness of the data. ACT5 uses two different flow control schemes to ensure that the received data on the PC is correct. One is on the hardware level and is active during any form of operation and one on the software level during the imaging process.
7.3.1 Hardware Flow Control

The first level of flow control of data in ACT5 is done on the hardware level where the controller monitors the Request to Send (RTS) signal it receives from the UART module. In case the UART module cannot take any new data from the controller, it raises its RTS signal. The RTS signal of the UART module is connected to the Clear to Send (CTS) pin of the controller FPGA where it is constantly monitored. When the controller notices the rise of CTS, it halts all serial communication transactions with the PC until the CTS flag is set back to normal.

Note that data flow from the PC to controller is significantly slower compared to the data flow from the controller to the PC. Additionally, the firmware of the controller is designed so that it can handle non-stop input of data where no input data packets are queued due to other services on the firmware, while the data transfer from the controller to the PC has to be handled by the PCs internal capabilities which do not guarantee seamless acceptance of data through the serial input. Hence, there is a more critical need for hardware flow control from the controller to the PC as opposed to the reverse direction.

7.3.2 Software Flow Control

Despite the effectiveness of hardware flow control where it insures that the data is transferred correctly most of the time, in occasional cases there are missing bytes in the data that causes misalignment in the data stream. ACT5 implements a software flow control where at the end of each frame of data, eight extra bytes are sent from the controller to the PC, named the End-of-Frame (EOF) data. Of the eight extra bytes, the first 3 bytes are codes for hardware faults (see Section 9.2.3), the next 2 bytes are the frame number, and the last three bytes are hardcoded as \{0, 85, 255\} so that the PC can check if there has been any loss in the UART data transfer. Upon receiving the full frame of data, PC checks for the three \{0, 85, 255\} bytes at the end of the frame and, if there is any mismatch, PC will know that there was an error in data transmission.

After detecting the error, the faulty data frame is discarded and the system resynchronizes itself with the new incoming data frame.
7.4 Received Data

The PC interprets the received data based on the mode of operation where the structure of received data during the calibration process is not similar to structure of the data during the imaging process.

7.4.1 Calibration Data

During the calibration process, the data received from ACT5 depends on the calibration phase. The volume of the received data depends on the number of bursts ($K$) that is set for the calibration process to repeat.

- Phase I, II-I, II-II: In these phases, data is received from the calibration board. Each data point is 8 bytes which makes the total received data to be $8 \cdot K$ bytes of information for each phase.

- Phase III: During phase III, received data is from the calibration board followed by all source channels. Assuming that there are $N$ channels in the system, the total volume of received information is $8 \cdot (N + 1) \cdot K$ bytes.

- Phase IV: In this phase, at each step, data is received from calibration board and a single source channel. Since each channel is calibrated separately, there will be $N$ steps, making the total received data to be $8 \cdot 2 \cdot N \cdot K$ bytes.

7.4.2 Image Data

At the time of imaging, the controller collects the data at the end of each burst from all the channels (voltages) and the calibration board (virtual ground current). During the next burst, the controller sends the voltage and current values back to the PC. The general flow of the processing the image data is shown in Fig. 7.8.

Since the voltage and current values consist of real and imaginary parts, and each part is represented by a 24-bit number (3 bytes), and the ECG data is 2 bytes, for $N$ number of electrodes, $(N + 1) \cdot 8$ bytes of data is transferred for each pattern. As there are $M$ patterns in ACT5, where $M \leq N$, the total amount of data for one frame is $M \cdot (N + 1) \cdot 8$ bytes, with
a maximum of $N \cdot (N+1) \cdot 8$. When ACT5 is operating with 32 electrodes and is applying all 32 patterns, this data is 8448 bytes per each frame.

At the end of the data, there is an extra 8 bytes of information for software flow control, record keeping of the frame number, and also communication of possible fault on the system. This makes the number of bytes for each frame to be $M \cdot (N+1) \cdot 8 + 8$. In MATLAB a callback function can be configured so that it is triggered whenever the number of bytes received from ACT5 has matched the number of bytes in a data frame.

The general structure of the received image data looks like

- Data: Frame data + error + frame counter + flow control

- Data packet: $\{P^1, ..., P^M, 3$-byte error, 2-byte counter, 0, 85, 255$\}$

where $\{P^1, ..., P^M\}$ is the data of the $M$ patterns with the structure of data for $j$th pattern ($P^j$) defined as

- Data of pattern $j$: $P^j = \{V^j_1, ECG^j_1, ..., V^j_N, ECG^j_N, I^j, RSVRD^j\}$

- Voltage from channel $i$, pattern $j$: $V^j_i = \{3$-byte real V, 3-byte Imaginary V$\}$

- ECG voltage from channel $i$, pattern $j$: $ECG^j_i = \{1$-byte MSB V, 1-byte LSB V$\}$
• Current from virtual ground, pattern $j$: $I^j = \{3$-byte real $I$, 3-byte Imaginary $I\}$

• Reserved data from virtual ground, pattern $j$: RSVRD$^j = \{2$ bytes reserved$\}$

If the end of the frame matches the pre-specified sequence of data, and there are no hardware faults on the systems, the data is broken to three parts: 1) The EIT voltage data, 2) the ECG voltage measurement data, and 3) the ground current data.

• The EIT voltage data is two matrices of size $(M \cdot N, 3)$, one for the real part of the voltage and one for the imaginary part of the voltage. The three bytes for each entry are converted to their 24-bit value by the following expression


Since the digital values are in the form of two’s complement, the negative numbers are converted to their corrected values

$$\text{Corrected } V_{Digital} = \begin{cases} V_{Digital}, & \text{if } V_{Digital} < 2^{24}. \\ V_{Digital} - 2^{25}, & \text{if } V_{Digital} \geq 2^{24}. \end{cases}$$ 

At this stage, each voltage entry is represented by two corrected digital values of voltage, one real and one imaginary. These two parts are combined to represent the total digital value of voltage.

$$\text{Total } V_{Digital} = \text{Corrected } V_{Digital} \text{ (real)} + i \cdot \text{Corrected } V_{Digital} \text{ (imaginary)}$$

The complex digital value of the voltage is then converted to the physical value of voltage by using the $V_{\text{correct}}$ factor introduced in Section 6.3.2.

$$\text{Physical Voltage Value} = V_{\text{correct channel}} \cdot \text{Total } V_{Digital}$$

Note that each channel has its unique $V_{\text{correct}}$ factor and this is taken into account during the calculation of the physical voltage values. At this stage, the voltage values are shaped into a matrix with size $(M, N)$ that represents the voltage readings on the channels.
Channel voltage measurements differ from the load voltages due to the series impedance components of cable shown in Fig. 6.9. The effects of cable series impedance can be approximately removed as shown in the following expression

\[
V_{\text{Load}} \approx V_{\text{channel}} - I_{\text{desired}} \cdot Z_{\text{Cable-Series}}. \tag{7.5}
\]

For a cable with length \( L \), with resistance per unit length of \( r \) and an inductance per unit length of \( l \), at frequency \( f \), (7.5) can be rewritten as

\[
V_{\text{Load}} \approx V_{\text{channel}} - I_{\text{desired}} \cdot L[r_{\text{Cable-Series}} + j \cdot 2\pi f \cdot l_{\text{Cable-Series}}]. \tag{7.6}
\]

By taking the applied current patterns and the length of the cables, the channel voltages are converted to the load voltages which builds a matrix of size \((M, N)\) which is called frame voltage matrix.

- The ECG measurements form one matrix of size \((M \cdot N, 2)\). Similar to the EIT voltage measurements, ECG measurements are converted to their digital values and corrected as

\[
\text{ECG Digital} = 256 \cdot \text{ECG}[15:8] + \text{ECG}[7:0]. \tag{7.7}
\]

\[
\text{Corrected ECG Digital} = \begin{cases} 
\text{ECG Digital}, & \text{if ECG Digital < } 2^{16} \\
\text{ECG Digital} - 2^{17}, & \text{if ECG Digital } \geq 2^{16}.
\end{cases} \tag{7.8}
\]

The digital ECG values are then converted to their physical values by dividing them by \(2^{18}\), which is equivalent to multiplying them with \(3.81 \mu \text{V}\). Finally, ECG data is converted to a matrix of size \((M, N)\) which is called frame ECG matrix.

- The ground current data forms two matrices of size \((M, 3)\), one for the real part of the current and one for the imaginary part of the current. Converting the raw ground current data to the their representative digital value is similar to the EIT data

\[
I_{\text{Digital}} = 256^2 \cdot I[23:16] + 256 \cdot I[15:8] + I[7:0]. \tag{7.9}
\]
Corrected $I_{\text{Digital}} = \begin{cases} 
I_{\text{Digital}}, & \text{if } I_{\text{Digital}} < 2^{24}. \\
I_{\text{Digital}} - 2^{25}, & \text{if } I_{\text{Digital}} \geq 2^{24}. 
\end{cases} \tag{7.10}$

$\text{Total } I_{\text{Digital}} = \text{Corrected } I_{\text{Digital}} \text{ (real)} + i \cdot \text{Corrected } I_{\text{Digital}} \text{ (imaginary)} \tag{7.11}$

To convert the digital values of ground current to the physical value of ground current, $I_{\text{factor}}$ introduced in Section 6.2.3.2 is used

$\text{Physical Current Value} = I_{\text{factor}} \cdot \text{Total } I_{\text{Digital}}. \tag{7.12}$

The ground current values are finally reorganized in a vector with size $M$ and is called frame current vector.

At the end of this process, the three matrices of frame voltage, frame ECG, and frame current represent all the information that ACT5 collects for a frame of data. ACT5 bundles these matrices through each imaging session. Assuming that ACT5 collects $P$ images on a given session, the final stored database would contain a voltage matrix with the size of $(P, M, N)$, and ECG matrix with the size of $(P, M, N)$, and a ground current matrix with a $(P, M)$ size. Other information saved in the database include the frequency of operation, the applied current patterns, information related to the operator and the subject, time and date of the images, and the annotations to the experiment that indicate major respiration points (such as “deep breath”, “breath hold”, etc.). The complete list of the data saved in the database is shown in Table 7.3.

### 7.5 Summary

This chapter covered the communication protocols in ACT5 and how the data is moved and processed between different components. Next chapter discusses the FPGAs used in ACT5 and their inner structure.
Table 7.3: Data fields in a dataset of ACT5, when collecting $P$ frames of images, with $N$ channels, and $M$ number of patterns at each channel.

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>frame_voltage</td>
<td>$(P, M, N)$</td>
<td>Load voltage for each electrode at each pattern</td>
</tr>
<tr>
<td>frame_current</td>
<td>$(P, M)$</td>
<td>Ground current for each pattern</td>
</tr>
<tr>
<td>frame_ECG</td>
<td>$(P, M, N)$</td>
<td>ECG voltage for each electrode at each pattern</td>
</tr>
<tr>
<td>EOF_data</td>
<td>$(P, 8)$</td>
<td>Faults, frame number, software flow control</td>
</tr>
<tr>
<td>frame_rate</td>
<td>1</td>
<td>Frame rate of imaging</td>
</tr>
<tr>
<td>frequency</td>
<td>1</td>
<td>Frequency of excitation signal</td>
</tr>
<tr>
<td>current_patterns</td>
<td>$(M, N)$</td>
<td>Applied current patterns</td>
</tr>
<tr>
<td>current_amplitude</td>
<td>1</td>
<td>Maximum amplitude of applied currents</td>
</tr>
<tr>
<td>annotations</td>
<td></td>
<td>Annotations made by operator</td>
</tr>
<tr>
<td>subject_ID</td>
<td></td>
<td>Subject identification number</td>
</tr>
<tr>
<td>operator</td>
<td></td>
<td>Name of the operator</td>
</tr>
<tr>
<td>location</td>
<td></td>
<td>Location of the data acquisition</td>
</tr>
<tr>
<td>date</td>
<td></td>
<td>Date of the data acquisition</td>
</tr>
</tbody>
</table>
CHAPTER 8

FPGAs

This chapter introduces the FPGAs used in ACT5 and describes their programmed functions.

8.1 FPGA Modules

For the FPGAs in ACT5, the Digilent Cmod A7 is used which is built around a Xilinx Artix-7 XC7A35T FPGAs as shown in Fig. 8.1. The Cmod A7 has 48 available pins which consists of a power pin, a ground pin, two analog input pins, and 44 pins that can be used as digital input and output pins for the FPGA. The FPGA can be programmed through Xilinx Vivado Design Suite software. All the FPGA codes are written in Verilog HDL.

![Cmod A7 board](image)

Figure 8.1: Cmod A7 board

8.2 Controller FPGA

The controller FPGA is responsible for smooth communication between the PC and rest of the ACT5 components, requiring multiple communication modules. A block diagram of the controller FPGA is shown in Fig. 8.2, depicting the major hardware components and the inputs and outputs of the FPGA and where those inputs and outputs are connected.

A UART module interfaces the USB-UART converter. Upon receiving a byte of data from the PC, the FPGA updates its state machine to either wait upon further instructions from the PC or take actions based on the received command. There are 4 SPI modules on the controller that communicate with source and calibration channels and they generally operate in parallel to increase the data throughput in the system.
In addition to acting as a communication hub, controller FPGA is also responsible for automating multiple tasks in the ACT5 system that speeds up various processes either for imaging or for calibration purposes. Furthermore, controller FPGA continuously monitors the received signals from source channels and the calibration channel to enact safety procedures in case of possible hazards in the system.

The floorplan and the resource utilization of the controller FPGA are shown in Fig. 8.3.

8.3 Source FPGA

The source FPGAs in ACT5 are responsible for generating the signal to feed the current sources and measuring the induced voltages. The block diagram of the source channel FPGAs is shown in Fig. 8.4 showing the registers, inputs and outputs, and functional blocks for current generation, ECG measurement, and the voltage measurement. Since only one
board can communicate with the controller at a given time, the source FPGAs compare the \texttt{board select} signal with the signal they receive from their address jumpers. If the \texttt{board select} signal matches the address, the source FPGA will activate the buffer that drives the \texttt{CIPO} line.

### 8.3.1 Current Generation - Forward Path

The main functionality of the source FPGAs is to generate and apply a sinusoidal current to the load. Figure 8.5 shows the forward path in the source FPGAs that outputs digital values of the current waveform. Based on the applied pattern, the gain address changes the output of the gain queue. The intended gain values are then added with the adjustment values to compensate the effects of shunt impedance. The corrected gain is then multiplied by the signal from the DDS to create the sinusoid waves. Since these computations are done in parallel paths for the real and the imaginary parts of the signal, these two signals are added at the end to create the desired digital sinusoid signal. The 16-bit output is then sent to DAC which converts the digital values to analog signal that can in turn drive a Howland current source to generate the analog output current.
8.3.2 DC Removal

The ADC on a channel constantly measures the voltage on the output of the current source. This voltage is specifically important when the current is being applied to the load. An undesirable property of the voltage measurements is that it has a relatively small DC bias due to noise and inaccuracies in the analog components. Any DC offset degrades the voltage measurement for the adaptive current sources loop and puts and offset unto the measured ECG waveform. Removing the DC value would help the source channels to reduce the noise in the system. For this, the DC value of the voltage is constantly measured on the source channels. Source channels measure and analyze the ADC input signal as shown in Fig. 8.6 to measure and remove the DC value on the input signal.

The implemented method of removing the DC from the signal can detect and remove slow changes in the DC value during the time of operation. This means that the implemented DC removal technique can dynamically keep the DC bias of the measured voltages to zero, even if the DC is changed due to temperature variation and component drift.

The DC removal circuit is a high-pass filter. The filter can be described by the following difference equation

\[ y[n] = x[n] - \sum_{k=0}^{n-1} \frac{y[k]}{2^{18}}, \]  

(8.1)
where $n$ is the time sample with the frequency of 1.2 MHz, $x[n]$ is the ADC signal, and $y[n]$ is the output of the filter. The time constant for the exponential convergence of this filter is approximately 218 ms. This response time is long enough to not interfere with ECG measurements, where significant changes like the QRS complex are shorter than 100 ms, and at the same time, it can capture the changes in the DC quickly for the adaptive current sources to work properly.
8.3.3 Voltmeter

The Voltmeter is a unit of the source channels that is active during the sinusoidal burst to measure the induced voltage on the channel. The functional process of voltage measurement and the block diagram of its hardware implementation are shown in Fig. 8.7. After the DC is removed from the ADC signal, the output is passed through a matched filter. That means that the signal is first multiplied by intended sine and cosine outputs of DDS. This moves the signal to baseband and provides the real and imaginary components of the voltage. The voltage during the burst is measured by accumulating 1024 samples during the burst taken after an initial wait period to allow transients to settle.

8.3.4 Current Generation - Feedback Path

Another major component of the source FPGAs is measurement of the gain adjustment that corrects the current output so that the desired current is delivered to the load. The functional process and the hardware block diagram of the current correction process are shown in Fig. 8.8. The received signal is passed through a Hilbert transform, which yields a 90° phase shift on the signal. The original and the transformed received signals are then multiplied by the DDS output which translates the signal to baseband, yielding the complex baseband representation of the voltage on the output at any given time. This voltage is then multiplied by a factor that represents the shunt admittance (scale) that yields the gain adjustment values. The values are processed by a moving average filter for smoothing.
8.3.5 ECG Measurement

Last module of the source channels is the ECG measurement hardware [92, 93], shown in Fig. 8.9. The ECG is measured by integrating the input signal over 1024 samples during the EIT sinusoidal burst.

The floorplan and the resource utilization of the source channels are shown in Fig. 8.10. The structure of source FPGA are more complex compared to the controller or the calibration FPGAs, hence source FPGAs have the highest utilization of resources available on them.
Figure 8.8: (a) Functional and (b) block diagram of gain adjustment calculation on source FPGA.

Figure 8.9: ECG measurement on source channels.

8.4 Calibration FPGA

Calibration FPGA can be seen as a simplified version of source FPGA where there is only a forward path for the current generation and a voltmeter. The block diagram of the calibration channel FPGAs is shown in Fig. 8.11. Since there is only one calibration board, the address of the calibration FPGA is set and is not variable. The floorplan and the resource utilization of the calibration channel are shown in Fig. 8.12
8.5 Summary

This chapter discussed the FPGAs and the inner structure of the controller, the source, and the calibration FPGAs. Next chapter overviews the safety features implemented in ACT5.
Figure 8.11: Block diagram of the calibration FPGA.

Figure 8.12: (a) Floorplan and (b) resource utilization on calibration FPGA.
CHAPTER 9
Safety Features

ACT5 employs various safety features to ensure that it does not pose any risk to the operator and subjects. These features can be categorized in the following classes: Physical safety, firmware safety, and the software safety.

9.1 Physical Safety Features

The first class of safety features are the general physical safety features that are employed to eliminate or limit possible hazards arising from the design of the system, especially introducing unwanted voltages and currents to the body. For this, ACT5 utilizes a medical power supply (NEVO+600M [94]) that isolates the system electrically and provides a first line of protection against hazards such as short circuits or noise on the supply voltages. Another potential path for electricity to ACT5 would be through its communication link to the PC. This path is broken by optically coupling the communication link so that the PC and ACT5 are not connected electrically. Other safety features in this category include employing a DC blocking capacitor at the output of each channel and limiting the possible current and voltage ranges to minimize any possible risk due to a failure in the system. These features are summarized in Table 9.1.

Table 9.1: Summary of hardware safety features

<table>
<thead>
<tr>
<th>Safety Feature</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>Medical safety standard approved</td>
</tr>
<tr>
<td>Optically decoupled UART link</td>
<td>Removes any possible electric connection to PC</td>
</tr>
<tr>
<td>Channel DC blocking capacitor</td>
<td>Blocks DC voltage on the patients</td>
</tr>
<tr>
<td>Limited voltage &amp; current</td>
<td>Minimize possible risk in case of failure</td>
</tr>
</tbody>
</table>
9.2 Firmware Safety Features

The second line of safety features are the ones that are implemented in the firmware. These features are related to hazards that can arise during operation and require an active intervention for them to be repelled and resolved. The cause of these hazards can be operator errors, electrode detachment due to movement of the patient, changes in the load, failure of electronic parts, or other similar actions. The firmware on the calibration board, the channels, and the controller have their own unique safety nets.

9.2.1 Calibration Board Firmware Safety

Since the calibration board acts as the virtual ground during data collection, it drains and measures any mismatched current applied to the body. The magnitude of the drained current is used to detect faults in the system. An overview of the safety check on the calibration board is shown in Fig. 9.1.

Figure 9.1: Safety check process on the calibration board firmware.

The calibration board checks three conditions on the ground current ($I_{\text{gnd}}$)

1. Comparing the ground current of imaging patterns to a maximum allowable current:
   For imaging patterns, the ground current is ideally zero. Hence, a maximum allowable ground current for imaging patterns ($I_{\text{max-image}}$) is set as the threshold where, if the ground current exceeds this value, it indicates a fault in the system, such as an electrode
detachment or a malfunction in a source. This test only considers ground current at the excitation frequency.

2. Comparing the broadband ground current of imaging patterns to maximum allowable broadband current: The calibration board accumulates the broadband ground current \(I_{\text{broadband}}\) for each of the bursts during the imaging patterns and compares it to a threshold of maximum allowable broadband current \(I_{\text{max-Broadband}}\) and a fault is detected if this threshold is exceeded. This test considers the case where an oscillation may occur.

3. Comparing the ground current of the zero-sequence pattern with minimum allowable current: In cases such as the ground electrode being detached, the ground current of the imaging patterns are still going to be close to zero, yet on the zero-sequence pattern (Section 11.2.2), the ground current is going to be smaller than expected. Hence, by setting a minimum threshold for the ground current during the zero-sequence pattern \(I_{\text{min-ZS}}\), we can detect if the ground electrode is still attached to the patient or not.

Upon detection of a fault, the calibration board raises the STOP signal on the backplane which is connected to all system boards. Upon receiving the STOP signal, the channels set their output to zero and open their load switch, which opens the connection to the cables and the patient. Note that in each of the three cases, the calibration board returns a unique code to the controller to indicate which fault has occurred.

<table>
<thead>
<tr>
<th>Fault check</th>
<th>Fault cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-zero current for Imaging patterns</td>
<td>Active electrode disconnected</td>
</tr>
<tr>
<td></td>
<td>Source malfunction</td>
</tr>
<tr>
<td>Large broadband current for Imaging patterns</td>
<td>Electronics malfunction</td>
</tr>
<tr>
<td></td>
<td>Environmental interference</td>
</tr>
<tr>
<td>Small current on zero-sequence pattern</td>
<td>Ground electrode disconnected</td>
</tr>
<tr>
<td></td>
<td>Secondary path to ground exists</td>
</tr>
</tbody>
</table>

9.2.2 Source Board Firmware Safety

The safety features in the firmware of the source boards is mostly concerned with the voltages seen by the source and detecting overflows on voltage. A voltage overflow can be
caused by either a high-impedance load, which can be due to the load itself or a loosely attached electrode, or high output current amplitude. Another possible way for a voltage overflow to occur is when the ground electrode is detached. When the ground electrode is detached, the residual current, although extremely small, is not drained to the ground, which can cause the overall average voltage to increase or decrease until the sources cease to operate properly. Specifically, the adaptive current sources become unstable and their voltages start fluctuating when the ground electrode is disconnected.

In any situation, in case of voltage overflow, the voltage samples received from the ADC will be \texttt{18'h3FFFF} when the voltage are above the maximum allowable voltage, and \texttt{18'h00000} when the voltage are below the minimum allowable voltage. Upon receiving either of these two values from the ADC, the channels flag their operation as faulty. If the overflow of voltage persists through multiple cycles, the channel will return (\texttt{24'h7FFFFF}, \texttt{24'h7FFFFF}) for the real and imaginary voltages back to controller, indicating the fault in their operation. Additionally, channels will halt their adaptive compensation for the shunt impedance module as that can cause instability in the applied current with erroneous voltages.

\textbf{9.2.3 Controller Firmware Safety}

The controller can only connect data from the sources and the calibration board, hence its safety features are dependent on the retrieved data from the peripheral devices. In case of receiving the \texttt{STOP} signal, the controller halts the imaging process. Additionally, the controller monitors the returned voltages from the channels and if multiple channels are facing overflow in their voltages or if a channel is facing overflow through multiple patterns, it will detect a fault and halts the imaging process.

Based on the type of the error that the controller detects, it will return specific commands at the EOF section of the data so that the PC knows the reason why the imaging was halted.
9.3 Software Safety Features

The returned data to the computer can reveal issues that are not necessarily hazardous, but can cause problems if they are not addressed. As an example, a loose electrode that introduces a series impedance on the channel might not cause the voltages to overflow during the burst, but this unwanted series impedance would still have adverse effect on the data and might also indicate if the electrode is more likely to become detached. Since neighboring electrodes have similar paths to the ground electrode, this series impedance can show up during the zero-sequence pattern where the loose electrode will have a higher voltage compared to its neighboring electrodes. ACT5 software monitors the induced voltages on the electrode and if the voltage on one electrode is significantly larger than its neighboring electrodes during the zero-sequence pattern, it will issue an alert on possible loose electrodes.

The software also provides stop, pause, and reset capabilities to the users. These features provide another layer of protection where the users can manually intervene the operation of ACT5 through the PC and either stop the imaging process and reset the system to make it ready to start over, or pause the imaging process and resume it immediately.

9.4 Summary

This chapter explained the safety features of ACT5, including the safety features at the physical level, safety features at the firmware level, and the safety features at the software level. The experimental results of ACT5 are presented in the next chapter.
CHAPTER 10
Experimental Results

This chapter covers some of the experimental results that have been acquired by ACT5. Performance of ACT5 can be evaluated with various criteria and in different aspects. Some of these criteria include the reconstructed images, the ECG measurements, ability to distinguish small changes in the impedance, SNR, and the ability to adapt current patterns.

10.1 Image Results

The main task of ACT5 is to apply currents, measure voltages, and reconstruct images based on the collected data. The capabilities of ACT5 for this purpose have been evaluated on a saline-filled tank and also on human subjects.

10.1.1 Tank Results

Performance of ACT5 was tested on a tank filled with saline as shown in Fig 10.1. The diameter of the tank is 30 cm and its height is 5 cm. There are 32 equally-spaced stainless steel electrodes around the tank. Each electrode has a height and width of 2.54 cm. The source channels are connected to the electrodes through a 1.5 m grounded-shielded cables. The tank is filled with saline where the depth of saline is approximately the same as the height of the electrodes. The virtual ground cable is inserted into the saline through a wire.

A series of objects are inserted into the saline while ACT5 is collecting data as shown in Fig. 10.2 to Fig. 10.7. A frame of data from the tank filled with homogeneous saline is used as the reference frame. The images are reconstructed by taking the difference between the voltages of each target configuration and the voltages of the reference frame. All the 2-D images are reconstructed using the NOSER algorithm [12]. NOSER reconstructs two images, a conductivity image where the conductance of the imaged medium is plotted, and a susceptance image, which is related to the capacitance, is shown. In Fig. 10.2 to Fig. 10.7 the photo image of the tank and the targets is on the left, the conductivity image is in the
middle, and the susceptance image is on the right side of the figures. Each reconstructed image has an associated Sigma value which provides the average conductivity or susceptance of the image. The unit of measurement for the Sigma is milli siemens per unit of length (mS/m), where siemens (S) can be written as $\Omega^{-1}$. At the same time, variations of the conductance and the susceptance are color coded, with the red color representing higher conductance or susceptance compared to the average and the blue color representing lower values. The maximum and minimum value of conductance and the susceptance with reference to the sigma are also displayed in each reconstructed image.

Figure 10.2 shows image of the saline-filled tank with no targets. The narrow range for the conductivity and the susceptance images show that the tank is homogeneous and there is minimal change between two frames of tank with only saline in it.

An insulator cylindrical target, with outer diameter of 33.3 mm, is inserted in saline as shown in Fig. 10.3, the target is clearly visible on the conductivity image, but it is hard to be recognized on the susceptance image due to very small capacitive characteristics of the insulator. Note that the conductivity of the target is lower than the conductivity of the saline which is shown in the reconstructed image with blue color.

A polished copper target, with outer diameter of 31.06 mm, is then placed in the
saline as shown in Fig. 10.4. The conductivity image shows the target distinctly, and the conductance of the target is shown to be higher than the saline. Some trace of the target can also be seen in the susceptance image, but since polishing the target has removed most of the oxide layer on its outer surface, the target has minimal capacitive properties.

To show the effectiveness of ACT5 in plotting the capacitive properties of the targets, an unpolished copper target, with outer diameter of 31.06 mm, is inserted in the saline as depicted in Fig. 10.5. The oxide layer on the outer surface of the target acts as a capacitance and, as a result, the target can be easily distinguished in both the conductivity, and the susceptance images.

Figures 10.6 and 10.7 show the three targets, including the insulator cylinder, the
polished copper cylinder, and the unpolished copper cylinder, in the tank simultaneously. It is notable that although the two copper targets might visually look similar, they can be differentiated from one another by checking the susceptance images. Another note is that the targets are defined more clearly when they are closer to electrodes. This is due to the fact that EIT systems have greater sensitivity to impedance changes closer to the electrodes as opposed to impedance changes closer to the middle of the saline tank.

10.1.2 Human Results

ACT5 is designed with the goal of monitoring the thorax region of body. For this purpose, electrodes can be mounted on the body in various configurations. Figure 10.8
shows two common ways that the electrodes are attached to the body where in Fig. 10.8a, 32 electrodes are connected around the body in one ring, and in Fig. 10.8b, 32 electrodes are mounted in two rings, with each ring having 16 electrodes. It is possible to have more rings of electrodes, or have more or fewer number of electrodes in a configuration. As an example if a subject has a thorax with smaller size, it is possible to use fewer than 32 electrodes in either 1 or 2 rings. On the other hand, it is possible to have 4 rings of electrodes with 12 electrodes at each ring with a 48 electrode system.

The main difference between the electrode placement configuration is the type of image that it yields. Attaching the electrodes in one ring yields a 2-D image of the chest, while
having more than one ring of electrodes gives us information about the 3-D properties of the thorax. Additionally, The reconstruction algorithm for the 2-D and the 3-D cases differs where the 2-D EIT images in ACT5 are reconstructed with the NOSER algorithm \[12\], while the 3-D images are reconstructed using the ToDLeR algorithm \[23, 24\].

Some results of the 3-D image reconstruction is provided in this section. EIT data was collected in accordance with the amended Declaration of Helsinki–Ethical Principles for Medical Research Involving Human Subjects under the approval of the Colorado State University Institutional Review Board (approval number 2943) with informed written consent.

3-D images obtained by ACT5 using two rings of 16 electrodes are shown in Fig. 10.9. Each ring of electrode can be considered as a plane, yielding two parallel planes inside the body. The ToDLeR algorithm uses the data from all electrodes to reconstruct two sets of images, one at each plane created by the electrode rings, and these two sets of images can be considered as a 3-D image. The view of the images is from top of the subjects as shown in Fig. 10.9. Figure 10.9 also depicts the approximate location of the heart and lungs and shows that which images align with which rings of electrodes.
Figure 10.9: Sample of a 3-D reconstructed image using ToDLer. Each pair of conductive and susceptance image represent one ring of electrodes. approximate location of lungs and heart is indicated in the images.

Figure 10.10 shows 3-D reconstructed images of thorax during a normal breathing session. The traces on top of the image show the average conductance of the image which translates to pattern of breathing by the subject. Local maximums of the traces show the state of maximum conductance, which means that the lungs are empty, and the local minimums of the traces show the state of minimum conductance, which means that the lungs are filled with air. The images in Fig. 10.10 show the thorax when the subject is inspiring. The images initially show the lungs in a state with no air in them (red - conductive) and show consecutive images of air moving into the lungs (increasingly blue - less conductive).

Figure 10.11 shows a sequence of images of heart-related activity. For this experiment, subject is holding their breath, so that the impedance changes are mostly related to changes in blood volume in the body. The EIT images are accompanied by ECG measurements which show exactly where each image is relative to the cardiac cycle. Image 1 shows that the heart region is red and the rest of the thorax is blue, meaning that there is more blood in the heart and less blood in the rest of the thorax. In the next images, it can be seen that the heart region turns less red to even blue in image 4 and the rest of the thorax region are turning red, indicating that blood has moved from the heart to the lungs and other organs. From images 5 to 8, the process is reversed where the heart becomes more conductive, i.e.
Figure 10.10: Sequence of 3-D EIT images of human subject breathing normally. Changes in the impedance are dominated by air flow in the lungs.
there is more blood in the heart, and the rest of the thorax turn blue, indicating that the
blood is moving back to the heart, ready for the next cycle to be pushed out.

10.2   ECG Results

To show the performance of the ECG measurement system in the ACT5 system, the
following scenarios are considered:

- ECG data when EIT is inactive (no EIT current is applied)
  - Raw ECG
  - Filtered ECG
- ECG data when EIT is active
  - Raw ECG
  - Filtered ECG

The electrodes are attached to the body in the two-rings with 16 electrodes in each ring as
described in Section 10.1.2. All of the electrodes collect individual ECG recordings. The
ECG recordings are averaged to build a reference signal of Wilson’s central terminal [95]. The
reference is then subtracted from the signal from each electrode to produce the individual
ECG signals.

10.2.1   ECG Data with Inactive EIT

Figure 10.12 shows the raw ECG recording of all electrodes when no EIT signal is
applied. The ECG recordings are plotted so that the electrodes on the top ring of electrodes
and the bottom ring of electrodes that are closer together are plotted side-by-side, i.e. elec-
trode 1 and 17 are plotted next to each other since they are vertically mounted on the body
one above the other. It can be seen in Fig. 10.12 that some of the signals are noisy, but the
recordings are such that the heart activity is clear. The raw ECG recordings are then filtered
by using a notch filter at 60 Hz and a low-pass filter with a cut-off frequency of 40 Hz. The
filtered ECG data is shown in Fig. 10.13. It can be seen that the noise is suppressed and
Figure 10.11: Sequence of 3-D EIT images of human subject holding their breath. Simultaneous ECG measurement is plotted to match the EIT images with heart cycle.
the ECG signal is more defined. These figures show the quality and capability of ACT5 to record ECG signals.

Figure 10.12: Raw ECG data from all channels where no EIT signal is applied.

10.2.2 ECG Data with Active EIT

The ECG signal is significantly affected when the EIT signal is applied, as shown in Fig. 10.14. This shows that with active EIT, the ECG signals are distorted to a degree that the raw recordings are not useful in determining the cardiac cycle. Because of this, ECG
signal is filtered by using a notch filter at 60 Hz, a low-pass filter with a cut-off frequency of 40 Hz, and a series of notch filters at the frame rate (27 Hz) and its higher-order harmonics. The results are shown in Fig. 10.15 where the ECG signal is clear and the cardiac cycle can clearly be seen. The results show that although raw ECG recordings of ACT5 with active EIT are dominated by interference from the EIT signals, the interference signal can be suppressed with proper filtering of the data, enabling ACT5 to obtain good quality ECG signals while it applies EIT signals.

Figure 10.13: Filtered ECG data from all channels where no EIT signal is applied.
10.3 Distinguishability Results

To analyze the capability of ACT5 to distinguish small changes in the impedance, small targets were either inserted in or removed from the tank and the EIT measurements are analyzed. The used targets were cylindrical metal objects (drill bits) with diameters of 4.7625 mm, 3.5719 mm, 2.7781 mm, and 1.5875 mm. The targets are shown in Fig. 10.16. The experiments were done with excitation frequencies of 23 437.5 Hz, 93 750 Hz, 140 625 Hz, and 199 218.75 Hz. A set of experiments were done with the targets at the center of the tank,
and a second set of experiments were done with the two smaller targets off the center of the tank.

10.3.1 Target at the Center of Tank

First set of experiments for distinguishability of small changes in the impedance was done by placing the targets in the middle of the tank as shown in Fig. 10.17 and imaging the impedance change using the trigonometric patterns.
For the experiments with the three bigger targets, a series of measurements were taken with the target initially in the tank and at some point the target was removed from the saline. The sequence was reversed for the smallest target. Since inserting and removing the objects in and out of the saline causes ripples on the surface, and the ripples cause impedance changes in the medium, each measurement session lasted for about one minute (1500 frames) where the object is inserted in or removed from the saline at approximately 15 seconds after the beginning of the measurement session. Plots shown in Fig. 10.18 to Fig. 10.21 show the change of average admittance of the tank during the first 1000 frames of the distinguishability test. As it can be seen in Fig. 10.18, Fig. 10.19 and Fig. 10.20 the admittance drops after the target is removed from the tank. Figure 10.21 shows that the admittance increases after the smallest target is inserted in the tank. It is clear that the change in the admittance is smaller with the smaller targets compared to the larger targets. Another observation from these figures is that, especially for the larger targets, the ripples on the surface of the saline caused by removing the object are visible on the admittance trace. These ripples dampen down in time, and by the end of the measurement, the effects
of the ripples are no longer noticeable.

Although the changes in admittance are visible in the admittance trace, the norm distinguishability and power distinguishability (introduced in Section 2.3.2.1) are calculated for each configuration using the average of the first 100 frames and the average of the last 100 frames. Figure 10.22 plots the norm distinguishability for each pattern of applied current. Each plot in the figure represents the experiments done with the four targets at one frequency. The plots show that patterns with the lowest spatial frequency (patterns 1, 2, 17, and 18) have the highest distinguishabilities and the distinguishability falls for the rest of the patterns. Figure 10.23 plots the power distinguishability for each pattern for all targets at different frequencies. It can be seen that similar to norm distinguishability, patterns 1 and 17 have the highest amount of information compared to other patterns.

Figure 10.24 plots the norm distinguishability for each pattern of applied current where each plot represents the experiments done with one of the targets at the four different frequencies. The plots show that for the larger targets, the distinguishability factor does not vary significantly for different frequencies of operation while, for the smaller targets, lower frequencies of operation yields smaller distinguishability. Figure 10.25 show the similar configuration for power distinguishability.

Finally, Fig. 10.26 plots the norm distinguishability versus the size of the objects for
different patterns. Each plot depicts the distinguishability factor of the 31 applied patterns at a given frequency. The plots show a general linear decrease in the distinguishability when the size of the target is decreased. The result for the smallest target is close to the region where the distinguishability falls to 0, i.e. where the system no longer distinguish objects when they are placed in the tank. The power distinguishability for the same configuration is shown in Fig. 10.27.

10.3.2 Target off the Center of Tank

The second test for distinguishability is when the two smaller targets with size of 2.7781 mm and 1.5875 mm were place in or removed from off the center of the circular saline tank as shown in Fig. 10.28.

The traces of the average admittance during the experiment is shown in Fig. 10.29 and Fig. 10.30. Similar to the experiment where the targets where at the center of the tank, the change in the average admittance is visually noticeable when the target is removed from or inserted in the tank.

Figure 10.31 and Fig. 10.32 show the norm and power distinguishability for each pattern at set frequencies. It can be seen that since the target is off center, more patterns have
Figure 10.20: Admittance trace of removing a cylindrical object with diameter of 2.7781 mm from center of the saline tank.

(a) Frequency = 23 437.5 Hz  
(b) Frequency = 93 750 Hz  
(c) Frequency = 140 625 Hz  
(d) Frequency = 199 218.75 Hz

Figure 10.21: Admittance trace of inserting a cylindrical object with diameter of 1.5875 mm in the center of the saline tank.

(a) Frequency = 23 437.5 Hz  
(b) Frequency = 93 750 Hz  
(c) Frequency = 140 625 Hz  
(d) Frequency = 199 218.75 Hz
Figure 10.22: Comparison of norm distinguishability of targets with various size at the center of the tank for each pattern with constant frequency of operation.

Figure 10.23: Comparison of power distinguishability of targets with various size at the center of the tank for each pattern with constant frequency of operation.
Figure 10.24: Comparison of norm distinguishability of targets at the center of the tank with various frequencies of operation for each pattern with constant diameter of target.

Figure 10.25: Comparison of power distinguishability of targets at the center of the tank with various frequencies of operation for each pattern with constant diameter of target.
Figure 10.26: Comparison of norm distinguishability against different size of target at the center of the tank for the imaging current patterns with constant frequency.

Figure 10.27: Comparison of power distinguishability against different size of target at the center of the tank for the imaging current patterns with constant frequency.
information related to the object in the tank compared to the case where the targets were put at the center of the tank.

Figures 10.33 and 10.34 show the norm and power distinguishability for all patterns for each object under the four frequencies of operation. Again, it can be observed that more patterns than just pattern 1 and 17 provide distinguishability for off-center targets.

10.4 Adaptive Current Patterns Results

ACT5 has the ability to apply any valid current pattern to an object. This means that ACT5 can apply current patterns that would yield maximum amount of information (maximize the distinguishability). To demonstrate this ability of ACT5, optimal current patterns for the tank shown in Fig. 10.35 were created through the iterative process introduced in Section 3.1.3.

The process for finding the optimal current patterns starts with applying the trigonometric patterns to the box, and measuring the voltages. The applied currents and the measured voltages for the 31 imaging patterns are shown in Fig. 10.36, where the amplitude of both the current patterns and the measured voltages is normalized to 1. As it can be seen from the figure, the applied voltages are not proportional to the applied current, meaning
that the trigonometric patterns are not optimal for imaging the box tank.

Figure 10.37 shows the applied current and the measured voltages where the applied current are calculated by executing one iteration of the process to find the optimal current patterns. It can be seen that the applied currents no longer look like the trigonometric current patterns, and at the same time the voltages and the currents match each other when they are normalized to 1, so that they are indistinguishable from one another on the plot.

10.5 Summary

This chapter presented the experimental results of ACT5. The results included experiments done on saline tanks and experiments with human subjects. Tank experiments included 2-D image reconstruction, capability of ACT5 to distinguish small changes in impedance, and its ability to apply optimal current patterns. Human results included 3-D image reconstruction of lung and heart activity and ECG recording from all electrodes. Next chapter introduces novel shunt impedance measurement technique that is used in ACT5.
(a) Frequency = 23 437.5 Hz
(b) Frequency = 93 750 Hz
(c) Frequency = 140 625 Hz
(d) Frequency = 199 218.75 Hz

Figure 10.30: Admittance trace of inserting a cylindrical object with diameter of 1.5875 mm off the center of the saline tank.

Figure 10.31: Comparison of norm distinguishability of targets with various size off the center of the tank for each pattern with constant frequency of operation.
Figure 10.32: Comparison of power distinguishability of targets with various size off the center of the tank for each pattern with constant frequency of operation.

Figure 10.33: Comparison of norm distinguishability of targets off the center of the tank with various frequencies of operation for each pattern with constant diameter of target.

Figure 10.34: Comparison of power distinguishability of targets off the center of the tank with various frequencies of operation for each pattern with constant diameter of target.
Figure 10.35: Image of the tank used in the adaptive current patterns study.
Figure 10.36: Applying trigonometric current patterns to the box tank. The x axis for each pattern is electrode number and y axis is the amplitude for the current and the voltage scaled to unity. The current is in blue and the scaled voltages are red.
Figure 10.37: Matching scaled applied current and scaled measured voltages after one iteration of process of finding optimal current patterns for box tank.
Shunt impedance on the current sources, as mentioned in Section 2.1, affects the performance of the EIT systems by causing the current being delivered to the body to not be equal to the intended current that is supposed to be delivered. ACT5 adaptive current sources negate the effects of shunt impedance by supplying an extra current that is equivalent to the current lost on the output impedance of the current sources. This extra current is directly calculated by taking the real-time output voltage of the source and dividing it by the value of shunt impedance. Accurate values of shunt impedance are essential for that the compensation method to work effectively, making the task of finding the shunt impedance a vital task for proper operation.

The shunt impedances on the current sources of ACT5 are roughly known at the design time as shown in Fig. 6.9. The shunt impedance can be broken down to parallel resistive and capacitive portions. The resistive part is set to be 100 kΩ in parallel with the output impedance of the Howland current drive and the input impedance of the voltage buffer. The capacitive part of the shunt impedance also consists of the output capacitance of the Howland current source and the input capacitance of the voltage buffer, in parallel with the capacitance introduced by cables. The cable capacitance is the dominant part of the shunt capacitance and its value depends on the length and the type of the cable connected to the output of the source. For a single-shielded cable with grounded shield, the capacitive part of the shunt impedance is approximately 100 pF per each meter, which translates to impedance values of approximately 21 kΩ at 5 kHz to 1 kΩ at 1 MHz for a 1.5-meter cable.

These approximate values are not accurate since they do not take multiple variable factors into account. Factors such as the temperature, position of the cables, position of the source on the board, the traces on the PCB, and the tolerance of the components on the boards are all variables that might affect the impedance to the degree that it will degrade the quality of reconstructed images [83]. Additionally, ACT5 is designed so that the attached cables can be changed depending on the application, whether it is a change in the length...
or a change in the type of the cable. This means that variations on the shunt impedance values of current sources, whether small or significant, are inevitable and requires frequent measurement to ensure their stability.

ACT5 utilizes two different methods for measuring the parallel impedance values on channels. The first method is the open-circuit (OC) method that is done during the calibration process introduced in Section [6.4.3] The second method is a novel technique that continuously measures the impedance values during the imaging operation by adding an extra current pattern and monitoring the current on the ground electrode. This chapter first discusses about how the OC impedance measurements can be improved, and then introduces the novel continuous shunt impedance measurement.

11.1 Improved Open-Circuit Measurements

The basic OC impedance measurement does not take the crosstalk between the cables into account. Consequently it can be improved if channels are not considered independent of each other. To measure the crosstalk between the cables, we have to define and find the admittance network of a fully-connected impedance graph of all electrodes.

11.1.1 Equivalent Fully-Connected Admittance Network

To find the impact of crosstalk, we start by assuming that the impedance network between the cables is a fully-connected network. A sample network for a 4-electrode system is shown in Fig. [11.1] where the four current sources have a parallel impedance to the ground and they are all connected to each other, where this connection can be either through the body or coupling through the air. In cases where the electrode is connected to the body, there is an extra ground route through the body for each electrode.

An equivalent admittance matrix can be written for this network as shown in (11.1)
Figure 11.1: Fully-connected model of body in an EIT system with four active electrodes. © 2020 IEEE

\[
G = \begin{bmatrix}
G_{o1} + G_{10} + \sum G_{1i} & -G_{12} & \ldots & -G_{1N} \\
-G_{21} & G_{o2} + G_{20} + \sum G_{2i} & \ldots & -G_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
-G_{N1} & -G_{N2} & \ldots & G_{oN} + G_{N0} + \sum G_{Ni}
\end{bmatrix}
\] (11.1)

where \(G_{oi}\) is the shunt admittance of the \(i\)th electrode to the ground, \(G_{ij}\) the admittance from the electrode to the ground through the body and \(G_{ij}\) is the admittance value between the \(i\)th and the \(j\)th electrode.

11.1.2 Measuring the Admittance Matrix

The admittance matrix in (11.1) is unknown, yet it can be calculated through experimental measurements. For this, we use the admittance matrix to relate the injected currents and the induced voltages for a given pattern to each other as

\[
\begin{bmatrix}
I_1 \\
I_2 \\
\vdots \\
I_N
\end{bmatrix} = G \cdot \begin{bmatrix}
V_1 \\
V_2 \\
\vdots \\
V_N
\end{bmatrix}
\] (11.2)
where $I_i$ is the current injected from the $i$th electrode, and $V_i$ is the voltage induced on the $i$th electrode. By using a set of $N$ linearly independent current patterns, we can extend the current and the voltage vectors into current and voltage matrices

$$\begin{bmatrix}
I^1_1 & I^2_1 & \ldots & I^N_1 \\
I^1_2 & I^2_2 & \ldots & I^N_2 \\
\vdots & \vdots & \ddots & \vdots \\
I^1_N & I^2_N & \ldots & I^N_N \\
\end{bmatrix} = \mathbf{G} \cdot \begin{bmatrix}
V^1_1 & V^2_1 & \ldots & V^N_1 \\
V^1_2 & V^2_2 & \ldots & V^N_2 \\
\vdots & \vdots & \ddots & \vdots \\
V^1_N & V^2_N & \ldots & V^N_N \\
\end{bmatrix}. \quad (11.3)$$

where $I^j_i$ is the current injected from the $i$th electrode at $j$th pattern, and $V^j_i$ is the voltage on the $i$th electrode at $j$th pattern. Note that the current patterns can be as simple as an identity matrix where only one current source is active at a time

$$\mathbf{I} = \begin{bmatrix}
1 & 0 & \ldots & 0 \\
0 & 1 & \ldots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
0 & 0 & \ldots & 1 \\
\end{bmatrix}. \quad (11.4)$$

By using (11.3), the admittance matrix can be calculated by multiplying the inverse of the voltage matrix to both sides

$$\mathbf{G} = \mathbf{I} \cdot \mathbf{V}^{-1} \quad (11.5)$$

11.1.3 OC Shunt impedance and Crosstalk

The elements in the admittance matrix can be categorized as two types of (i) admittance to ground, and (ii) admittance between two electrodes. Hence, the admittance matrix can be separated to two different matrices, one to show the admittance matrix to the ground, and one to show the admittance matrix between the electrodes.

To extract the ground admittance matrix, we can sum the rows of the admittance matrix which will yield a vector of admittance values to ground for each electrode.
This vector can then be converted to a diagonal matrix which yields the ground admittance matrix \( \mathbf{G}_{\text{gnd}} \)

\[
\mathbf{G}_{\text{gnd}} = \begin{bmatrix}
G_{o_1} + G_{10} & 0 & \ldots & 0 \\
0 & G_{o_2} + G_{20} & \ldots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
0 & 0 & \ldots & G_{o_N} + G_{N0}
\end{bmatrix}.
\]  

Note that under the OC configuration, we will have \( G_{i0} = 0 \) for all channels. This means that diagonal elements of \( \mathbf{G}_{\text{gnd}} \) can be used as the shunt impedance values of channels.

The second matrix, which represents the admittance present between each pair of electrode in the network, is calculated by subtracting the ground admittance network from the admittance network

\[
\mathbf{G}_{\text{pair}} = \mathbf{G} - \mathbf{G}_{\text{gnd}} = \begin{bmatrix}
\sum G_{1i} & -G_{12} & \ldots & -G_{1N} \\
-G_{21} & \sum G_{2i} & \ldots & -G_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
-G_{N1} & -G_{N2} & \ldots & \sum G_{Ni}
\end{bmatrix}.
\]  

We can infer that \( \mathbf{G}_{\text{pair}} \) represents the crosstalk between the channels, and hence can be used to remove the artifacts related to channel crosstalk from the data.

11.1.4 Disadvantages of OC impedance

Measuring the shunt impedance values with OC measurements has some disadvantages. Due to the high shunt impedance values on channels, specifically at lower frequencies of operation, the magnitude of applied current must be small, causing a small signal-to-noise ratio for the voltages. To suppress the noise, we need to average a high number of voltage

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measurements, meaning that the time spent on the OC measurement can become large.

The other disadvantage of OC measurement of shunt impedance is the need to detach the cables from the electrodes. This means that in long-term monitoring applications of EIT, if the impedance values change during the time of the imaging operation, the system must not only halt the operation but also the cables must be physically detached from the electrodes in order for the system to be able to remeasure the shunt impedance values.

11.2 Continuous Shunt Impedance Measurement

ACT5 utilizes a novel shunt impedance measurement technique that can operate at the time of the imaging process. This technique requires (i) adding an extra pattern to the imaging patterns, and (ii) monitoring the current passing thorough the ground electrode. By this, a set of linear equations emerge where its solution are the shunt impedance values. Ground electrode current measurement is implemented in ACT5 for safety purposes and does not introduce any additional overhead. The extra current pattern is added to the system with minimal overhead.

11.2.1 Ground Electrode Current

For any given pattern, the current on the ground electrode can be written as the sum of the current injected through the active electrodes into the body as shown in (11.9)

\[ S = I_{L1} + I_{L2} + \ldots + I_{LN} = \sum_{i=1}^{N} I_{Li} \]  

(11.9)

where \( S \) is the current on the ground electrode (or current sum), \( I_{Li} \) is the current injected to the body through the \( i \)th electrode, and \( N \) is the number of electrodes.

For the model of shunt impedance shown in (11.2) the current injected to the body through an electrode is related to the current generated by the current source, the voltage induced on the electrode, and the shunt impedance that is on the output of the current source as shown in (11.10)
\[ I_L = I_{S_i} - I_{Z_{o_i}} = I_{S_i} - \frac{V_i}{Z_{o_i}} = I_{S_i} - V_i.G_{o_i} \quad \text{for } i = 1, 2, \ldots, N \]  \hspace{1cm} (11.10)

where \( I_{S_i} \) is the current generated on the \( i \)th current source, \( I_{Z_{o_i}} \) is the current that passes through the shunt impedance on the \( i \)th current source, and \( Z_{o_i} \) (\( G_{o_i} \)) is the shunt impedance (admittance) value on the \( i \)th current source. Note that the circuit in Fig. 11.2 is a simplified model of the ACT5 circuits, yet this work is valid with the more complicated circuit model of ACT5. Combining (11.9) and (11.10) will yield

\[ S = \sum_{i=1}^{N} I_{S_i} - V_i.G_{o_i} \]  \hspace{1cm} (11.11)

which can be rewritten as

\[
\begin{bmatrix}
-V_1 & \cdots & -V_N \\
\vdots & \ddots & \vdots \\
G_{o_1} & \cdots & G_{o_N}
\end{bmatrix}
= S - \sum I_{S_i}. \hspace{1cm} (11.12)
\]

Expression (11.12) can be expanded for all \( N - 1 \) patterns
\[
\begin{bmatrix}
-V_1^i & \ldots & -V_N^i \\
\vdots & \ddots & \vdots \\
-V_1^{N-1} & \ldots & -V_N^{N-1}
\end{bmatrix}
\begin{bmatrix}
G_{o1} \\
\vdots \\
G_{oN}
\end{bmatrix}
= \begin{bmatrix}
S^1 - \sum I_{S_i}^1 \\
\vdots \\
S^{N-1} - \sum I_{S_i}^{N-1}
\end{bmatrix}
\] (11.13)

where \(V_i^j\) is the voltage on the \(i\)th current source on \(j\)th current pattern, \(S_i\) is the current on the ground electrode during the \(j\)th current pattern, and \(I_{S_i}^j\) is the current of the \(i\)th source during the \(j\)th current pattern. Voltages and the ground electrode current are measured during the imaging operation and the current source outputs are set prior to the operation. The unknowns in (11.13) are the output admittance values and the problem to find them is that the count of the patterns used for taking images does not equal the number of electrodes, meaning that the number of equations are fewer than the number of unknowns.

### 11.2.2 Zero-Sequence Pattern

To be able to calculate the shunt admittance values, an extra current pattern needs to be added to the existing patterns. As the patterns used for the imaging process fundamentally sum up to zero, any current pattern that does not sum up to zero can be used as the extra pattern. ACT5 uses a zero-sequence pattern where all the sources apply a current with the same phase and amplitude as the \(N\)th current pattern. An example pattern for a four-electrode system is shown in (11.14) where each row represents a current pattern. The first three patterns are the imaging patterns and sum up to zero, and the last pattern is the zero-sequence pattern where all the electrodes apply the same current. Note that the amplitude of current on a single source for the zero-sequence pattern is lower than the imaging patterns. The reason for this is that since all the current of zero-sequence pattern is drained through the virtual ground, lowering the amplitude of current on each electrode would help to keep the current density on the virtual ground low.

\[
\text{Pattern} = \begin{bmatrix}
0 & -1 & 0 & 1 \\
1 & -1 & 1 & -1 \\
-1 & 0 & 1 & 0 \\
\frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4}
\end{bmatrix}
\] (11.14)
11.2.2.1 Calculating Shunt Admittance

By adding the zero-sequence pattern to the system of equations in (11.13), we will have

\[
\begin{bmatrix}
-V_1^1 & \ldots & -V_N^1 \\
\vdots & \ddots & \vdots \\
-V_1^N & \ldots & -V_N^N
\end{bmatrix}
\begin{bmatrix}
G_{o_1} \\
\vdots \\
G_{o_N}
\end{bmatrix}
= \begin{bmatrix}
S^1 - \sum I_1^1 \\
\vdots \\
S^N - \sum I_N^N
\end{bmatrix}
\] (11.15)

which can be solved by calculating the inverse of the negative of the voltage matrix and multiplying it to both sides of the expression

\[
\begin{bmatrix}
G_{o_1} \\
\vdots \\
G_{o_N}
\end{bmatrix}
= \begin{bmatrix}
-V_1^1 & \ldots & -V_N^1 \\
\vdots & \ddots & \vdots \\
-V_1^N & \ldots & -V_N^N
\end{bmatrix}^{-1}
\begin{bmatrix}
S^1 - \sum I_1^1 \\
\vdots \\
S^N - \sum I_N^N
\end{bmatrix}.
\] (11.16)

11.3 Results

This section, discusses the results of the experiments.
11.3.1 Impedance Measurements

The first step to demonstrate the feasibility of the proposed method is to validate impedance measurement values. The measured values for the impedance are shown in Fig. [11.4] where Fig. [11.4a] shows the shunt resistance and Fig. [11.4b] plots the shunt capacitance. In parallel they form the output impedance for each current source. Note that at the frequency of operation, the capacitance has a more significant impact on the magnitude of the shunt output impedance. It can be seen that the OC and adaptive impedance are in the same range, yet the results of the two methods are not identical. It is likely that the adaptive results are more varied due to interaction between the output impedances associated with nearby electrodes. Current from one source can flow into the output impedance of another source through the conductive saline that connects the electrodes, though the algorithm will assign that current flow to the source output impedance.

11.3.2 Reconstructed Images

Reconstructed difference images for the case with multiple targets (Fig. [11.3a]) is shown in Fig. [11.5]. The images are created using the NOSER algorithm [12] and subtracting the
saline only image from the target image. The left and right images are the conductivity and susceptibility, respectively. The two upper targets are copper pipes, with the one on the left having a thin layer of oxide that creates a capacitive component observable in the susceptibility image. The lower target is PVC pipe. The images are formed by averaging voltages from 1000 frames. Fig. 11.5a shows the result using the OC impedances and Fig. 11.5b show the result using the adaptive impedances. The sets of images are nearly identical.

11.3.3 Ground Current

The ground current under the two configurations of OC impedance and the Adaptive impedance is shown in Fig. 11.6. The results show that for all patterns of current, virtual ground current is lower when the sources are operating with the adaptive impedance as opposed to them operating with the OC impedance.

11.3.4 Distinguishability

The distinguishability measures for the small target of Fig. 11.3b were computed with adaptive and OC output impedances and their ratios are plotted in Fig. 11.7. The results show that in all but 2 current patterns - the ones for the lowest spatial frequency cosine and sine - the adaptive impedance configuration has higher norm distinguishability and power distinguishability compared to the OC impedance configuration. These higher distinguishabilities point to the adaptive output impedances providing somewhat improved performance.

11.4 Summary

This chapter introduced the techniques that ACT5 uses for improved measurement of shunt impedance values on the channels, including a novel method that measures the shunt impedance while the system is attached to the load. Next chapter lists the contributions of this work to the ACT5 EIT system, provides a list of publications related to this project, and discusses possible future work for ACT5.
Figure 11.5: Reconstructed Image of three targets in tank under (a) OC impedance, and (b) adaptive impedance configurations. © 2021 IEEE
Figure 11.6: Amplitude of mismatched current collected through the virtual ground under the two operation configurations of (i) OC impedance and (ii) adaptive impedance. © 2021 IEEE

Figure 11.7: Relative (a) norm distinguishability, and (b) power distinguishability of collected data. © 2021 IEEE
CHAPTER 12
Contributions & Future Work

This chapter summarizes the contributions of this work on ACT5 and provides a list of publications related to the ACT5 EIT system.

12.1 Contributions

ACT5 is a complex system that properly operates when every component is working in harmony with the rest of the system. The components of ACT5 can be broken down to general categories of analog components, digital components, and the image reconstruction process. The primary contributions of this work are related to the design and implementation of the digital components of the system. These contributions can be listed as:

- Developing a custom UART module for communication between the controller and the PC with transfer rate of up to 6 Mbit s\(^{-1}\).
- Developing the backplane communications protocol using four parallel SPI channels with dual data lines.
  - Implementing the protocol in the controller and channel FPGAs to produce an overall internal transfer rate of up to 96 Mbit s\(^{-1}\).
  - Support of arbitrary number of channel boards of up to 12 boards (48 channels).
- Design, implementation, and optimization of fully-programmable channel firmware.
  - Digital compensation of lost current on output shunt impedance.
  - Capable of applying any sequence of current patterns.
- Design and implementation of the controller firmware.
  - Automation and speed-up of tasks.
  - Synchronization of system.
• Design, implementation, and optimization of a various MATLAB routines and applications.
  – Design and implementation of calibration routines.
  – Design and implementation of debugging routines.
  – Design and implementation of pattern-setup routines.
  – Design and implementation of data processing routines for received data from ACT5.
  – Optimization of image reconstruction routines.
  – Implementation of a developer GUI.
  – Partial implementation of a clinical GUI.

• Design and implementation of a novel shunt impedance measurement technique for EIT systems.

• Design and implementation of safety features on firmware and software levels.

• Extensive testing and troubleshooting of ACT5 EIT system.

12.2 Publications

List of the publications related to the ACT5 EIT system is as follows:


12.3 Future Work

ACT5, at its current state, meets all the requirements for an EIT system. It has been extensively tested in the lab environment on both saline tanks and human subjects with satisfactory results, yet it can be improved upon on multiple aspects.

12.3.1 Smooth Transition of Excitation Signals

Currently the patterns are applied sequentially as sinusoidal bursts and, for the time between the bursts, the channels are set to apply zero current to their output. Although the bursts are set to be cosine waves that start and end with a zero slope, due to existence of capacitance on the load and noise in the system, ensuring that the burst end with a zero derivative is not possible. This will introduce a charge on the DC-blocking capacitance which, due to the existence of a parallel resistor to the capacitance, will be discharged through
time. Despite this, this charge and discharge of the DC-blocking capacitance is undesirable and can cause unpredictable behavior, including the noise that is observable on the ECG measurements.

One way to address this issue is to not end the current at the end of the burst. The applied current can be set such that the transition between the signals is done in a way that the current output is not set to zero and instead its amplitude is transitioned smoothly to the amplitude of the next burst. For example, Fig. 12.1 shows transition of a signal amplitude changing from +1 to +0.25 under the current configuration and under the proposed configuration which transitions the signal without setting it to zero.

![Figure 12.1: Current transition of current (top) vs. the proposed smooth transition of current (bottom)](image)

12.3.2 Spectroscopy

ACT5 is capable to change the frequency of the excitation signal without any overhead in hardware or time. Applying signals in different frequencies provides an spectroscopic view of the impedance. ACT5 has the potential to be an effective spectroscopy tool by interleaving signals with different frequencies with each other in a frame. The only downside of this update is that, if all the excitation patterns for each excitation frequency are applied,
the frame rate will drop.

12.3.3 Using Data from Previous Frames

When applying a current, the adaptive current patterns start the burst by assuming the voltage on the load to be 0 V and adapt the current as they update their voltage measurement. This process can be improved by keeping a record of the voltage from the previous frame and starting the burst by assuming the voltage is going to be similar to the value it held during the same pattern at previous frame.

12.3.4 Computation on the Controller

The controller FPGA is responsible for data transmission and collection, automation of tasks, and monitoring the safety issues in the system. The controller FPGA can take on more responsibilities by doing low-level computation such as converting digital values of voltages to their physical values before transmitting them to the PC, or more sophisticated computations such as measuring optimal current patterns and updating them at the time of the imaging process.

12.3.5 Replacing FPGA Modules

All the previous suggested future work for ACT5 can be done by updating the firmware. A major upgrade the would require updating the design of PCBs of ACT5 is to replace the current FPGA modules with standalone FPGA chips. This change would reduce the size of the PCBs and make the size of the system smaller too. This change is specifically important if more copies of ACT5 are to be built as the reduced cost of the production would be significant.

12.3.6 Other Minor Changes

Some other possible minor changes to ACT5 include measuring the temperature on FPGAs, adding physical lights for safety, adding physical reset and stop buttons, and increasing the communication speed between the PC and the controller.
12.4 Summary

This chapter provided a list of contributions of this work and the publications related to ACT5. It also listed possible improvements that can be implemented on ACT5. Next chapter will provide the concluding remarks for this dissertation.
CHAPTER 13

Conclusions

In this document, the ACT5 EIT system is introduced. ACT5 is a multiple-source applied-current EIT system, designed mainly for monitoring the thorax region of human subjects. ACT5 can deploy arbitrary number of electrodes of up to 48 electrodes and is capable of acquiring images at a frame rate of 30 frames/sec when operating with 32 electrodes. The frequency range of excitation signals for ACT5 is from 5 kHz to 1 MHz and the signals have a maximum peak of 1 mA on each electrode. The channels dedicated to each electrode are equipped with high-accuracy voltmeters and Howland current pumps that are controlled digitally by an FPGA.

ACT5 incorporates numerous novel design ideas, including calibration techniques that automate the calibration of channels and minimizes need of user intervention, adaptive current sources that digitally provide high effective output impedance and eliminate multiple analog circuits used in conventional EIT systems, and the ability to adapt the current patterns based on the shape and the impedance distribution of the body. Additionally, ACT5 collects ECG recordings from all the channels during the imaging operation, providing an opportunity to match the EIT images with the cardiac cycles. A novel shunt impedance measurement technique is also implemented in ACT5 that monitors the shunt impedance on the sources and detects any change on them. The continuous shunt impedance measurement, in addition to other features such as adaptive measurement of DC on channels and the ability of ACT5 to recalibrate itself while it is attached to the load, make ACT5 a suitable EIT system for long-term monitoring purposes.

The design of ACT5 also ensures the safety of the patient. Multiple layers of safety, in hardware, firmware, and software, are placed so that they either prevent, or intervene and eliminate electrical hazard to patients. For controlling ACT5 a clinical GUI and a developer GUI are developed where the clinical GUI is an easy-to-use application that provides high-level control to clinical technicians, and the developer GUI provides low-level control that is useful for calibration and debugging purposes.
Performance of the ACT5 system is tested on both saline tank and human subjects. Circular saline tank experiments include image reconstruction of the tank with large targets in the tank, and ability of ACT5 to distinguish small targets in the tank. The ability of ACT5 to apply optimal current patterns is also shown on a box tank. Human experiments include image reconstruction of normal breathing and image reconstruction of heart activity during a breath-holding session. ACT5 capability to collect ECG recordings from all electrodes are also shown.
Acronyms

2-D 2-Dimensional. 4

3-D 3-Dimensional. 4

ACT5 Adaptive Current Tomograph 5. 3

ADC Analog-to-Digital Converter. 28

APT Applied Potential Tomography. 16

CIPO Controller In, Peripheral Out. 34

COPI Controller Out, Peripheral In. 34

CT Computerized Tomography. 1

CTS Clear to Send. 67

DAC Digital-to-Analog Converter. 28

DDS Direct Digital Synthesis. 28

ECG Electrocardiogram. 4

ECT Electrical Capacitance Tomography. 1

EIT Electrical Impedance Tomography. 1

EITS Electrical Impedance Tomography Spectroscopy. 1

EOF End-of-Frame. 67

ERT Electrical Resistivity Tomography. 1

FPGA Field-Programmable Gate Array. 26

GIC General Impedance Converter. 20
GUI  Graphical User Interface. 25

HDL  Hardware Description Language. 61

LSB  Least Significant Bits. 63

MRI  Magnetic Resonance Imaging. 1

MSB  Most Significant Bits. 63

NIC  Negative Impedance Converter. 20

OC  Open-Circuit. 56

PC  Personal Computer. 24

PCB  Printed Circuit Board. 30

ROI  Region of Interest. 16

RTS  Request to Send. 67

SD  Shield Driver. 19

SNR  Signal-to-Noise Ratio. 9

SPI  Serial Peripheral Interface. 24

SW  Switch. 42

UART  Universal Asynchronous Receiver/transmitter. 24

USB  Universal Serial Bus. 61

VME  Versa Module Eurocard. 24
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