Characterization of wide-bandgap SiC field effect transistors and their active gate driving circuit in high power applications

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CHARACTERIZATION OF WIDE-BANDGAP SIC FIELD EFFECT TRANSISTORS AND THEIR ACTIVE GATE DRIVING CIRCUIT IN HIGH POWER APPLICATIONS

by

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To my parents
ABSTRACT

Silicon Carbide (SiC) devices are slowly becoming one of the most reliable choices for high power density, high switching frequency applications with higher efficiency than Gallium Nitride (GaN) and Silicon (Si) devices. For a wide range of applications, such as Electric Motor Drives, Switching Power Supplies, and Renewable Energy Circuits, SiC devices are being tested and are found to yield prominent results.

In this research, the characterization of two similarly rated commercially available SiC devices - a trench Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and a cascoded Junction Field Effect Transistor (JFET) are done. It is followed by a comparative analysis of both devices. Firstly, a Conventional Gate Drive (CGD) circuit is implemented, followed by the proposal and implementation of an Active Gate Driver (AGD) circuit. Both the devices are characterized for the CGD and AGD topologies to predict whether the proposed circuit improves the device performance, based on dI/dt and dV/dt characteristics. Switching characteristics during turn-on and turn-off for both the CGD and AGD topologies are compared and it is observed that the proposed AGD circuit does minimize the switching losses. The proposed AGD topology follows a simple design of using an N-channel MOSFET (NMOS) with a series resistor in parallel with the turn-on branch and a P-channel MOSFET (PMOS) with a series resistor in parallel with the turn-off branch of the gate driver circuit of the device under test (DUT). Characterization of the DUT is done using SPICE models of the devices for a comparative study. It is followed by the design of a printed circuit board (PCB) to implement both the CGD and AGD topologies which is compatible with both the DUTs. The DUTs are chosen as such that their characteristics are very similar to one another for an accurate comparative analysis. The devices are tested at rail voltages from 200V to 800V and at inductor currents from 10A to 60A. A detailed analysis shows a reduction in switching losses and shortening of the miller plateau in the proposed AGD circuit when the switching is made faster whereas over-voltage and over-current reduction when the switching is slowed down. Thus the proposed AGD circuit can be used to either speed up switching to minimize losses or slow down switching to mitigate noise issues dynamically during circuit operation, which was the intended purpose of this research.
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ABBREVIATIONS

AGD Active Gate Driving.

BJT Bipolar Junction Transistor.

CGD Conventional Gate Driving.

DUT Device Under Test.

FWD Free-Wheeling Diode.

IGBT Insulated-Gate Bipolar Transistor.

JFET Junction Field Effect Transistor.

MOSFET Metal Oxide Semiconductor Field Effect Transistor.

PCB Printed Circuit Board.

Si Silicon.

SiC Silicon Carbide.

SPICE Simulation Program with Integrated Circuit Emphasis.

$V_{PWL}$ Piecewise Linear Voltage Source.
Nomenclature

\( C_{ds} \)  Drain to source capacitance
\( C_{gd} \)  Gate to drain capacitance
\( C_{gs} \)  Gate to source capacitance
\( C_{iss} \)  Input capacitance
\( C_{oss} \)  Output capacitance
\( C_{ox} \)  Oxide capacitance
\( C_{rss} \)  Reverse transfer capacitance
\( E_{off} \)  Turn-off energy loss
\( E_{on} \)  Turn-on energy loss
\( E_{tot} \)  Total energy loss
\( f_T \)  Unity-gain frequency
\( g_m \)  Transconductance
\( I_D \)  Drain current
\( I_G \)  Gate current
\( Q_G \)  Gate charge
\( Q_{rr} \)  Reverse-recovery charge
\( R_{DS(on)} \)  Drain to source resistance
\( V_{ov} \)  Overdrive voltage
\( V_{th} \)  Threshold voltage
CHAPTER 1
Introduction

1.1 Overview

The growing advancements in the field of power electronics has facilitated the way for fabrication of highly efficient power semiconductor devices meeting the needs of modern appliances and automobiles. The industry standards nowadays is devices with more than 99% efficiency to meet the requirements such as high switching frequency, low switching losses and high current density simultaneously for high power applications.

Traditionally, power semiconductor devices made from [Si] such as IGBTs and MOS-FETs are either capable of working in high voltage and low frequency or low voltage and high frequency. On the contrary, [SiC] devices overcome this by performing high-speed switching at high voltage, which is the need for current power applications requiring high current density.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
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<tr>
<td>Bandgap, $E_g (eV)$</td>
<td>1.12</td>
<td>1.43</td>
<td>3.03</td>
<td>3.26</td>
<td>3.45</td>
<td>5.45</td>
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<tr>
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<td>11.9</td>
<td>13.1</td>
<td>9.66</td>
<td>10.1</td>
<td>9</td>
<td>5.5</td>
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<tr>
<td>Electric Breakdown Field, $E_c (kV/cm)$</td>
<td>300</td>
<td>400</td>
<td>2500</td>
<td>2200</td>
<td>2000</td>
<td>10000</td>
</tr>
<tr>
<td>Electron Mobility, $\mu_n (cm^2/V\cdot s)$</td>
<td>1500</td>
<td>8500</td>
<td>500</td>
<td>1000</td>
<td>1250</td>
<td>2200</td>
</tr>
<tr>
<td>Hole Mobility, $\mu_p (cm^2/V\cdot s)$</td>
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<td>400</td>
<td>101</td>
<td>115</td>
<td>850</td>
<td>850</td>
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<tr>
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<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
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<td>1</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
<td>2.7</td>
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Table 1.1: Physical Characteristics of Si and wide bandgap semiconductors

A comparative study of wide bandgap semiconductors and Si is shown in Table 1.1. Replacing traditional Si devices with SiC devices for power electronics applications such as EV charging, PV inverters, Switch mode power supplies etc. will typically result in more efficient systems having reduced losses, increased efficiency and reduced packing dimensions.

\[ \varepsilon = \varepsilon_r \cdot \varepsilon_0 \text{ where } \varepsilon_0 = 8.85 \times 10^{-12} F/m \]
i.e. size and volume. Hence SiC as the semiconductor choice for the research paves way for characterization of the transistors at very high voltages and current rise rates. Out of all the different existing polytypes of SiC, 4H–SiC is preferred for power devices primarily because of its high carrier mobility, particularly in the vertical c-axis direction[3].

1.2 Literature Review

Silicon carbide power devices have been investigated for more than two decades now, and a wide range of such devices are available commercially now[10]. Currently, the widely used power devices, which replaced the Si devices, are Gallium Nitride (GaN) and Silicon Carbide (SiC) devices out of which SiC devices are considered superior in terms of performance for their versatile high temperature applications, high voltage operation and high frequency switching as shown in Fig.1.1. Hence for the purpose of this experiment, the focus will be on SiC devices.

Figure 1.1: Summary of Si, SiC, and GaN relevant material properties[10, 12, 18]

The key points for choosing SiC devices for this thesis as seen in Fig.1.1 are:

1. Wider energy bandgap width means there will be much lower leakage currents and significantly higher operating temperatures in the SiC devices. Also, the devices will
have improved radiation hardening.

2. Higher breakdown electric field or critical electric field will enable having thinner blocking layers in the SiC devices. If the doping concentration is high too, it will result in very low on-resistance i.e. $R_{DS(on)}$ compared to equivalent Si or GaN devices.

3. Higher electron saturation velocity enables to higher frequency switching.

4. Higher thermal conductivity in SiC improves heat dissipation and allows operation at higher power densities\[^{15}\].

With all these aforementioned advantages, SiC devices becomes a suitable choice for the switching characteristics experiments to be conducted as a part of this thesis.

Figure 1.2: Milestones of SiC power devices’ development process\[^{4, 18}\]

The beginning of a new era in power semiconductor devices was marked by the launch of the SiC Schottky diode by Infineon\[^{20}\] as shown in Fig.1.2. Currently, the various types of SiC devices available commercially include JFETs, MOSFETs, BJTs and IGBTs. The devices chosen for this thesis are a MOSFET and a JFET.

Power MOSFETs are voltage-controlled devices and require only a small input current. The switching speed is very high and the switching times are of the order of nano-seconds. MOSFETs do not have the problems of second breakdown phenomena like BJTs. However, planar gate MOSFETs have the problems of electrostatic discharge and are relatively difficult
Infineon’s trench MOSFET structure is more reliable in comparison. It inherently exhibits a favorable capacitance ratio with the miller capacitance $C_{GD}$ being small while $C_{GS}$ being comparably large allowing for a well-controlled switching with very low dynamic losses. In particular this feature is essential to suppress undesirable parasitic turn-on.

JFETs, on the other hand, have a normally conducting channel connecting the source and drain. The gate is used as the contact to control current flow through the channel. The types of JFET structures currently available commercially are:

1. Lateral Channel JFET (LCJFET)
2. Vertical JFET (VJFET)
3. Vertical trench JFET (VTJFET)
4. Buried grid JFET (BGJFET)
5. Double-gate vertical channel trench JFET (DGVTJFET)

The UnitedSiC JFET utilises an N-channel depletion-mode VTJFET with very low $R_{DS(on)}$ and a specialized custom LV MOSFET cascoded in series connection to simplify FET operation and enable gate drive compatibility with all existing SiC MOS and Si IGBT and MOS switches. The device is normally-on depending on the thickness of the vertical channel and the doping levels of the structure. Enhancement-mode JFETs have natural advantages in safe operation as they are normally-off whereas the depletion-mode JFET have advantages with almost twice the saturation current, lower on-resistance and no gate current requirement in the on-state. The normally-on JFET remains in the on-state when no negative voltage is fed to the gate, whereas the gate-source junction of the normally-off JFET needs to be forward biased by supplying a positive voltage in order for it to conduct. Also to achieve a low on-state resistance, a large gate current should be supplied at steady state for the normally-off JFET which is not required for that of the normally-on JFET. Hence, in order to utilise these advantages, a normally-on JFET is used for the cascode design. Moreover, vertical JFETs, in general, exhibit very low switching losses making them an excellent candidate for high frequency, high-efficiency power conversion applications.
In the experiments, the top device in the half bridge configuration is a free-wheeling
diode for simplicity. A 1200V 50A SiC Schottky MPS diode is used, manufactured by Gen-
eSiC Semiconductor. Merged Pin Schottky (MPS) diode consists of inter-digitated Schottky
and p+ implanted areas. Only the Schottky regions of the diode conduct for on-state volt-
age drops less than 3V and so the device is also known as a Junction Barrier Schottky
(JBS) diode. The design consists of choosing the Schottky metal, size and spacing of the
p+ implanted regions, and thickness and dopant density of the drift region optimally. It is
important to achieve a good quality Schottky interface in order to obtain a low on-state drop
when operated in the JBS diode mode. The metal-SiC barrier height of the Schottky metal
must be low so that it gives a low on-state voltage but is still capable of enabling effective
pinch-off during the off state. This is achieved by using Nickel (Ni) as the Schottky metal[1].

Theoretically, SiC devices can allow a very high voltage and high operating temperature
due to their wide band-gap. However, the thermal capability of all materials has not reached
the same technological maturity. The maximum operating junction temperature for most
commercial SiC devices is only up to 210°C as of now[4]. The current rating and other
parameters of both the transistors are discussed in details in Chapter 2. Both of these device
technologies are fairly recent and further research and development on designing devices
with improved performances are still going on. Hence both of these devices will serve as an
excellent starting point to test and understand the current progress of SiC devices.

In order to characterize the devices to their fullest potential, it is not sufficient to
test and compare them with respect to a conventional gate drive circuit. A CGD circuit
encounters over-voltage during switching transitions. This induces sharp spike of current and
electromagnetic induction (EMI) in the circuit, mainly due to the high switching frequency
of SiC devices and presence of parasitic inductance in the circuit[25]. In order to improve
the switching performance, two methods can be adopted as seen in Fig.1.3.

1. Optimizing the power loop of the circuit to minimise the effect of parasitic inductance
which can be either minimising the PCB layout inductance or optimising the mea-
surements by placing the probes and coils as close to the packaged components as
possible.

2. Enhancing the performance of the gate driver circuit itself.
In this research, the second method of improving the gate driver circuit is explored. A CGD circuit operates with fixed voltage and resistance. A larger external gate resistance can minimise the switching stress and suppress EMI. However this will increase the switching losses and will slow down the device switching making one of the key features of SiC devices which is very fast switching frequency redundant. In order to overcome the shortcomings of the CGD topology, different active gate driver techniques have been proposed in the past few years.

The circuit proposed in [25] has a two-part implementation for active gate driving. The first stage is a FPGA controller circuit which runs at 200MHz. It controls the next stage which consists of four transistors to generate corresponding gate drive voltage. This proposed circuit increases the switching speed while minimising the switching stress.

The circuit proposed in [8] has a simpler design compared to the previous design. It uses a parallel capacitor and an auxiliary switch in the external gate resistance branch. The proposed circuit is intended to reduce crosstalk by improving the gate loop impedance and power loop impedance design. The parallel capacitor is so designed that it only operates during turn-off of SiC MOSFET and thereby reduces the crosstalk voltage effectively.

The circuit proposed in [13] utilizes a two-switch implementation coupled with high speed comparators to minimize over-current and over-voltage. The gate driver is able to control the di/dt turn-on and the dv/dt turn-off individually along with lowering the switching losses. This design can be used for high-frequency applications till 100 kHz of switching.
frequency and for high power converters.

The circuit proposed in [24] uses a gate boost circuit consisting of a delay circuit, resistor and switch. The proposed gate driver is able to reduce switching loss and switching time without increasing switching noise. Thus it provides a solution to optimize between the switching speed, switching loss and switching stress of the circuit.

The circuit proposed in [2] is predominantly for GaN devices but is an interesting design that can possibly be extended to other WBG devices too. The AGD technique in this design is based on a sub-nanosecond delay feedback loop, which reduces the gate current only during the dv/dt sequence of the switching transients. It uses a four transistor design preceded by a main stage driver with two transistors. Experimental results at 400V showed significant dv/dt reduction, with an optimization of the turn-on losses.

Reviewing these topologies and a few other proposed designs with the intention to either control the switching losses or minimizing the effect of noises, a simpler design was proposed and tested for this research. A two transistor design of an active driver is proposed in this research with minimal additions to the CGD topology. The main purpose of the proposed AGD circuit is to dynamically vary the gate resistance during switching in order to minimise losses and shorten the miller plateau region. This proposed design is explored in details in Chapter 4.

1.3 Motivation

Power electronic devices are used in applications requiring gate-drive circuits with advance control, high speed, high efficiency, and compactness, gate driver circuits is one of the first and foremost important requirements in today’s world. With this in mind, the main objective of this research is to explore the switching behaviour of two latest generation 1.2kV SiC transistors available and propose a gate driver circuit that can be used for these devices and yield highly efficient performance. The devices chosen for the experiments are a cascoded JFET from UnitedSiC and a CoolSiC trench MOSFET from Infineon Technologies. The JFET is a normally-on device whereas the MOSFET is a normally-off device which makes them an interesting choice for comparison. The device structure of the MOSFET is of a CoolSiC trench MOSFET cell which combines low static and dynamic losses with high
Si-IGBT like gate oxide reliability. The JFET on the other hand is an enhancement-mode power switch formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series offering low conduction and switching losses. Even though structurally the devices are different but their device parameters are very similar to one another as discussed in Chapter 2.

The main objectives of the experiments as a part of this thesis:

1. Generation of SPICE models of the JFET and MOSFET and double pulse test of the devices using conventional gate drive circuit
2. Proposal of an active gate driver circuit and double pulse test of the devices using the proposed circuit
3. Design of a printed circuit board capable of testing the both the gate drive methodologies using both the devices
4. Comparison of switching characteristics of the transistors and evaluation of the improvement in the proposed circuit

1.4 Outline

The thesis is divided into five chapters as described below:

Chapter 1 contains a brief introduction to the thesis with overview of power semiconductor devices, followed by detailed literature review of past experiments on the similar topics and an outline of the overall experiment plan.

Chapter 2 explores the basic working principle of SiC transistors. Starting with a comparison between SiC Cascoded JFET and MOSFET, this chapter explains the relevant switching characteristics of the devices for a Conventional Gate Driver (CGD) circuit by mathematical analysis and simulation of the said circuit.

Chapter 3 contains detailed discussion on the proposed Active Gate Driver (AGD) circuit with its simulation results and comparison with the CGD circuit results.

Chapter 4 explains the experimental setup followed by the analysis and comparison of the experimental results from the CGD and AGD circuits for both the JFET and the
MOSFET.

Chapter 5 contains the conclusion from the performed experiment with observations from the previous chapter and explores the possible future modifications and applications of the project.
CHAPTER 2
Switching Characteristics of SiC Power Devices

2.1 JFET vs MOSFET

The two most prominent SiC power switches commercially available currently are the cascaded JFET and trench MOSFET. Apart from their basic structural differences and working principles, they have a lot of common physical properties discussed in details later.

The cascaded SiC JFET chosen for this research is an enhancement-mode power switch formed by a high-voltage SiC depletion-mode JFET and a low-voltage Si MOSFET connected in series. The SiC JFET is intended to provide high voltage blocking in the off state whereas the Si MOSFET is intended to serve as the control unit. This combination of devices in a single package provides usability of the transistors with standard gate drivers offering superior performance in terms of low $R_{DS(on)}$, $C_{oss}$, $Q_G$, and $Q_{rr}$. This is essential for low conduction and switching losses. The body diode of the cascaded JFET package is said to have excellent reverse conduction capability and removes the need for an external anti-parallel diode.[22]

For high performance power switches, a proper PCB layout design is essential to minimize circuit parasitics due to the high $dv/dt$ and $di/dt$ during switching. An external gate resistor is used when the cascode is working in the diode mode to achieve the optimum reverse recovery performance.[22]

The SiC MOSFET, on the other hand, has a CoolSiC trench structure.[7] The most

![Figure 2.1: Cascoded JFET][22]

![Figure 2.2: MOSFET][7]
common SiC MOSFET structure uses a planar gate and a quasi-vertical structure. An alternative approach is double trench structure where using a trench gate results in an increased channel width but still provides a higher channel mobility even though off-axis material is used. In the CoolSiC trench structure, the main channel is exactly oriented along the a-plane <11\overline{2}0> which gives the best channel mobility and lowest interface trap density. Thus the optimal channel properties are realized with the tradeoff of using the 2nd trench sidewall as an active channel. This paves the way for a well-controlled switching with very low dynamic losses\textsuperscript{[19]}.

Commercial manufacture and applications of SiC FETs have increased exponentially over the past decade. Some of the companies that manufacture SiC devices are namely Cree (Wolfspeed), Infineon Technologies, ROhm Semiconductor and UnitedSiC. The devices chosen for this research are UF3C120040K4S cascoded JFET from UnitedSiC and IMW120R030M1H MOSFET from Infineon Technologies. The common key factor in choosing these devices is their very low $R_{DS(on)}$ in the range of a few mΩ, other than their similar voltage and current ratings. A comparative study of some of the important parameters of the transistors is shown in Table 2.1.

<table>
<thead>
<tr>
<th>Property</th>
<th>JFET</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model No.</td>
<td>UF3C120040K4S</td>
<td>IMW120R030M1H</td>
</tr>
<tr>
<td>Drain-source voltage, $V_{DS}(V)$</td>
<td>1200</td>
<td>1200</td>
</tr>
<tr>
<td>Gate-source voltage, $V_{GS}(V)$</td>
<td>-25 to +25</td>
<td>-7 to +23</td>
</tr>
<tr>
<td>Continuous drain current, $I_D(A)$</td>
<td>65</td>
<td>56</td>
</tr>
<tr>
<td>$T_c = 25°C$</td>
<td>47</td>
<td>45</td>
</tr>
<tr>
<td>$T_c = 100°C$</td>
<td>175</td>
<td>150</td>
</tr>
<tr>
<td>Pulsed drain current, $I_{DM}(A)$</td>
<td>-55 to 175</td>
<td>-55 to 175</td>
</tr>
<tr>
<td>$T_c = 25°C$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating and storage temperature $(°C)$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1: Comparing Characteristics of chosen JFET and MOSFET\textsuperscript{[7],[22]}

The packaged JFET and MOSFET are shown in Figures 2.1 and 2.2. In order to understand about the electrical characteristics of the two devices, it is mandatory to understand first the how they can be switched. For this research, ISO5852S High-CMTI 2.5-A and 5-A Reinforced Isolated FET Gate Driver\textsuperscript{[21]} is chosen to drive the gate terminal of these

\textsuperscript{1}Limited by $T_{J,max}$

\textsuperscript{2}Pulse width $t_p$ limited by $T_{J,max}$
devices.

Conventional gate driving technique is used first to examine the switching characteristics of these devices followed by an active gate driving technique. The aim of this research is to calculate the switching losses in CGD and minimise them in AGD.

It is imperative to understand the working of the circuit elements before moving forward with the SPICE simulations and PCB design.

2.2 Circuit Analysis

2.2.1 Equivalent Model

The MOSFET equivalent model is shown in figure 2.3. The capacitance between the FET terminals can be expressed in terms of the device parameters as follows:

\[
C_{iss} = C_{gd} + C_{gs} \\
C_{oss} = C_{gd} + C_{ds} \\
C_{rss} = C_{gd}
\]  

(2.1)  

(2.2)  

(2.3)

where \(C_{iss}\) is the input capacitance, \(C_{oss}\) is the output capacitance, \(C_{rss}\) is the reverse transfer capacitance, \(C_{gd}\) is the gate to drain capacitance, \(C_{gs}\) is the gate to source capacitance and \(C_{ds}\) is the drain to source capacitance.
The values of $C_{iss}$, $C_{oss}$ and $C_{rss}$ are fixed for a particular FET device. The corresponding values of these capacitances for the devices chosen for the research are given in the following table:

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>JFET</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{iss}$ (pF)</td>
<td>1500</td>
<td>2120</td>
</tr>
<tr>
<td>$C_{oss}$ (pF)</td>
<td>210</td>
<td>116</td>
</tr>
<tr>
<td>$C_{rss}$ (pF)</td>
<td>1.7</td>
<td>13</td>
</tr>
</tbody>
</table>

Table 2.2: Capacitance values of chosen JFET and MOSFET[7][22]

These dynamic characteristics are dependent on temperature as well as the applied voltages as stated above. Considering a particular value of $V_{DS}$ and $V_{GS}$, it is possible to calculate the terminal capacitances using the equations 2.1 - 2.3. In the next sections, these capacitances will be re-calculated based on various pre-defined models, and the values can be equated to derive values of some unknown parameters such as the $R_{G,ext}$ values for the on and off transitions.

2.2.2 Small Signal Analysis

The small signal circuit models during on and off transitions are shown in Figures 2.4 and 2.5 respectively. The $V_{in}$ signal denotes the output coming from the gate driver circuit via the totem-pole. The $V_{gs}$ of the DUT during on-transition is denoted by

$$V_{gs,on} = V_{in} - V_{th}$$

or, $$V_{gs,on} = V_{CC} - V_{th}$$ (2.4)

where $V_{th}$ denotes the threshold voltage of the transistor and $V_{CC}$ is the voltage applied at the VCC2 pin (pin 5) of the gate driver and fed to the collector terminal of the NPN transistor at the top of the totem-pole. The diode current, $I_{D,on}$ is given by

$$I_{D,on} = I_s \cdot e^{(V_{D} - V_T)}$$

or, $$I_{D,on} = I_s \cdot e^{(V_{in} - V_{T})}$$

$^3$V$_{DS}$ = 100V, V$_{GS}$ = 0V, f = 100kHz
$^4$V$_{DD}$ = 800V, V$_{GS}$ = 0V, f = 1MHz, V$_{AC}$ = 25mV
Figure 2.4: Small signal model circuit during ON transition[17]

\[ I_{D,\text{on}} = I_s \cdot e^{(V_{CC}/n \cdot V_T)} \]  \hspace{1cm} (2.5)

where \( V_T \) is the thermal voltage and \( V_T = kT/q \) where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature in K and \( q \) is the magnitude of electronic charge, \( I_s \) is the saturation current or scale current, \( V_D \) is the forward bias voltage and \( n \) is a constant, usually between 1 and 2.

Using Kirchoff’s law, the gate current of the DUT is calculated to be

\[ I_{g,\text{on}} = I_{D,\text{on}} + V_{gs,\text{on}} \cdot R_{on} \]  \hspace{1cm} (2.6)

or,

\[ I_{g,\text{on}} = I_s \cdot e^{(V_{CC}/n \cdot V_T)} + (V_{CC} - V_{th}) \cdot R_{on} \]  \hspace{1cm} (2.7)

Now, the gate to source voltage \( V_{gs,\text{on}} \) can also be expressed as

\[ \frac{dV_{gs,\text{on}}}{dt} = \frac{1}{C_{gs}} I_{g,\text{on}} \]

or,

\[ f \cdot (V_{CC} + V_{EE}) = \frac{1}{C_{gs}} I_{g,\text{on}} \]
integrating over the entire time period of the input waveform from the Arduino, 60µs)

\[ C_{gs} = \frac{I_{g,on}}{f \cdot (V_{CC} + V_{EE})} \]  

(2.8)

or, \[ C_{gs} = \frac{I_s \cdot e^{(V_{CC}/n \cdot V_T)}}{f \cdot (V_{CC} + V_{EE})} \]  

(2.9)

where \( f \) is the frequency of the input signal and \( V_{EE} \) is the voltage applied at the VEE2 pins (pins 1 & 8) of the gate driver and fed to the collector terminal of the PNP transistor at the bottom of the totem-pole.

Figure 2.5: Small signal model circuit during OFF transition

Now, similarly the \( V_{gs} \) of the DUT during off-transition is denoted by

\[ V_{gs,off} = V_{in} + V_{th} \]

or, \[ V_{gs,off} = -V_{EE} + V_{th} \]  

(2.10)

The diode current, \( I_{D,off} \) is given by

\[ I_{D,off} = I_s \cdot e^{(V_D/n \cdot V_T)} \]

or, \[ I_{D,off} = I_s \cdot e^{(V_{gs,off}/n \cdot V_T)} \]
or,  \( I_{D,\text{off}} = I_s \cdot e^{(-V_{EE} + V_{th})/(n \cdot V_T)} \)  \hspace{1cm} (2.11)

Using Kirchoff’s law, the gate current of the DUT is calculated to be

\[
I_{g,\text{off}} = -I_{D,\text{off}} + V_{gs,\text{off}} \cdot R_{\text{off}}
\]  \hspace{1cm} (2.12)

or,  \( I_{g,\text{off}} = I_s \cdot e^{(-V_{EE} + V_{th})/(n \cdot V_T)} + (-V_{EE} + V_{th}) \cdot R_{\text{off}} \)  \hspace{1cm} (2.13)

Now, the gate to source voltage \( V_{gs} \) can also be expressed as

\[
\frac{dV_{gs,\text{off}}}{dt} = \frac{1}{C_{gs}} I_{g,\text{off}}
\]

or,  \( f \cdot (V_{CC} + V_{EE}) = \frac{1}{C_{gs}} I_{g,\text{off}} \)

(integrating over the entire time period of the input waveform from the Arduino, 60\(\mu\)s)

\[
\text{or, } C_{gs} = \frac{I_{g,\text{off}}}{f \cdot (V_{CC} + V_{EE})}
\]

\[
\text{or, } C_{gs} = \frac{I_s \cdot e^{(-V_{EE} + V_{th})/(n \cdot V_T)} + (-V_{EE} + V_{th}) \cdot R_{\text{off}}}{f \cdot (V_{CC} + V_{EE})}
\]  \hspace{1cm} (2.15)

Equating the expressions for \( C_{gs} \) from the equations 2.9 and 2.15, it is possible to derive a ratio of the desired \( R_{\text{on}} \) and \( R_{\text{off}} \) in terms of \( V_{EE} \) and \( V_{CC} \), which are constants for the circuit. For this experiment, the value of 10\(\Omega\) is chosen for \( R_{\text{off}} \) and \( R_{\text{on}} \). Other than that, during simulation, the resistor values is varied between 5\(\Omega\) and 20\(\Omega\) in order to understand how the \( E_{\text{on}} \) and \( E_{\text{off}} \) varies with the resistor values.

### 2.2.3 High Frequency Model Analysis

The high frequency equivalent circuit models during on and off transitions are shown in Fig. 2.7 and 2.8 respectively. The analysis is very similar to the small signal model. The only additional components in these models are that the parasitic capacitance between all the terminals are considered here, which can be calculated using the equations stated in the previous two sections.
Some of the notable parameters in these model are:

\[ g_m = \mu_n C_{ox} \frac{W}{L} V_{ov} \]

\[ \text{or,} \quad g_m = \frac{2I_D}{V_{ov}} \]  \hfill (2.16)

where \( g_m \) is the transconductance, \( \mu_n \) is the electron mobility, \( C_{ox} \) is the oxide capacitance, \( W \) is the channel width, \( L \) is the channel length, \( I_D \) is the drain current and \( V_{ov} = V_{gs} - V_{th} \).
These parameters are dependent on the device that is being characterised.

$I_D$ is the drain current without the channel-length modulation and given by,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2$$  \hspace{1cm} (2.17)

The output resistance between the drain and source terminals, $r_o$, is given by,

$$r_o = \frac{|V_A|}{I_D}$$  \hspace{1cm} (2.18)

where $V_A = \frac{1}{\lambda}$ is a FET parameter.

Another important parameter for high frequency operation is the unity-gain frequency, $f_T$. The MOSFET hybrid-$\pi$ model is shown in Fig.2.9 with the source as the common terminal between the input and the output ports.

![MOSFET Hybrid-\(\pi\) model](image)

**Figure 2.8: MOSFET Hybrid-\(\pi\) model\[17\]**

In order to calculate the short-circuit current gain, the input is fed with a current source $I_i$ and the output terminals are short-circuit. The current in the short-circuit is given by

$$I_o = g_m V_{gs} - sC_{gd} V_{gs}$$

where $s$ is the Laplace variable. Since $C_{gd}$ is small at high frequencies, the above equation can be stated as

$$I_o = g_m V_{gs}$$  \hspace{1cm} (2.19)
Now, \( V_{gs} \) can be expressed in terms of the input current as

\[
V_{gs} = \frac{I_i}{s(C_{gs} + C_{gd})}
\]

(2.20)

From equations 2.19 and 2.20, the short-circuit current gain can be stated as

\[
\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}
\]

(2.21)

The Laplace variable \( s=j\omega \) for physical frequencies. Therefore, the frequency at which the magnitude of current gain becomes unity can be stated as

\[
\omega_T = \frac{g_m}{(C_{gs} + C_{gd})}
\]

or in other words, the unity-gain frequency, \( f_T \) is

\[
f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}
\]

(2.22)
as \( f_T = \omega_T / 2\pi \). The value of \( g_m \) can be substituted from equation 2.16 here in order to express \( f_T \) in terms of the drain current.

### 2.3 Double Pulse Test

The input pulse shown in Figure 2.9 is generated using Arduino Uno Rev3 and fed to the gate driver ISO5852S. The code used for the circuit setup is included in the appendix. The main focus in this section is to understand the various working modes of the circuit by discussing the timing diagram in details.

The output from the gate driver circuit is fed to a totem-pole circuit. The totem-pole, often referred to as a push-pull amplifier comprises of MJD44H11/MJD45H11 BJT pair, capable of handling upto 8A current[21]. The purpose of using a totem-pole as seen in Fig.2.15 below is to push current to the DUT when the output voltage from the gate driver is high, which activates the NPN transistor at the top connected to \( V_{CC} \) and then to pull current from the DUT when the output voltage is low, which activates the PNP transistor at the bottom connected to \(-V_{EE}\).
The voltage from the totem-pole is fed onto the DUT via the $R_{on}$ and $R_{off}$. The on-transition and off-transition paths are isolated from one another using low voltage diodes as shown in Figs.2.4 and 2.5. The purpose of the diodes is not only to isolate the two paths but also to block any stray currents flowing back into the gate driver. Hence they are placed in opposite directions with respect to one another in order to facilitate unidirectional current flow between the gate driver and the DUT.

The most significant challenge with power semiconductor devices is to minimise their switching losses while maintaining acceptable switching noises. In order to measure the switching parameters of a power device, the standard method used is a double pulse test\[9\]. The timing diagram of the double pulse test is shown in Fig.2.10 with the 4 modes of operation subsequently shown in Figs.2.11-2.14. As the name suggests, the double pulse consists of two pulses of different pulse width. The pulse width of the first pulse is much larger than the second pulse because they serve different purposes in the device characterization. In Figs.2.10-2.14, The gate-source voltage, $V_{gs}$ is equal to $-V_{EE}$ when the device is off and $V_{CC}$ when on. The drain current, $I_D$ varies between the intended maximum current value $I_{D,\text{max}}$ and 0A. The drain-source voltage, $C_{ds}$ is equal to 0V when the device is on and equal to the rail voltage, $V_{RAIL}$ when the device is off. The current through the free-wheeling diode, $I_{FWD}$ is equal to 0A when the device is on and equal to $I_L$ when its off, where $I_L=I_{D,\text{max}}$.

The different modes of operation are discussed below:

1. Mode 1(t1-t2): During mode 1, the device turns on at t1 and the inductive load ramps
up to reach the desired current value $I_{D,\text{max}}$ as shown in Fig.2.11. This is first wider pulse of the two pulses used in the test and the device turns off at $t_2$.

2. Mode 2($t_2$-$t_3$): As the device turn off at $t_2$, current from the device flows into the free-wheeling diode as shown in Fig.2.12. The device turns back on at $t_3$ and the current from the diode flows back into the drain terminal of the device connected to the inductive load.

3. Mode 3($t_3$-$t_4$): The device turns on again at $t_3$ and the current level from $t_1$ is maintained at the drain terminal at $t_3$ as shown in Fig. 2.13. This is the second narrower
pulse and the device is on only for a small amount of time such that the current remains almost constant and do not ramp up again. The turn-on and turn-off losses are measured during this pulse near t3 and t4 respectively.

4. Mode 4 (t4 onwards): At t4, the device is turned off again which completes the double pulse test. The current at the drain terminal will go down to 0 and feed into the free wheeling diode again, as shown in Fig.2.14 until the device is turned on again.

The complete double pulse test setup is shown in Figure 2.15 below. The control signal sent from the Arduino is at 5V which is not sufficient to turn on the DUT fully.
In order to level shift the incoming signal from the Arduino, a Totem Pole circuit is used at the output of the gate driver before feeding the signal onto the gate of the DUT. The 15V/20V drive required by the power transistors are met ensuring high-voltage isolation between the driver side and the micro-controller side. As seen in Fig.2.10, the collector of the NPN [BJT] is connected to $V_{CC2}$ and the collector of the PNP [BJT] is connected to $-V_{EE2}$ which are the positive and negative output supplies with respect to GND2 respectively. For this experiment, $V_{CC2}$ is kept at 15V and $-V_{EE2}$ is kept at -5V. The emitters are connected together and then connected to the next circuit stage containing the external gate resistors.
and diode isolation before making it’s way onto the DUT. This complementary pair of BJTs form the Totem Pole or the Push-Pull output stage. The purpose is to maximize the output voltage, equal to the supply voltage. Thus emitter follower circuits are used, made of NPN and PNP transistors in sequence for both load sourcing and load sinking. Hence, the double pulse exiting the totem pole stage varies between $V_{CC2}$ and $-V_{EE2}$ instead of 5V and 0V as supplied by the Arduino, as if the higher voltage is pulled up to 15V from 5V and the lower voltage is pushed down to -5V from 0V, hence justifying the name given to this kind of circuit. This also acts as a non-inverting current buffer to increase the gate drive current,
which is required for certain IGBTs. Since the DUTs in this experiment do not require very high gate current, the MJD44H11/MJD45H11 BJT pair is used, which is appropriate for currents up to 8A.\[21\]

The double pulse generation is fairly straight-forward in a SPICE software using a \(V_{\text{PWL}}\) source. The details of it are mentioned in the following section. The most important aspect of the double pulse generation is to determine the appropriate pulse width for the correct optimal operation of the circuit and to measure the requisite parameters in order to determine the usability of the DUT. The method used to replicate the double pulse
Figure 2.15: Double Pulse Test Setup Schematic for Conventional Gate Driving

generation in order to test the hardware has been discussed briefly in the previous sections and will be further discussed in Chapter 4 alongside the experimental results. The first wider pulse of the double pulse determines how much current will be generated at the drain of the DUT, and hence is calculated using the following equation:

\[ \delta V = L \frac{\delta I}{\delta T} \]

\[ \text{or, } \delta T = L \frac{\delta I}{\delta V} \]  \hspace{1cm} (2.23)

where \( \delta T \) is the width of the first pulse, and the width of the second pulse is kept at a constant of 1\( \mu \)s in order to prevent the drain current increase significantly and stay almost constant. \( L \) is the external load inductor connected at the high voltage side of the circuit. \( \delta V \) and \( \delta I \) are the change in the drain voltage and current respectively, and is hard-coded in the Arduino code for each voltage and current level operation. The code used in this experiment with the Arduino is included in the Appendix. In this experiment, the rail voltage is varied from 200V upto 800V and the drain current from 10A upto 60A. The load inductor, connected in parallel with the FWD, is kept at 60\( \mu \)H in order to prevent saturation at higher currents.

2.4 Simulation Results

The first simulation tests done with the transistors in SPICE is testing the typical output characteristics of the devices at 25\( ^\circ C \), as shown in Figs.2.16-2.19. The JFET was
swept from 0-10V whereas the MOSFET was swept from 0-20V as seen in the plotted waveforms. The output characteristics matches that to the datasheets of the transistors respectively, hence it can be inferred that the SPICE models are working as intended.

![SPICE Schematic for JFET Output Characteristics](image)

**Figure 2.16: SPICE Schematic for JFET Output Characteristics**

The SPICE models were imported onto LTspice and simulated. The values of the drain currents for a particular drain-source voltage of the transistor was recorded in a spreadsheet and plotted using MS Excel. As seen in Figs.2.17 and 2.19, there are multiple curves in each plot for a particular values of gate-source voltage, as mentioned. This is essential to understand the various working modes of the DUT, namely cut-off, active and saturation which can be seen in the plotted waveforms.

After testing and verifying the output characteristics in LTspice, the next set of simulations is to determine the switching characteristics of transistors, i.e. to calculate the switching losses, $E_{ON}$ and $E_{OFF}$ and also analyse the gate voltage transitions.

Fig.2.20 shows the SPICE schematic used to determine the switching characteristics of the JFET and Fig.2.23 shows that of the MOSFET. The gate voltage transitions of the transistors are shown in Figs.2.21 and 2.24 respectively and the switching losses versus...
the drain current are plotted in Excel and shown in Figs.2.22 and 2.25 respectively. The switching losses are also observed for various V_{RAIL} values and is included completely in the Appendix. A comparative plot of the total switching losses when V_{RAIL} is 200V, 400V, 600V and 800V are shown in Figs.2.26 and 2.27 for the JFET and MOSFET respectively. It is quite obvious that the switching losses are lower when the V_{RAIL} or V_{DD} is lower, with all other parameters kept constant.

Apart from varying the rail voltage, the gate voltage and external gate resistor were also varied in order to understand their impact on the switching losses. It is observed from Figs.2.28 and 2.29 that lowering the equivalent external gate resistor lowers the overall switching loss, but the circuit becomes very fast thereby making it more susceptible to electromagnetic interference. Hence a optimum gate resistance of 10\(\Omega\)is chosen for the experiment. On the other hand, the gate voltage is chosen to be +15V/-5V for observing an optimal performance from both the transistors and to compare them more suitably. The MOSFET can operate between +23V and -7V with its best performance at +20V/-5V and the JFET yields the best performance at +15V/-5V as seen from Figs. 2.30 and 2.31. The package inductance of the JFET plays a crucial role in the odd increase of the switching

Figure 2.17: Simulation Waveform for JFET Output Characteristics
losses at +20V/-5V as compared to the +15V/-5V combination. The losses should have followed a similar trend as of the MOSFET otherwise. Therefore in order to make an optimum comparison and reducing any such parasitic switching losses, both the devices are supplied with the particular gate-source voltage of +15V/-5V.

As seen from the gate voltage of both the transistors, it is seen that during the switching transitions, a miller plateau region is formed which adds to the losses. The same can be seen in the drain-source voltage transition too and is one of the primary concerns that needs to be addressed in order to make the devices more efficient. Chapter 3 on active gate driving will focus on this issue. Circuit designs will be proposed which aims to reduce the switching losses by transitioning faster through the miller plateau region by dynamically varying the gate resistor and thereby also making the circuit less susceptible to external factors such as EMI.

Chapter 3 will also feature further comparative studies between the devices as well as the gate driving methodology to infer whether the approach taken is fruitful in achieving more reliable circuits. The circuit modifications will be discussed in detail before diving
Figure 2.19: Simulation Waveform for MOSFET Output Characteristics

onto the actual hardware experiment setup, which will be discussed in Chapter 4. Chapter 4 will feature the CGD and AGD circuit setups followed by the experimental results. The main goal in that chapter will be to re-verify the simulation results from Chapters 2 and 3 and to understand the differences if any. One of the key design differences on the high voltage side of the DUT between the simulation and hardware experimental setups is that in simulation, the isolated gate driver has been replaced by ideal diode isolation, the external inductive load has been replaced by a constant current source and the FWD is also kept as an ideal diode. This prevents addition of further losses into the circuit, but also preserves the intended functionality as the experiment is concerned with the turn-on and turn-off of the circuit.

Thus the purpose of determining the switching characteristics of the transistors and their comparative analysis was to identify the transistor yielding better performance under the same test conditions. Observing the various plots of the switching characteristics of the transistors, it can be clearly seen that the JFET performs much better in terms of switching losses. For example, from Figs.2.26 and 2.27 it can be seen that for the same rail voltage and drain current, the total switching losses of the MOSFET twice or thrice that of the
JFET. Hence in applications such as DC-DC converters, PV inverters, motor drives etc. involving switching of inductive loads, the JFET will be a more suitable choice given their low switching losses in spite of having similar device rating as that of the MOSFET. It is also seen that the turn-on switching losses are dependent on the gate voltage and external gate resistor values whereas the turn-off switching losses is solely dependent on the drain current. This dependence of the losses on the various circuit parameters will prove to be useful while experimenting with the hardware setup. Even though the simulation circuits contain various ideal components which in the real circuit is bound to be different due to various noises adding up with the voltage and current waveforms and thereby adding on to the switching losses, the overall performance of the devices will remain similar and comparable. Hence while designing the PCB for the experiment and while populating the circuit board later with the electronic components, one of the key factors to keep in mind is the parasitic inductance adding up to the gate drive circuit. These will be further discussed in the following chapters when the comparisons are done side by side.
Figure 2.21: Simulated Results: JFET Gate Voltage Waveform at $V_{gs}=[-5V,15V]$, $V_{ds}=800V$ & $I_d=40A$

Figure 2.22: Simulation Waveform for JFET Switching Losses
Figure 2.23: SPICE Schematic for MOSFET Switching Characteristics

Figure 2.24: Simulated Results: MOSFET Gate Voltage Waveform at $V_{gs}=[-5\,\text{V}, 15\,\text{V}]$, $V_{ds}=800\,\text{V}$ & $I_d=40\,\text{A}$
Figure 2.25: Simulation Waveform for MOSFET Switching Losses

Figure 2.26: Simulated Results: Comparative Waveform for JFET Switching Losses
Figure 2.27: Simulated Results: Comparative Waveform for MOSFET Switching Losses

Figure 2.28: Simulated Results: JFET Switching Losses for various external gate resistors at $V_{gs}=[-5\,\text{V},15\,\text{V}]$, $V_{ds}=800\,\text{V}$ & $I_d=40\,\text{A}$
Figure 2.29: Simulated Results: MOSFET Switching Losses for various external gate resistors at $V_{gs}=-5V, 15V$, $V_{ds}=800V$ & $I_d=40A$

Figure 2.30: Simulated Results: JFET Switching Losses for various gate voltages

Package inductance adds up to the switching losses.
Figure 2.31: Simulated Results: MOSFET Switching Losses for various gate voltages
CHAPTER 3
Active Gate Driving

3.1 Circuit Analysis

The circuit schematic and setup of the proposed Active Gate Driver is shown in Fig.3.1. Various existing models were tested before finalizing this design aimed at not only reducing the electromagnetic interference in the circuit but also to keep the modifications simple and easy to implement. The changes in this AGD setup is very minimal from the CGD setup described in Chapter 2. An alternating ON transition path is added with a small resistor followed by an NMOS. Similarly, an alternating OFF transition path is added with a small resistor followed by a PMOS. The values of the resistors on the main ON and OFF paths are changed to make the overall equivalent gate resistor of the DUT close enough to the CGD analysis for a fair comparison of the switching losses using the two different methods. The main goal here is to dynamically vary the external gate resistor, $R_{G, ext}$ to shorten the miller plateau region by making the switching transitions faster or slower as needed and thereby minimize the switching losses.

Figure 3.1: Double Pulse Test Setup Schematic for Active Gate Driving
A detailed circuit analysis of the AGD setup is done before performing the simulations. The simplified equivalent small signal model between the totem pole and the DUT i.e. the external dynamic gate resistor of the DUT during ON and OFF transitions is shown in Fig.3.2. The input current, $I_{in}$ is given by

\[ I_{in} = I_{D, on} = I_s \cdot e^{(V_D/n \cdot V_T)} \]

or, \[ I_{in} = I_s \cdot e^{(V_{in}/n \cdot V_T)} \]

or, \[ I_{in} = I_s \cdot e^{(V_{CC}/n \cdot V_T)} \] (3.1)

where $V_T$ is the thermal voltage and $V_T = kT/q$ where $k$ is Boltzmann’s constant, $T$ is the absolute temperature in K and $q$ is the magnitude of electronic charge, $I_s$ is the saturation current or scale current, $V_D$ is the forward bias voltage and $n$ is a constant, usually between 1 and 2.

![Small Signal Model of the Active Gate Driving Circuit](image)

**Figure 3.2: Small Signal Model of the Active Gate Driving Circuit**
Let the current through $R_{on}$ be $I_1$ which can be written as
\[
I_1 = \frac{V_{CC} - V_T - V_{gs,DUT}}{R_{on}} \tag{3.2}
\]

and the current through the lower impedance path be $I_2$ which can be written as
\[
I_2 = \frac{V_{CC} - V_T - V_{dn}}{R_1} + \frac{V_{dn} - V_{gs,DUT}}{r_o} + g_m \cdot (V_{gn} - V_{gs,DUT}) \tag{3.3}
\]

where $V_{dn}$ and $V_{gn}$ are the voltages at the drain and gate of the added NMOS respectively.

The current at the gate of the DUT during the ON transition can thus be written as,
\[
I_{G,DUT} = I_{in} + I_1 + I_2 \tag{3.4}
\]

which can be substituted from the previous equations.

Similarly for the OFF transition, the input current, $I'_{in}$ is given by
\[
I'_{in} = I_{D,off} = I_s \cdot e^{(V_D/n \cdot V_T)}
\]
\[
or, \quad I'_{in} = I_s \cdot e^{(V_{in}/n \cdot V_T)}
\]
\[
or, \quad I'_{in} = I_s \cdot e^{(V_{EE}/n \cdot V_T)} \tag{3.5}
\]

Let the current through $R_{off}$ be $I'_1$ which can be written as
\[
I'_1 = \frac{V_{EE}}{R_{off}} \tag{3.6}
\]

and the current through the lower impedance path be $I'_2$ which can be written as
\[
I'_2 = \frac{V_{EE} - V_{dp}}{R_2} + \frac{V_{dp} - V_{gs,DUT}}{r'_o} + g'_m \cdot (V_{gp} - V_{gs,DUT}) \tag{3.7}
\]

where $V_{dp}$ and $V_{gp}$ are the voltages at the drain and gate of the added PMOS respectively.

The current at the gate of the DUT during the OFF transition can thus be written as,
\[
I'_{G,DUT} = I'_{in} + I'_1 + I'_2 \tag{3.8}
\]
which can be substituted from the previous equations. Since the DUT is a transistor, it can be considered as a capacitive switch as shown in Fig.3.2. Thus the change in current between the ON and OFF states, i.e. $\delta I = I_{G,DUT} - I'_{G,DUT}$. Therefore,

$$\delta V_{gs,DUT} = \frac{\delta I}{C_{gs,DUT}} \quad (3.9)$$

Integrating this equation over the entire duration of the double pulse generation, which is the pulse width of the two pulses and the OFF state separating the two pulses will yield the corresponding capacitor values of the DUT since the $V$ and $I$ will be known. This analysis can be expanded similarly into the high-frequency model, as was shown for the CGD circuit in Chapter 2, taking into account the other capacitors between the terminals of the DUT. For the purpose of simulation testing and circuit comparison, the small signal analysis is enough and can depict what can be expected out of the circuit model when simulated in LTSpice which is discussed in the next section.

3.2 Simulation Results

The first simulation tests done in SPICE are sweeping the NMOS and PMOS transistors used in the AGD circuit. The NMOS used in this experiment is IPD200N15N3G N-channel MOSFET from Infineon Technologies and the PMOS used is NTD2955T4G P-channel MOSFET from ON Semiconductor. The NMOS is connected in parallel with the $R_{G,on}$ with a 10Ω resistor in series, and the PMOS is connected in parallel with the $R_{G,off}$ with a 10Ω resistor in series respectively. Hence, a similar structure is followed for the sweep test as shown in Figs. 3.3 and 3.4 and the $V_{DS}$ are also assigned +15V and -5V to the NMOS and PMOS accordingly.

The NMOS and PMOS sweep schematics are shown in Figs. 3.3 and 3.4 below. Since there is a 10Ω resistor in series with the MOSFETs and a 20Ω resistor in parallel in the original CGD path, the external turn-on and turn-off gate resistance vary between 6.67Ω when the MOSFET is fully on and 20Ω when fully off. The detailed table containing equivalent gate resistor values is included in the Appendix. It is observed that the PMOS is partially on when $V_{gs,p}$ varies between -5V and -4V and the NMOS is partially on when the $V_{gs,n}$ varies between 5V and 6V respectively. The partially on mode is important as we see
the dynamic variance of the external gate resistance during this range.

The main idea for this approach of active gate driving is to dynamically vary the external gate resistor in order to shoot through the miller plateau region, thereby reducing the switching losses and the effect of electromagnetic interference on the circuit. Hence this partially on mode is the most important operating mode to understand and compare whether this approach works or not. The dynamic gate resistance for the NMOS and PMOS are plotted in Figs. 3.5 and 3.6 respectively. Even though when fully on, both the MOSFETs generate $R_{ds,ON}$ in the order of milli-ohms thereby making the equivalent external gate resistor the lowest, it is of less significance because when fully on, each of the turn-on and turn-off path will basically see two resistors - one 20Ω and one 10Ω in parallel, and the both the MOSFETs become redundant. Since the dynamic external gate resistance value is very close to the actual gate resistance value in the CGD circuit, it becomes more significant to compare the losses during this mode. This will be further explained in the later paragraphs.

The next step is to calculate the turn-on and turn-off losses in this proposed circuit in order to compare it with the CGD circuit switching losses calculated in the previous chapter as well as the compare the voltage transitions. The main region of concern during the switching is the miller plateau region. The miller effect exists because there is an effective capacitance $C_{gd}$ between the drain and gate of the FET, the so called miller capacitance. The miller plateau shows the amount of charge in $C_{gd}$ by its width. For a given FET the width of the miller plateau is a function of the voltage traversed by $V_{DS}$ as it switches on.
Figure 3.5: Simulated Results: NMOS Sweep Waveform to calculate dynamic \( R_g \)

The turn-on and turn-off losses are calculated separately for simplicity and to negate out any mutual effect since the path isolation in the simulation is achieved through an diode instead of an actual isolated gate driver as shown in Figs. 3.7 and 3.8.

Figs.3.9-3.12 show the turn-on and turn-off switching losses of the DUTs at (800V,20A) and (800V,60A) with respect to the gate-source voltage, \( V_{gs} \) of the MOSFETs in the AGD branch. From Figs. 3.9 and 3.11, it can be easily observed that the NMOS in the turn-on path of the AGD circuit is fully off between 0V to 5V, partially on between 5V to 6V and fully on from 6V onwards, thereby validating the results previously obtained from the NMOS sweep. Similarly, from Figs. 3.10 and 3.12, it can be easily observed that the PMOS in the turn-off path of the AGD circuit is fully off between 0V to -4V, partially on between -4V to -5V and fully on from -5V onwards, thereby validating the results previously obtained from the PMOS sweep. It can also be observed that changes in the resistance of the low voltage gate side of the DUT does not affect the turn-off losses in the JFET that much, which was also seen in Chapter 2.
Figure 3.6: Simulated Results: PMOS Sweep Waveform to calculate dynamic $R_g$

Figs.3.13-3.16 depicts the turn-on and turn-off switching losses of the DUT for different values of the drain current, $I_D$ of the DUT. From Figs. 3.13 and 3.15, it can be easily observed that the NMOS in the turn-on path of the AGD circuit is fully off between 0V to 4V and fully on from 6V onwards since the losses are higher in the former range, thereby validating the results previously obtained from the NMOS sweep. Similarly, from Figs. 3.14 and 3.16, it can be easily observed that the PMOS in the turn-off path of the AGD circuit is fully off between 0V to -4V, and fully on from -6V onwards, thereby validating the results previously obtained from the PMOS sweep. It is seen again that the changing the gate-source voltage of the PMOS does not affect the turn-off losses much in the JFET. It therefore proves the fact stated in Chapter 2 that the turn-on losses are mostly dependent on the gate voltage and external gate resistance of the DUT which in this case is dynamically varied by changing the MOSFET gate-source voltage in the added AGD path in parallel whereas the turn-off losses of the DUT is mostly dependent on the drain current of the DUT as seen from Figs.3.9-3.16.
Figure 3.7: Schematic to evaluate AGD Turn-On Characteristics

Figs.3.17 and 3.18 shows the $dV_{DS}/dT$ and the $dI_{D}/dT$ characteristics of the DUT. Here the JFET has been used to sweep. The particular three values of $V_{gs}$ of AGD MOSFETs has been chosen in order to make them work in the fully off, partially on and fully on modes respectively. As seen from the curves, it again emphasises the importance of the partially on mode. When the NMOS $V_{gs}$ equals 5.5V and the PMOS $V_{gs}$ equals -4.5V, the $dV_{DS}/dT$ and the $dI_{D}/dT$ values seem to be the lowest in comparison with the other two. Thus it is essential compare the switching losses and miller plateau of the CGD circuit with the AGD circuit when the NMOS and PMOS are partially on.

The comparison of the CGD and AGD circuits are done side by side as shown in Figs.3.19-3.22 and it is seen that the AGD circuits does minimise the switching losses in both the transistors. For the best set of comparison, the rail voltage is chosen to be 800V and the drain current as 60A which yields a significant amount of switching losses in both turn-on and turn-off of both the transistors and any small differences also will be visible in this test scenario. It is observed from the figures that the miller voltage is reduced and the turn-on and turn-off losses reduce significantly. A general trend is observed that the
switching transition in faster in the AGD circuit than the CGD circuit, thereby signifying that the $\frac{dV_{DS}}{dT}$ and the $\frac{dI_D}{dT}$ will be inherently lower in case of the AGD circuit, with the lowest being when the MOSFETs are partially on as seen in Figs.3.17 and 3.18. Figs.3.22-3.26 explores the partially-on state of the PMOS and NMOS further to understand how the switching losses actually varies and is seen to follow the expected trend.

It can therefore be stated that the AGD circuit does improve the circuit performance. The transitions are relatively faster, the switching losses are visibly lower and the miller effect is also lower compared to the CGD circuit. Even though it cannot be stated from simulation results alone, but looking at the trend of switching losses and other circuit characteristics, it can also be stated that the electromagnetic interference in the AGD circuit will be lower compared to the CGD circuit. In the next chapter, a better analysis can be shown when the actual test runs of the hardware circuit are computed and compared amongst the gate drive methodologies as well as with the simulation results. Even though there are many ideal parameters in the simulation tests, the double pulse test of the DUTs fulfills the purpose of characterising the device performance and the validity of the proposed AGD circuit. The
superior performance of the AGD circuit over the CGD circuit determines the usefulness of the proposed idea and its real world significance will be seen in the next chapter.
Figure 3.10: Simulated Results: $E_{OFF}$ vs Gate-Source Voltage of PMOS for JFET

Figure 3.11: Simulated Results: $E_{ON}$ vs Gate-Source Voltage of NMOS for MOSFET
Figure 3.12: Simulated Results: $E_{OFF}$ vs Gate-Source Voltage of PMOS for MOSFET

Figure 3.13: Simulated Results: $E_{ON}$ vs Drain Current for JFET
Figure 3.14: Simulated Results: $E_{\text{OFF}}$ vs Drain Current for JFET

Figure 3.15: Simulated Results: $E_{\text{ON}}$ vs Drain Current for MOSFET
Figure 3.16: Simulated Results: $E_{OFF}$ vs Drain Current for MOSFET

Figure 3.17: Simulated Results: $dV_{DS}/dT$ characteristics of DUT for varying $V_{gs}$ of AGD MOSFETs
Figure 3.18: Simulated Results: $dI_D/dT$ characteristics of DUT for varying $V_{gs}$ of AGD MOSFETs

Figure 3.19: Simulated Results: AGD vs CGD comparison of turn-on characteristics in JFET
Figure 3.20: Simulated Results: AGD vs CGD comparison of turn-off characteristics in JFET

Figure 3.21: Simulated Results: AGD vs CGD comparison of turn-on characteristics in MOSFET
Figure 3.22: Simulated Results: AGD vs CGD comparison of turn-off characteristics in MOSFET

Figure 3.23: Simulated Results: MOSFET partially on state $E_{\text{off}}$ variance in terms of PMOS’ $V_{\text{gs}}$
Figure 3.24: Simulated Results: MOSFET partially on state $E_{on}$ variance in terms of NMOS’ $V_{gs}$

Figure 3.25: Simulated Results: JFET partially on state $E_{off}$ variance in terms of PMOS’ $V_{gs}$
Figure 3.26: Simulated Results: JFET partially on state $E_{on}$ variance in terms of NMOS' $V_{gs}$
CHAPTER 4
Experimental Results

4.1 Experimental Setup

The experimental setup is shown in Fig. 4.1 and the PCB designed for this research using Autodesk EAGLE is shown in Fig. 4.2. The PCB shown is populated with the electronic components as stated in the BOM included in the Appendix. The major components at the gate driver side of the DUT includes the isolated gate driver ISO525SDW, the external gate resistors which are 1W 2512 1% thick film resistors, 30V 1A Schottky diodes for protection and added isolation between the turn-on and turn-off paths, IPD200N15N3G NMOS and NTD2955T4G PMOS for the active gate driver. The isolated gate driver ISO5852S used in this experiment is a 5.7-kVRMS, reinforced isolated gate driver for transistors with split outputs, OUTH and OUTL, providing 2.5-A source and 5-A sink current. Input CMOS
logic and output power stage of the gate driver are separated by a SiO$_2$ capacitive isolation. The input-output circuitry on the input side interfaces with a micro-controller and consists of gate drive control, RESET input, READY and FAULT alarm outputs. The power stage consists of power transistors to supply the 2.5A pull-up and 5A pull-down currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor collector-emitter over-voltage of the transistor under short circuit events. The capacitive isolation core consists of transmitter circuitry to couple signals across the capacitive isolation barrier, and receiver circuitry to convert the resulting lowering signals into CMOS levels. The gate driver also contains under-voltage lockout circuitry to prevent insufficient gate drive to the external transistor, and active output pull-down feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. Other than that, it also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to Miller effect, for uni-polar supply operation\cite{21}.

VCC and VEE which is 15V and -5V respectively is generated from MGJ6D241505DC isolated DC/DC converter taking 24V input and supplying 15V and -5V outputs. The major components at the supply side of the gate driver include various 0805 resistors and capacitors which are fed required voltages coming from TEC 2-2421WI isolated DC/DC
converter configured to take 24V input and supply 5V output. Both the DC-DC converter inputs are connected with small capacitors at the input and output sides to maintain voltage levels as per their datasheets. As mentioned earlier, the double pulse input to the gate driver is fed from an Arduino Uno and the program used has been included in the Appendix. As for the high voltage side of the DUT, 4 B32778Z8506K000 50µF capacitors are connected in parallel to generate 200µF capacitance, followed by the free-wheeling diode 1200V 50A SiC Schottky GC50MPS12-247, and the inductor is coiled manually to keep the number of turns as such that it generates 60µH inductance. This is measured using a LCR meter in order to make sure the current do not saturate below the intended value for the purpose of the test. A 270k 5W resistor SMF5270KJT is also connected in parallel with the capacitors. Since the 3-pin MOSFET has a different footprint than the 4-pin JFET, provision for both the footprints is kept in the PCB in order to test both the devices one after another. Lastly, the DESAT pin of the gate driver is connected by 3 1200V 2A SiC Schottky diodes GB02SLT12-252 in order to prevent any backflow from the high voltage side to the gate driver chip and beyond. After populating all the components correctly, it is suitable now to start testing the devices and analyse the results.

4.2 Experimental Results and Analysis

4.2.1 Conventional Gate Driving

The conventional gate drive circuit is run at rail voltages 200V, 400V, 600V and 800V respectively. The current is controlled using the 60µH inductor and is kept within the current limit of the transistors. As seen in Fig.4.3-4.4, the switching losses from both the transistors are recorded using Keysight MSOX3054T Mixed Signal Oscilloscope and the calculations are done in Excel and MATLAB using the .csv and .h5 files. Voltages $V_{gs}$ and $V_{ds}$ are measured using KeySight N2791A Differential Probes and the current $I_d$ is measured using Keysight N7312A Rogowski Coil. Figs.4.3-4.4 shows the screenshots of the oscilloscope during test and measurement. The product of $V_{ds}$ and $I_d$ is calculated using the MATH function from oscilloscope and then it is integrated to get the switching losses, i.e. the area under the curve of the product is calculated.

The switching losses calculated for different drain current values are plotted in Figs.4.5-4.8. Figs.4.5-4.6 shows the turn-on and turn-off losses of the JFET and Figs.4.7-4.8 shows the
Figure 4.3: Experimental Results: $V_{gs}$ (green, 50V/div), $V_{ds}$ (blue, 500V/div) and $I_d$ (red, 36A/div) measurement using oscilloscope at $V_{rail}=800V, I_L=40A$

turn-on and turn-off losses of the MOSFET. As seen in the figures, the switching losses trends are similar to what was observed in the simulation. Even though the switching transitions are susceptible to atmospheric noises and encounter ringing, the offset for both devices at 0V was calculated and subtracted from every calculated value for better accuracy. The switching losses at particular drain current and drain-source voltage is close to the observed value from simulation, and hence the total switching losses are also very close to that of the simulation. A general trend is observed that the turn-off losses are relatively lower and the turn-on losses are relatively higher compared to the simulation values for both the transistors. Both the turn-off and turn-on losses are thus also very close to the mentioned values in the respective datasheets of the devices.

4.2.2 Active Gate Driving

A similar technique as that of the CGD circuit is also utilised to measure the switching losses for the AGD circuit. After the CGD measurements were completed, the NMOS on
Figure 4.4: Experimental Results: Power calculation, $V_{ds}I_d$ (pink, 20kW/div) from $V_{ds}$ and $I_d$ during turn-on and turn off

the turn-on branch is populated along with the series resistance to measure the turn-on losses. Thereafter, the NMOS along with the series resistor is removed, and the PMOS on the turn-off branch is populated along with its series resistor to calculate the turn-off losses. They are not populated together for the experiment in order to nullify any interaction between the two devices, even though they are isolated by the gate driver. This setup for the experiment makes it exactly like it was in the simulation tests and hence the measurements and comparison will become more comprehensive and reliable.

For the AGD experiment, the rail voltages are chosen as 200V and 800V in order to
provide an understanding of the functionality at a comparatively low and high voltage. In the simulation tests, only 800V was used to determine whether the proposed AGD circuit had any improvements compared to the CGD circuit, since the change in switching losses will be more clearly visible at the highest rail voltage which is 800V for this experiment. Figs.4.9-4.16 shows the plots containing the turn-on and turn-off losses for both the JFET and the MOSFET at rail voltages of 200V and 800V for various gate-source voltage of the NMOS and PMOS respectively.

Figs.4.9-4.10 shows the JFET at 200V and Figs.4.11-4.12 at 800V whereas Figs.4.12-4.13 shows the MOSFET at 200V and Figs.4.15-4.16 at 800V. As it was seen in the simulation results too, it can be clearly observed from the results that the NMOS is fully off when its $V_{gs}$ is 0-4V, partially-on between 4-6V and fully on 6V onwards. Similarly, the PMOS is fully off when its $V_{gs}$ is -4V or below, partially-on between -4V and -6V and fully on -6V onwards. When either of the PMOS or NMOS is fully off, the external gate resistor at the DUT is the highest and hence the switching losses are high. It is clearly visible at the turn-on losses since the turn-on losses depend on the gate-source voltage and external gate resistor of the DUT. For the turn-off losses, it is not so clear since it is primarily dependent on the drain current of the DUT but nevertheless, a visible difference can be seen between the PMOS/NMOS
Figure 4.6: Experimental Results: JFET CGD turn-off switching losses for various $V_{ds}$ and $I_d$

fully-off and fully-on scenarios. One of the major points to note from the plots is that this demarcation between the PMOS/NMOS operating modes is more clearly visible for both the DUTs at 800V since the difference is larger, as was seen in the simulation. In the lower voltage of 200V, it is much less visible even though it’s there since the switching losses itself are many folds smaller at this rail voltage.

4.2.3 Comparative Analysis

After analysing the results, it is observed that the AGD circuit does improve the performance of the DUTs. The switching losses are comparatively lower than the CGD circuit which was also observed in the simulation results. In Figs.4.17-4.20, a comparative plot between the CGD losses and AGD losses are shown. The turn-on losses are compared when the $V_{gs}$ of the NMOS is at 4V and 6V, whereas the turn-off losses are compared when the $V_{gs}$ of the PMOS is at -4V and -6V. These particular voltages are chosen since at these values the NMOS and PMOS are at the junction of being fully on and fully off. In between these voltage values, they are partially on. It was observed in simulation that these devices being partially on provides the best comparative results, with the external gate resistance of the DUT being almost equivalent and thus the comparison makes sense. The key points
Figure 4.7: Experimental Results: MOSFET CGD turn-on switching losses for various $V_{ds}$ and $I_d$

to note from Figs.4.17-4.20 are that:

1. In the JFET, the turn-on losses for the AGD circuit with NMOS’ $V_{gs}$ at 6V are lower than the turn-on losses for the CGD upto a certain drain current value of approx. 45A.

2. In the JFET, the turn-off losses for the AGD circuit with PMOS’ $V_{gs}$ at -6V are lower than the turn-off losses for the CGD until the full scale of 60A.

3. In the MOSFET, the turn-on losses for the AGD circuit with NMOS’ $V_{gs}$ at 6V are lower than the turn-on losses for the CGD for the CGD until the full scale of 60A.

4. In the MOSFET, the turn-off losses for the AGD circuit with PMOS’ $V_{gs}$ at -6V are lower than the turn-off losses for the CGD until the full scale of 60A.

Thus, it can be stated that the AGD circuit does improve the switching performance of the devices. The $dI/dt$ and $dV/dt$ comparison of the devices are shown in Figs.4.21-4.23. This comparison shows visible ringing at the drain current and voltage transitions due to the noises in the circuit and package inductance of the DUT which was measured to be very high between 200-400nH. The switching losses were calculated by subtracting an offset which was the measured loss at 0V operation. This enabled a much appropriate comparison since the
same was done for both the CGD and AGD analyses. The switching losses are calculated by the area under the curve of the product of $I_d$ and $V_{ds}$, so subtracting an offset from this value makes sense. Comparing the transitions, it is seen that the visible improvements include shorter miller plateau of $V_{gs}$, lower under-voltage, lower over-voltage in $V_{ds}$ and lower current spikes in $I_d$ but at the cost of more off-state ringing and a higher over-voltage in the $V_{gs}$. Thus it is a trade-off to select the optimum conditions for the circuit operation.
Figure 4.9: Experimental Results: JFET AGD turn-on switching losses for various $I_d$ and NMOS’ $V_{gs}$ at the DUT $V_{ds}=200\text{V}$

Figure 4.10: Experimental Results: JFET AGD turn-off switching losses for various $I_d$ and PMOS’ $V_{gs}$ at the DUT $V_{ds}=200\text{V}$
Figure 4.11: Experimental Results: MOSFET AGD turn-on switching losses for various $I_d$ and NMOS’ $V_{gs}$ at the DUT $V_{ds} = 200V$

Figure 4.12: Experimental Results: MOSFET AGD turn-off switching losses for various $I_d$ and PMOS’ $V_{gs}$ at the DUT $V_{ds} = 200V$
Figure 4.13: Experimental Results: JFET AGD turn-on switching losses for various $I_d$ and NMOS’ $V_{gs}$ at the DUT $V_{ds}=800V$

Figure 4.14: Experimental Results: JFET AGD turn-off switching losses for various $I_d$ and PMOS’ $V_{gs}$ at the DUT $V_{ds}=800V$
Figure 4.15: Experimental Results: MOSFET AGD turn-on switching losses for various $I_d$ and NMOS’ $V_{gs}$ at the DUT $V_{ds}=800V$

Figure 4.16: Experimental Results: MOSFET AGD turn-off switching losses for various $I_d$ and PMOS’ $V_{gs}$ at the DUT $V_{ds}=800V$
Figure 4.17: Experimental Results: JFET turn-on switching losses comparison at $V_{ds}=800\,\text{V}$ for CGD and AGD at NMOS’ $V_{gs}=4\,\text{V},\,6\,\text{V}$

Figure 4.18: Experimental Results: JFET turn-off switching losses comparison at $V_{ds}=800\,\text{V}$ for CGD and AGD at PMOS’ $V_{gs}=-4\,\text{V},\,-6\,\text{V}$
Figure 4.19: Experimental Results: MOSFET turn-on switching losses comparison at $V_{ds}=800\text{V}$ for CGD and AGD at NMOS’ $V_{gs}=4\text{V},6\text{V}$

Figure 4.20: Experimental Results: MOSFET turn-off switching losses comparison at $V_{ds}=800\text{V}$ for CGD and AGD at PMOS’ $V_{gs}=-4\text{V},-6\text{V}$
Figure 4.21: Experimental Results: DUT $I_d$ comparison for CGD and AGD circuits

Figure 4.22: Experimental Results: DUT $V_{ds}$ comparison for CGD and AGD circuits
Figure 4.23: Experimental Results: DUT $V_{gs}$ comparison for CGD and AGD circuits
CHAPTER 5

Conclusion

5.1 Conclusion

In this research, an active gate driver circuit is proposed for improving the switching performance. The proposed design is intended to be used to dynamically varying the external gate resistance of the DUT in order to either speed up the switching transitions and minimize switching losses or to slow down the switching transition to minimize the switching stress and mitigate the effect of circuit noises. The experimental and simulation results from the previous chapters depict that the AGD circuit does achieve improvements over the switching characteristics from the CGD circuit. As observed, an optimization between the switching losses and switching stress is achieved as intended. Thus the purpose of usability of the AGD topology is fulfilled to an extent. But there are still room for improvement with an updated active gate driver with more control on the gate voltage and can form an immediate future work from this research.

5.2 Future Work

The immediate future work to follow this research would be to design an isolated DC-DC converter capable of powering the gate drive in a more portable solution than using multiple power supplies as used in this experiment. It can also form a tighter design overall, reducing a significant portion of stray inductances as noticed throughout this experiment.

The next possibility can be improving the gate driver control technique itself. The Arduino used in this experiment to feed the isolated gate driver fulfill its intended purpose for this research, but the switching transitions of the gate voltage is more prone to noise due to the fact the Arduino is susceptible to such circuit noises. This can be mitigated by using a more detailed design similar to [25] to allow more control on the gate pulse itself. A digital implementation using PWM signals from a superior FPGA controller can be a possible choice for this.
Another basic changes to possibly improve the device performance can be done by using the same DUT as the top device in place of the FWD. Further testing and characterization using a full bridge converter or a specialised DC-DC converter such as an LLC converter can be formed using the said DUTs to examine their usability and efficiency.

The other possible characterization can be using the same gate driver circuit for much higher voltage devices which are available commercially and possibly compare their performance with the DUTs chosen for this experiment at the 800V rail voltage to understand whether this design can be universally adapted or not.

In applications such electric vehicle, solar panels, power supplies both the DUTs can be a suitable choice for use, with the cascoded JFET edging before the trench MOSFET due to the switching losses of the JFET being around 30-40% of that of the MOSFET under similar working conditions. The test results from the simulation and experiment verify the same, as claimed in the datasheets of these devices. The results from these extensive series of experimental tests can also form a basis of understanding why the cascode topology is an added advantage for the JFET over the MOSFET.
APPENDIX A

Simulation

The code used for generating the double pulse using waveform Arduino Uno Rev3:

```c
// Double Pulse Generation
#define portOfPin(P)\n    (((P)>=0&&(P)<8)?&PORTD:(((P)>7&&(P)<14)?&PORTB:&PORTC))
#define ddrOfPin(P)\n    (((P)>=0&&(P)<8)?&DDRD:(((P)>7&&(P)<14)?&DDRB:&DDRC))
#define pinOfPin(P)\n    (((P)>=0&&(P)<8)?&PIND:(((P)>7&&(P)<14)?&PINB:&PINC))
#define pinIndex(P)((uint8_t)(P>13?P-14:P&7))
#define pinMask(P)((uint8_t)(1<<pinIndex(P)))
#define pinAsInput(P) *(ddrOfPin(P))&=~pinMask(P)
#define pinAsInputPullUp(P) *(ddrOfPin(P))&=~pinMask(P);digitalHigh(P)
#define pinAsOutput(P) *(ddrOfPin(P))|=pinMask(P)
#define digitalLow(P) *(portOfPin(P))&=~pinMask(P)
#define digitalHigh(P) *(portOfPin(P))|=pinMask(P)
#define isHigh(P)((*(pinOfPin(P))& pinMask(P))>0)
#define isLow(P)((*(pinOfPin(P))& pinMask(P))==0)
#define digitalState(P)((uint8_t)isHigh(P))

int k = 1;
int delV = 800; //200-800V
int delI = 40; //10-60A
int L = 60; //60uH
int delT = L*delI/delV + 1; //1us buffer time
void setup() {
    Serial.begin(9600);
    pinMode(7, INPUT);
    pinMode(2, OUTPUT);
```
void loop() {
    int sw = digitalRead(7);
    if((sw == HIGH) && (k == 1)){
        digitalHigh(2);
        delayMicroseconds(delT);
        digitalLow(2);
        delayMicroseconds(3);
        digitalHigh(2);
        delayMicroseconds(2);
        digitalLow(2);
        Serial.println(1);
        k++;
    }
}

The equivalent external resistor values from PMOS and NMOS sweep operation is shown in Fig.A.1 below:

<table>
<thead>
<tr>
<th>NMOS Sweep</th>
<th>PMOS Sweep</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vds</td>
<td>Vgs</td>
</tr>
<tr>
<td>0</td>
<td>1.75E+11</td>
</tr>
<tr>
<td>1</td>
<td>1.75E+11</td>
</tr>
<tr>
<td>2</td>
<td>1.75E+11</td>
</tr>
<tr>
<td>3</td>
<td>1.75E+11</td>
</tr>
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</tr>
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</tr>
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<td>7</td>
<td>1.14E+01</td>
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<tr>
<td>8</td>
<td>8.81E+00</td>
</tr>
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<td>9</td>
<td>6.77E+00</td>
</tr>
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<td>15</td>
<td>8.72E+00</td>
</tr>
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<td>1.14E+01</td>
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<td>6.75E+00</td>
</tr>
<tr>
<td>19</td>
<td>6.25E+00</td>
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</tr>
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<td>2.00E+02</td>
</tr>
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<td>1.50E+02</td>
</tr>
<tr>
<td>23</td>
<td>1.50E+02</td>
</tr>
</tbody>
</table>

Figure A.1: Dynamic Rg calculation table
APPENDIX B

Experiment

A broader picture of the experimental setup is shown in Fig.B.1. below: It shows the

differential probes used to measure the voltages $V_{GS}$ and $V_{DS}$ and the Rogowski coil used to measure the drain current $I_D$ of the DUT. It also shows the generated waveform on the oscilloscope which is saved using an USB drive.
BIBLIOGRAPHY


[5] Infineon Technologies AG, Coolsic™ 1200v sic mosfet application note, 1 2018, Revision 1.01.


[7] Infineon Technologies AG, Coolsic™ 1200v sic trench mosfet in to247-3 package, 12 2020, Rev. 2.2.


