Design and simulation of a voltage controlled current source for electrical impedance tomography applications

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Design and Simulation of a Voltage Controlled Current Source for Electrical Impedance Tomography Applications

By

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Abstract

Electrical impedance tomography (EIT) is a simple, non-invasive and ionizing radiation-free imaging technology with potential application to medical diagnostics such as lung function, cardiac output, breast cancer, and cysts. Of the above applications, lung imaging has developed into the prime application for EIT. Because it presents an ill-posed inverse problem, EIT requires high-precision instrumentation and this thesis studies a new method for obtaining a high-precision current source and voltmeter for EIT. This thesis describes various simulation studies performed in a voltage-controlled current source (VCCS). The output impedance (\(Z_O\)) of various types of Howland current sources including the basic Howland current source (BHCS), the improved Howland current source (IHCS), and variations these sources that prevent the generation of a DC current, are characterized in terms of the parallel components of output resistance (\(R_O\)) and output capacitance (\(C_O\)). We further analyze the voltage compliance, gain, and noise power density (NPD) of the system. A complete system for single-channel in an EIT system was simulated in which a sinusoidal signal is generated using an FPGA passes through a 16-bit digital-to-analog converter (DAC), difference amplifier, BHCS, load impedance, buffer, instrumentation amplifier (IA), an 18-bit analog-to-digital converter (ADC) before returning to the FPGA for voltage measurement. These studies were performed over the frequency range of 1 Hz to 100 MHz The results indicate that the BHCS maintains high \(Z_O\) over a wider frequency bandwidth compared to the IHCS, making it better suited for our proposed system, despite that fact that the IHCS has better voltage compliance and lower power dissipation. Finally, the NPD demonstrates that the system is well-
designed from a noise perspective. For hardware implementation as a test bench, we designed the printed circuit board (PCB) for a single channel out of thirty-two channel current source for the new EIT system.
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Contents

Abstract ........................................................................................................................................ ii
Acknowledgments ...................................................................................................................... iv
List of Figures ............................................................................................................................... vii
List of Tables ................................................................................................................................. viii
Chapter 1 Introduction .................................................................................................................. 1
  1.1 New Approach ..................................................................................................................... 6
  1.2 Goal ................................................................................................................................... 7
Chapter 2 Background .................................................................................................................. 9
  2.1 Howland Current Source (HCS) ...................................................................................... 9
  2.2 Basic Howland Current Source (BHCS) .......................................................................... 10
  2.3 Effect of Resistance Mismatches .................................................................................... 12
  2.4 Improved Howland Current Source (IHCS) .................................................................. 13
  2.5 Output Impedance ........................................................................................................... 15
  2.6 Single Electrode System .................................................................................................. 16
  2.7 Noise Power Density (NPD) .......................................................................................... 17
Chapter 3 Simulation Analysis and Comparison ...................................................................... 18
  3.1 Gain Calculation of BHCS ............................................................................................. 18
  3.2 Gain Calculation for IHCS .............................................................................................. 19
  3.2.1 Voltage Compliance (VC) of IHCS ........................................................................ 22
  3.2.2 Theoretical Calculation of VC for IHCS ................................................................. 24
  3.2.3 Simulation Results of VC for IHCS ....................................................................... 25
  3.2.5 Simulation Analysis of IHCS for RO .................................................................... 30
Chapter 4 Noise Analysis ............................................................................................................ 51
  4.1 NPD for Single Electrode System .................................................................................... 52
  4.2 NPD Calculation for the ADC ....................................................................................... 62
Chapter 5 PCB for Single Electrode System .............................................................................. 66
  5.1 Prototype .......................................................................................................................... 67
  5.2 PCB Layers : 4 ................................................................................................................ 68
  5.2.1 Top Layer for Signal: ............................................................................................... 69
  5.2.2 Ground Layer ........................................................................................................... 70
  5.2.3 Power Layer ............................................................................................................. 71
  5.2.4 Bottom Layer for Signal ......................................................................................... 72
5.2.5  3D Diagram of PCB ................................................................. 73
Chapter 6 Conclusion ....................................................................... 74
References ...................................................................................... 76
List of Figures

Figure 1:1 General Diagram for EIT System................................................................. 2
Figure 1:2 Current Source of EIT System........................................................................ 3
Figure 1:3 Proposed New EIT System............................................................................... 6
Figure 2:1 Schematic Diagram of BHCS ......................................................................... 10
Figure 2:2 Norton Equivalent Circuit of BHCS.............................................................. 10
Figure 3:1 BHCS Test Circuit for Voltage Compliance.................................................... 20
Figure 3:2 Simulation Results of VC for BHCS............................................................... 22
Figure 3:3 IHCS Test Circuit for Voltage Compliance.................................................... 23
Figure 3:4 Simulation Results of VC for IHCS............................................................... 25
Figure 3:5 Test Circuit for Finding the Output Impedance of the BHCS......................... 26
Figure 3:6 Simulation Analysis of BHCS for RO............................................................. 27
Figure 3:7 Simulation Analysis of BHCS for CO............................................................ 28
Figure 3:8 Output Impedance Calculation of IHCS......................................................... 29
Figure 3:9 Simulation Analysis of Output Resistance RO.............................................. 30
Figure 3:10 Simulation Analysis of IHCS for CO........................................................... 31
Figure 3:11 Circuit Diagram for DC Analysis................................................................. 33
Figure 3:12 Simulation Results for Output DC............................................................... 34
Figure 3:13: Blocking DC with a Capacitor ................................................................... 35
Figure 3:14 Simulation Results for Output DC............................................................... 36
Figure 3:15 Simulation Analysis of Output Resistance RO with Variable Capacitors ...... 37
Figure 3:16 Simulation Analysis of Output Capacitance CO with Variable Capacitors ... 38
Figure 3:17 Single Electrode System with a 10 μF Capacitor......................................... 40
Figure 3:18 Simulation Results of Single Electrode System for RO with a 10 μF Capacitor 42
Figure 3:19 Simulation Analysis of a Single Electrode System for CO with a 10 μF Capacitor 43
Figure 4:1 Block Diagram of Single Electrode System for NPD .................................... 51
Figure 4:2 Schematic Diagram of Single Electrode System for NPD................................. 52
Figure 4:3 Transient Analysis of the Complete System.................................................. 54
Figure 4:4 NPD at the Input to the IA............................................................................ 56
Figure 4:5 NPD at the Output of the IA with a Capacitor.............................................. 57
Figure 4:6 NPD at the Output of the IA without a Capacitor........................................... 58
Figure 4:7 NPD at the Output of the IA with Gain of Eight............................................ 60
Figure 5:1: Schematic Diagram of Single Electrode System........................................... 67
Figure 5:2 Footprint of the Top Layer............................................................................. 69
Figure 5:3 Footprint of Ground Layer............................................................................ 70
Figure 5:4 Footprint of Power Layer............................................................................. 71
Figure 5:5 Footprint for Back Layer............................................................................. 72
Figure 5:6 3D Diagram................................................................................................. 73
List of Tables

TABLE 3:1 RESULTS OF OUTPUT RESISTANCE RO ................................................................. 28
TABLE 3:2 RESULTS OF OUTPUT CAPACITANCE CO .................................................................. 29
TABLE 3:3 RESULTS OF IHCS FOR RO .................................................................................. 30
TABLE 3:4: RESULTS OF IHCS FOR CO .................................................................................. 32
TABLE 3:5 RESULTS OF OUTPUT RESISTANCE RO WITH VARIABLE CAPACITORS .................................................. 37
TABLE 3:6 SIMULATION ANALYSIS OF BHCS FOR RO WITH VARIOUS CAPACITORS .................................................. 39
TABLE 3:7 RESULTS OF BHCS FOR RO WITH A 10µF CAPACITOR ........................................ 42
TABLE 3:8 SIMULATION RESULTS OF BHCS FOR CO WITH A 10µF CAPACITOR ............................. 44
TABLE 3:9 RESULTS OF BHCS WITH TWO CAPACITORS ...................................................... 48
TABLE 4:1 TRUTH TABLE OF TRANSPARENT GAIN MODE .................................................. 55
TABLE 4:2 NPD AT THE INPUT OF THE IA ............................................................................. 56
TABLE 4:3 NPD AT THE OUTPUT OF THE IA FOR THE GAIN OF ONE ...................................... 59
TABLE 4:4 RESULTS OF NPD AT THE OUTPUT OF THE IA FOR THE GAIN OF EIGHT ......................... 61
TABLE 4:5 TOTAL NPD FOR THE SYSTEM ............................................................................. 64
Chapter 1 Introduction

Electrical Impedance Tomography (EIT) is a simple, non-invasive, inexpensive and radiation-free medical imaging technology. In medical experiments, EIT has been used for studying gastric emptying, lung function, heart disease, water in the lungs and detecting breast malignancy and cysts. Of the above applications, lung imaging has turned into the most promising for EIT applications and has been the subject of many investigations. A major advantage of EIT for this application is that it enables continuous real-time monitoring of the lung function. [2-3]

Early investigations of EIT were reported over three decades ago. The technique is based on the measurement of the intrathoracic bioimpedance [4] distribution through the use of electrodes that are arranged in a circular ring on the surface of the patient's chest. A moderate frequency, very low magnitude current is applied to the chest by the successive pairs of electrodes in a type of EIT called Applied Potential Tomography (APT) [5].
In an alternate type of EIT called Adaptive Current Tomography (ACT), where current patterns are applied to all electrodes simultaneously. The ACT approach has been shown to provide greater sensitivity to changes in impedance. In both cases, a reconstruction algorithm is used to convert the measurements into a cross-sectional tomographic image of the impedance distribution within the chest [6]. In our proposed system, 32 electrodes will be used to detect changes in lung function and structure in cystic fibrosis patients.

Figure 1.1 shows the basic arrangement used for EIT where an array of electrodes is placed around a chest. A proper set of current patterns is applied to create an excitation in the electrodes on the object surface to generate an electromagnetic (EM) field within that object. Each current pattern has an individual value of the current for each electrode and the reconstruction algorithm uses the applied patterns and measures of the resulting voltages to solve the inverse problem and figure out the electrical conductivity and permittivity distributions in that object [7-8].
A limitation of EIT is that it has a poor spatial resolution. In mathematical terms, the reconstruction of the images is an ill-posed inverse problem, which means that large changes in the interior impedance distribution may produce only small changes in the surface voltages. Therefore, this technology requires high-precision instrumentation that can apply a desired current to the object and measure the output voltages of each electrode. EIT also requires precise knowledge of the shape of the object and the electrode placement [7-8].

Many current sources operate very well over a low-frequency bandwidth and present a large output impedance to the load. However, when the frequency band extends upward, the output impedance of the current source drops because of the stray shunt capacitance present in the circuit. Thus, the performance of the current source declines [8][10].

![Figure 1:2 Current Source of EIT System](image_url)
One of the most commonly used current sources in modern EIT systems is the Howland Current Source (HCS) because it is a simple, reliable and high-performance voltage controlled current source (VCCS) based on a single operational amplifier and a few resistors. It can be adjusted to produce high output resistance over a reasonable frequency range but leaves a non-zero output capacitance. In our analysis, we considered two techniques of HCS: basic Howland current source (BHCS) and improved Howland current source (IHCS). We also studied modified Howland sources that block the application of DC current. These methods are further discussed in Chapter 2 [8] [12].

In previous EIT studies, many approaches have been used to produce very high output impedance. One common approach is using a negative impedance converter (NIC) circuit, which can establish an adjustable negative capacitance that can be placed in parallel with the output of the current source. It is tuned to form a capacitance of equal intensity but opposite sign to cancel the output and stray capacitance associated with the current source. A drawback of the NIC is that it requires adjustment for the particular frequency being used since both the output capacitance and negative capacitance vary somewhat with frequency. It also has stability issues and may produce undesirable oscillations [1] [7].

Another method to compensate for capacitance uses a generalized impedance converter (GIC) circuit in parallel with the output of the current source to generate an inductance. It adjusts this inductance to build a parallel resonant circuit with the current source output capacitance at the operating frequency. This parallel LC resonant circuit will offer an infinite impedance at its resonant frequency cancelling the effect of the capacitance in the current source output impedance.
However, since it must be tuned to the operating frequency, it requires readjustment for each different frequency, in some cases requiring a change in components [1] [7].

The NIC and GIC circuits can deliver the desired compensating effect. The partnership of a GIC or NIC with a Howland circuit can produce remarkably large output impedances, but they require a comparably complex circuits, including switchable and flexible components [11-16].
1.1 New Approach

To establish a high output impedance over a wide frequency range, we examined numerous ways of making a voltage controlled current source (VCCS) for EIT applications. The HCS remains the best choice for the core of the VCCS but a new method is proposed for maintaining a high output impedance over a broad frequency range. In our proposed system, an adjusted current is applied by the HCS to compensate for current lost through the output impedance and any stray capacitance to ground. The result is that the desired output current flows into the load. This compensation is performed in the digital domain, making the analog hardware maintain low-complexity and be adjustment free.

Figure 1:3 Proposed New EIT System
In figure 1.3, the digital processor (FPGA) produces a proper sinusoidal signal with an accurate phase and amplitude. This signal then sent into the digital-to-analog converter (DAC) for transformation. The transformed analog signal is inserted into the VCCS (Howland Current Source) to generate the proper source current of \( I_s \) which helps to set the desired load current \( I_L \) plus the current in the output impedance \( I_O = \frac{V_L}{Z_O} \) in the system. Consequently,

\[
I_s = I_L + \frac{V_L}{Z_O} = I_L + I_O.
\]

The voltage created by this \( I_O \) will be processed by an analog-to-digital converter (ADC) and then fed into a digital processor (FPGA) in the system. This voltage is used to continuously update \( I_s \) and maintain the desired load current.

### 1.2 Goal

The motivation of this thesis is studying the analog circuitry used to implement the system in figure 1.3. Multiple variations of the Howland current source are simulated to measure the output impedance \( Z_O \), measured as \( C_O \) and \( R_o \) in the circuit. This methodology is further discussed in Chapter 2. The study was performed in two systems of HCS: BHCS and IHCS, and variations that used capacitors to block the production of a DC current, with the frequency range from 1 Hz to 1 MHz. The analysis further covers the voltage compliance, gain, and noise power density (NPD) of the circuits. For the simulation inquiry, the Cadence Capture CIS and Allegro PSpice Simulator
are used. Additionally, the noise power density (NPD) of the circuit is studied to ensure that the circuit is well-designed from a noise perspective, meaning that a particular component or components are not dominating the noise performance. Finally, for hardware implementation, we designed a printed circuit board (PCB) for a single electrode system of EIT using kiCAD software.
Chapter 2 Background

2.1 Howland Current Source (HCS)

Many applications such as instrumentation, medical equipment, and industrial process management applications involve low power current sources. In current source topologies, the VCCS produces a current that is proportional to an input voltage. There are many varieties of op-amp based VCCS are available, but Howland Current Source (HCS) is a good choice due to its simplicity and good performance.

Professor Bradford Howland of MIT invented an elemental version of HCS about 1962. HCS has become an essential part of EIT applications because of its stable signal-to-noise ratio and wide bandwidth. In this chapter, the background of Basic Howland Current Source (BHCS), Improved Howland Current Source (IHCS), the methodology for output impedance measurement, and Noise Power Density (NPD) will be discussed.
2.2 Basic Howland Current Source (BHCS)

The figure shows a basic Howland current source (BHCS) that applies current to a grounded load. Looking back from the load, the circuit looks like the resistance of $R_1$ to ground in parallel with a negative resistance converter that presents a grounded resistance of value $-R_2R_4/R_3$.

Figure 2:1 Schematic Diagram of BHCS

The figure illustrates the Norton Equivalent circuit of the BHCS and the overall output resistance of $R_o$ seen by the load using the following equation.

Figure 2:2 Norton Equivalent Circuit of BHCS
In a true current source system, output resistance must be infinity for ideal source behavior. This condition can be achieved by making the magnitude of the negative resistance $R_2 R_4 / R_3$ equal $R_1$, resulting in the four balanced resistors

$$\frac{R_4}{R_3} = \frac{R_1}{R_2}. \quad (2.2)$$

The output current becomes independent of $V_L$, when the above condition is met, meaning that

$$i_O = \frac{1}{R_4} V_1. \quad (2.3)$$

The gain of the converter can be calculated as

$$\frac{i_O}{V_1} = \frac{1}{R_4}. \quad (2.4)$$
Equation 2.4 gives the gain of the circuit and for $V_1 > 0$ the circuit will source current to the load, and for $V_1 < 0$ it will sink current. Voltage compliance ($V_L$) is the maximum range of load voltage ($V_O$) for which the circuit behaves as a current source. From figure 2.1, we can measure the $V_L$ as given below.

$$V_L = V_O \frac{R_3}{(R_3 + R_4)} = V_O \frac{R_3}{(R_1 + R_2)}.$$  \hspace{1cm} (2.5)

We can compute the voltage compliance assuming symmetric output voltage saturation ($V_{sat}$), which is the maximum output voltage of the op-amp given as (+VCC and -VEE) in figure 2.1, as

$$|V_L| \leq \frac{R_1}{R_1 + R_2} V_{sat}.$$  \hspace{1cm} (2.6)

### 2.3 Effect of Resistance Mismatches

In practical cases, the resistive bridge can be unbalanced because of resistance tolerance and this impact will degrade the output resistance $R_O$, resulting in non-ideal current source behavior. Non-ideal op amp characteristics also produce non-ideal current source behavior.
2.4 Improved Howland Current Source (IHCS)

The BHCS can be unnecessarily wasteful of power depending on the circuit conditions. An example illustrates this property. Let $V_1 = 1 \text{ V}$, $R_1 = R_3 = 1 \text{ k}\Omega$, and $R_2 = R_4 = 4 \text{ k}\Omega$ and suppose the load is such that $V_L = 5 \text{ V}$. From Eq (2.3), $i_{O} = 1 \text{ mA}$. It can be noted that the current through $R_1$ toward the left is $i_1 = V_L / R_1 = 5/1000 = 5 \text{ mA}$, indicated that the op-amp will waste 5 mA through $R_1$ to deliver the only 1mA to the load under these given conditions.

This problem can be avoided with IHCS, where the resistance of $R_2$ has been split into two parts, $R_{2A}$ and $R_{2B}$[12], such that the balanced condition is now

$$\frac{R_4}{R_3} = \frac{R_{2A} + R_{2B}}{R_1}. \tag{2.7}$$

![Figure 2.3 Schematic Diagram of IHCS](image)
The gain of the circuit can be calculated using the following equation:

\[ \frac{i_o}{V_1} = \frac{R_2}{R_1} / \frac{1}{R_{2B}}. \]  

(2.8)

The gain term is \( \frac{R_2}{R_1} \), and \( R_{2B} \) can be made as small as needed while the remaining resistance is kept high to avoid power losses. Let \( R_1 = R_3 = R_4 = 100 \, \text{k}\Omega \), \( R_{2B} = 1 \, \text{k}\Omega \), and \( R_{2A} = 100 - 1 = 99 \, \text{k}\Omega \). Here, \( i_o = 1 \, \text{mA} \) with an input \( V_1 = 1 \, \text{V} \). Here, for a 5 V load voltage, the current in \( R_1 \) is \( i_1 = V_L/(R_1 + R_{2A}) = (5)/(100000 + 99000) = 0.025\,\text{mA} \) that means it will waste only 0.025 mA current through \( R_1 \) to deliver 1 mA current in the load.

The voltage compliance is approximate \(|V_L| \leq |V_{\text{sat}}| - R_{2B} |i_o|\). By Eq (2.8), this can be written as

\[ V_L \leq |V_{\text{sat}}| - (\frac{R_2}{R_1}) |V_1|. \]  

(2.9)
2.5 Output Impedance

In our analysis, the output impedance \( Z_O \) is modelled as two parallel components - one resistor \( (R_O) \) and one capacitor \( (C_O) \) as presented in figure 2.4.

![Figure 2:4 Model for Output Impedance Calculation](image)

The capacitance \( (C_O) \) consists of the actual output capacitance of the source plus any additional stray capacitance. Similarly, the resistance \( (R_O) \) is the output resistance of the source in parallel with any other shunt resistance. The equations for \( R_O \) and \( C_O \) in terms of \( Z_O \) are given below:

\[
R_O = \frac{1}{Re\left(\frac{1}{Z_O}\right)}
\]

(2.10)

and

\[
C_O = \frac{Im\left(\frac{1}{Z_O}\right)}{2\pi f}.
\]

(2.11)

Where \( Re() \) denotes the real part, \( Im() \) denotes the imaginary part, and \( f \) is the frequency.
2.6 Single Electrode System

Figure 2.5 is a single channel in the EIT system, where the signal comes from a balanced-output digital to analog converter (DAC) and passes the signal through a difference amplifier. This difference amplifier is used to convert the balanced output from the DAC into a single ended voltage signal.

![Diagram of Single Electrode System](image)

The difference amplifier output goes to a BHCS making the desired output load current flow into the load. The resulting voltage will pass through the buffer and instrumentation amplifier for amplification. The amplified signal then again passes into an analog to voltage converter (ADC) for conversion. The electronics for this single channel will be analyzed in the later chapters.
### 2.7 Noise Power Density (NPD)

Electronic devices introduce noise into a circuit, which can be represented in terms of a noise power spectral density (NPD). Information about this NPD is available from the datasheets. An ADC or DAC introduces quantization noise ($\sigma_q^2$) which is often assumed to be white, i.e. has a NPD that is flat over the frequency range from $-\frac{f_s}{2}$ to $\frac{f_s}{2}$, where $f_s$ is the sampling frequency, as shown in figure 2.6. The total quantization noise power is obtained by integrating power noise density over the range of $-\frac{f_s}{2}$ to $\frac{f_s}{2}$ [22]. It can be shown that the total quantization noise power is

$$\sigma_q^2 = \Delta^2 \frac{1}{12},$$

where $\Delta$ is the quantization step size $= \frac{A}{2^n}$ and $A$ is the full range of analog signal to be digitalized and $n$ is the number of bits per sample. The NPD is

$$\text{Noise Power Density} = \frac{\sigma_q^2}{f_s} = \frac{\Delta^2}{12} \frac{1}{f_s} \frac{1}{2}$$

(2.12)

![Diagram of Noise Power Density](image)

Figure 2:6 Uniform Distribution of $P(f)$ and $\sigma_q^2$
Chapter 3 Simulation Analysis and Comparison

The aim of this chapter is to analyze the gain, voltage compliance (VC), and output impedance ($Z_O$) of the Basic Howland Current Source (BHCS) and Improved Howland Current Source (IHCS). Variations on these sources that prevent them from applying a DC current are also analyzed. The evaluation further considers the electronics for a single electrode in a thirty-two-electrode system that uses the BHCS. The electronics for each electrode can deliver the desired current and measure the resulting voltage. The evaluation will help to validate which methods are best for our proposed EIT system.

3.1 Gain Calculation of BHCS

Consider a BHCS that uses the component values shown in figure 2.1. From equation (2.4), we can calculate the gain for the BHCS as

$$\frac{1}{R_4} = \frac{1}{4k\Omega} = 0.25 \frac{\text{mA}}{\text{V}}.$$  (3.1)
3.2 Gain Calculation for IHCS

An IHCS constructed using the component values shown in figure 2.3 has the same gain, as can be seen from equation (2.8)

\[
\frac{R_2/R_1}{R_{2B}} = \frac{1k\Omega/8k\Omega}{0.5k\Omega} = 0.25 \frac{\text{mA}}{V}.
\]  

(3.2)

By using the same gains for each circuit, we can fairly compare their voltage compliance (VC) and output impedance \((Z_o)\).

3.1.1 Voltage Compliance (VC) of BHCS

Figure 3.1 shows the test circuit for evaluating the voltage compliance of the BHCS. A maximum input voltage \(V_{in} = 5V\) is applied to the BHCS. The op amp is the Analog Devices AD8033 [20].
3.1.2 Theoretical Calculation of VC for BHCS

To meet the balance resistance condition for the Howland current source from equation (2.2) we assumed $R_1 = R_4 = 4 \, \text{k}\Omega$, $R_2 = R_3 = 1 \, \text{k}\Omega$, and used a variable $R_L = R_{\text{var}}$ in the BHCS system. From equation (2.6), we can compute the voltage compliance as
\[
\frac{R_1}{R_1+R_2} \times (-5V) + \frac{R_2}{R_1+R_2} \times (V_i) \leq \frac{R_1}{R_1+R_2} \times (5V) \frac{R_2}{R_1+R_2} \times (V_i).
\]

For \( V_i \) in the range of \( \pm 5V \)

\[
\frac{R_1}{R_1+R_2} \times (-5V) + \frac{R_2}{R_1+R_2} \times (V_i) \leq \frac{R_1}{R_1+R_2} \times (5V) \frac{R_2}{R_1+R_2} \times (V_i)
\]

\[-3 \leq V_L \leq 3.\]

### 3.1.3 Simulation Results of VC for BHCS

In figure 3.2, the \( R_{val} \) varies from \( 1k\Omega \) to \( 5k\Omega \) in \( 1k\Omega \) steps. For values \( 3k\Omega \) and above, the output voltage is distorted showing that Howland current source is not working as a current source anymore as it cannot supply the desired current. The output voltage values become increasing non-linear with further increases in the load resistance, with the output voltage clipped at \( 3V \) in the simulation results.
3.2.1 Voltage Compliance (VC) of IHCS

In this analysis, we have taken five resistors of $R_1, R_{2A}, R_{2B}, R_3, R_4$ and one load resistor of $R_L$. $R_2$ is basically divided into $R_{2A}$ and $R_{2B}$ in the circuit.
To balance the resistances as given in equation (2.7), we assumed $R_1 = R_4 = 8 \, \text{k}\Omega$, $R_2 = R_3 = 1 \, \text{k}\Omega$, where $R_2 = R_{2A} + R_{2B} = 0.5 \, \text{k}\Omega + 0.5 \, \text{k}\Omega$, and used a variable load resistor $R_L = R_{\text{var}}$. Here, $R_{\text{var}}$ is considered from $1\,\text{k}\Omega$ and $5\,\text{k}\Omega$ at $5V (V_{in})$. For theoretical calculation of VC for IHCS, we have used equation (2.9).
3.2.2 Theoretical Calculation of VC for IHCS

The voltage compliance can be written as follows:

\[-5 + \left( \frac{R_2}{R_1} \times V_i \right) \times \left( \frac{R_1+R_{2B}}{R_1+R_2} \right) \leq V_L \leq 5 + \left( \frac{R_2}{R_1} \times V_i \right) \times \left( \frac{R_1+R_{2B}}{R_1+R_2} \right)\]

For the resistor values used,

\[-5 + \left( \frac{1k}{8k} \times V_i \right) \times \left( \frac{8k+0.5k}{8k+1k} \right) \leq V_L \leq 5 + \left( \frac{1k}{8k} \times V_i \right) \times \left( \frac{8k+0.5k}{8k+1k} \right)\]

\[-5 + (0.125 \times V_i) \times (0.94) \leq V_L \leq 5 + (0.125 \times V_i) \times (0.94)\]

\[-4.7 + 0.117 \times V_i \leq V_L \leq 4.7 + 0.117 \times V_i\]

If \( V_i = \pm 5V \),

\[-4.7 + 0.117 \times (+5V) \leq V_L \leq 4.7 + 0.117 \times (-5V)\]

\[-4.115 \leq V_L \leq 4.115.\]
3.2.3 Simulation Results of VC for IHCS

In figure 3.4, when the value of $R_{var}$ is 4kΩ and 5kΩ, the output voltage of the circuit is distorted for large $V_{in}$. At this point, the simulation results show that the IHCS is not working as a current source as it is unable to deliver the correct current to the load. The voltage values are clipped at around 4 V in the simulation results. From this analysis, we noted that voltage compliance of IHCS is better than BHCS and matches with the theoretical calculation results.

![Figure 3:4 Simulation Results of VC for IHCS](image-url)
3.1.4 Output Impedance ($Z_O$) of BHCS

To measure the output impedance ($Z_O$), we have grounded the input terminal of the current source and applied a sinusoidal voltage $V_{in} = 1V$ in place of the load resistance in the circuit. Using the applied voltage and measured current from the source, we are able to determine the output resistance ($R_O$) and output capacitance ($C_O$) of the circuit using the Pspice simulation. The test circuit is shown in figure 3.5.

Figure 3:5 Test circuit for finding the Output Impedance of the BHCS
3.1.5 Simulation Analysis of BHCS for $R_O$

In Figure 3.6, we observed that for the frequency range from 1 kHz to 100 kHz the output resistance is high and measured around 25 MΩ. However, when the frequency increases more, the overall resistance starts to decrease. Eventually, at 1 MHz the output resistance measured as 5.02 MΩ.

![Figure 3.6 Simulation Analysis of BHCS for Ro](image)
Table 3:1 Results of Output Resistance $R_O$

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_O$</td>
<td>25.46 MΩ</td>
<td>25.45 MΩ</td>
<td>24.47 MΩ</td>
<td>5.023 MΩ</td>
</tr>
</tbody>
</table>

### 3.1.6 Simulation Analysis of BHCS for $C_O$

Figure 3.7, we observed that the output capacitance measured a constant 6.25 pF over the 1 kHz to 1 MHz frequency range.

![Figure 3:7 Simulation Analysis of BHCS for $C_O$](image)
Table 3.2 Results of Output Capacitance ($C_O$)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
</table>

3.2.4 Output Impedance of IHCS

The output impedance of the IHCS is measured in the same way as for the BHCS, as shown in [Figure 3.8 Output Impedance Calculation of IHCS](#).
3.2.5 Simulation Analysis of IHCS for $R_O$

Figure 3.9 shows the measured output resistance ($R_O$), which is somewhat different than for the BHCS. We observed that at low frequency $R_O$ at 1 kHz to 100 kHz is 16.728 MΩ which is the lower than for the BHCS. Finally, at 1 MHz, the output resistance decreased at 7.846 MΩ.

![Figure 3:9 Simulation Analysis of Output Resistance ($R_O$)](image)

Table 3:3 Results of IHCS for $R_O$

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_O$</td>
<td>16.728 MΩ</td>
<td>16.726 MΩ</td>
<td>16.54 MΩ</td>
<td>7.846 MΩ</td>
</tr>
</tbody>
</table>
3.2.6 Simulation Analysis of IHCS for $C_O$

Figure 3.10 shows the measured output capacitance, which remains at a constant value of about 9.52 pF from 1 kHz to 1 MHz.
Table 3.4: Results of IHCS for $C_0$

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_0$</td>
<td>9.52pF</td>
<td>9.52pF</td>
<td>9.52pF</td>
<td>9.52pF</td>
</tr>
</tbody>
</table>

The conclusion from the above analysis is that BHCS is suitable for our proposed system because BHCS is giving higher output resistance and lower output capacitance for the frequency range from 1 kHz to 1 MHz

### 3.3 Output Direct Current

The purpose of this analysis is to measure the direct current (DC) at the Howland source output due to the offset voltage and bias current in the op-amp. For this analysis, we have grounded the input terminal of the current source and used transient analysis of the PSpice simulator.
3.3.1 Simulation Analysis for DC

The simulation results shown in figure 3.12 indicate that we are getting about 1.25µA DC current at the output of the current source. But the load of the circuit is going to be a human body, so we do not want any dc to flow into the human body. If a DC voltage was applied to the input of the current source, the output DC current would increase further. In this case, we need to block this DC from flowing in the load.
3.3.2 Blocking Capacitor

One way to prevent any DC in the load is to use a blocking capacitor in the circuit. If this capacitor was inserted in series with the load, DC current from the current source would tend to charge the capacitor over time until the voltage compliance of the source was exceeded. Instead, a capacitor can be inserted into the source, effectively making its DC gain zero. For this analysis, we have used $C_1 = 1\mu F$ inserted as shown in figure 3.13.
3.3.3 Simulation Analysis for DC with a capacitor

As demonstrated by figure 3.14, the DC current dropped to about 1.12pA after inserting the capacitor in the circuit. This analysis has helped us to figure out that using a capacitor is useful for the system. Now we will find out the appropriate capacitance value for the proposed system.
3.3.4 Simulation Analysis of BHCS for $R_O$ with Various Capacitors

In this examination, we varied the capacitor values, using 1µF, 3µF, 5µF, 7µF, and 10µF, to study the impact on the output resistance and capacitance. We noted a significant variation while changing the value of the capacitor. The output resistance ($R_O$) for 1µF measured 161.074 kΩ for 1kHz and started increasing while frequency increased. At 1 MHz we measured 5.239 MΩ. For 3µF, 5µF, 7µF the low frequency $R_O$ increased with increasing capacitor value. Finally, we observed that for 10µF capacitor value we are getting very high $R_O$ from 1kHz to 1 MHz. The measured values are shown in table 3.5.

![Figure 3:14 Simulation Results for Output DC](image)
Figure 3.15 Simulation Analysis of Output Resistance $R_O$ with Variable Capacitors

**Table 3.5 Results of Output Resistance ($R_O$) with Variable Capacitors**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1 kHz</th>
<th>10 kHz</th>
<th>100 kHz</th>
<th>1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_O$(1µF)</td>
<td>161.074kΩ</td>
<td>10.021kΩ</td>
<td>28.384MΩ</td>
<td>5.2392MΩ</td>
</tr>
<tr>
<td>$R_O$(3µF)</td>
<td>1.3537MΩ</td>
<td>10.407MΩ</td>
<td>25.744MΩ</td>
<td>5.0957MΩ</td>
</tr>
<tr>
<td>$R_O$(5µF)</td>
<td>3.4360MΩ</td>
<td>22.608MΩ</td>
<td>25.231MΩ</td>
<td>5.0957MΩ</td>
</tr>
</tbody>
</table>
### Table 3.6: Values of Resistances

<table>
<thead>
<tr>
<th>$R_O(7\mu F)$</th>
<th>5.9569MΩ</th>
<th>24.647MΩ</th>
<th>25.013MΩ</th>
<th>5.0957MΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_O(10\mu F)$</td>
<td>8.5407MΩ</td>
<td>25.195MΩ</td>
<td>24.892MΩ</td>
<td>5.0957MΩ</td>
</tr>
</tbody>
</table>

#### 3.3.5 Simulation Analysis of BHCS for $c_o$ with Various Capacitors

For output capacitance ($C_O$) measurement from 1kHz to 1MHz, we observed that for 1µF capacitor we get a very high $C_O$ compared to other capacitor values of 3µF, 5µF, 7µF, and 10µF. But we want a low $C_O$ for the system. A 10µF capacitor gives the best $C_O$. The measurements for $C_O$ shown in the given figure 3.16 and mentioned in table 3.6.

![Figure 3:16 Simulation Analysis of Output Capacitance ($C_O$) with Variable Capacitors](image-url)
From the above analysis, we concluded that $C_{val} = 10\mu F$ gives high output resistance and low output capacitance value for the frequency range of 1kHz to 1 MHz. We also observed that the larger the capacitor value, the better the low frequency behavior. But we could not extend the capacitance value over $10\mu F$ because, in the practical case, $10\mu F$ is the largest ceramic capacitor available in a reasonable surface mount package. Hence, this is our final $C_{val}$ for our proposed system from this analysis.
3.4 Single Electrode Electronics (SEE) with a 10µF Capacitor

Figure 3.17 presents the electronics for a single electrode in a thirty two channel EIT system. As was shown in figure 2.5, this system includes a difference amplifier, BHCS, buffer, and instrumentation amplifier (IA). The circuit which delivers the desired current to the specified load and measures the voltage that is produced. In this system, the voltage source $V_0 = 5V$ is applied in the load terminal of BHCS that uses a capacitor value of $C_{val} = 10 \text{ µF}$ to measure the $R_O$ and $C_O$ of the comprehensive circuit.

![Diagram of Single Electrode System with a 10 µF Capacitor](image)

Figure 3:17 Single Electrode System with a 10 µF Capacitor
In this interpretation, we expect to receive the high output resistance for the frequency range of 1 kHz and 1 MHz because our proposed system will be working on this spectrum. For output capacitance, we are demanding as low as possible.

### 3.4.1 Simulation Analysis of the SEE for $R_O$ with 10µF Capacitor

In figure 3.18, we observed that at 1 kHz, the output resistance value reached up to almost 832 kΩ. At 10 kHz and 100 kHz, it extended approximately up to 878 kΩ and 877 kΩ, respectively. Eventually, at 1 MHz the output resistance value subsided and reached approximately 760 kΩ. We compared the two measured results of $R_O$ for SEE and BHCS alone, and found out that SEE is giving lower $R_O$ because of the 1 MΩ resistor near the input to the voltage buffer. This resistor is needed to provide DC bias current to the op amps.
Figure 3: 18 Simulation results of Single Electrode System for \( R_O \) with a 10\(\mu\)F Capacitor

Table 3: 7 Results of BHCS for \( R_O \) with a 10\(\mu\)F Capacitor

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_O )</td>
<td>832 k(\Omega )</td>
<td>878 k(\Omega )</td>
<td>877k(\Omega )</td>
<td>760k(\Omega )</td>
</tr>
</tbody>
</table>
3.4.2 Simulation Analysis of SES for \( C_O \) with a 10µF Capacitor

We want the output capacitance as small as possible in the process. In figure 3.19, at 1 kHz the capacitance is - 627 pF and started increasing (towards zero) when the frequency increased. At 1 MHz the capacitance is 6.27pF. We also noted that the output capacitance \( (C_O) \) is nearly same as the BHCS alone for 10µF capacitor in Table 3.6 and 3.8.

Figure 3.19 Simulation Analysis of a Single Electrode System for \( C_O \) with a 10µF Capacitor
Table 3.8 Simulation Results of BHCS for $C_O$ with a 10µF Capacitor

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_O$</td>
<td>-627 pF</td>
<td>-66 fF</td>
<td>6.2pF</td>
<td>6.2pF</td>
</tr>
</tbody>
</table>

3.5 BHCS Analysis with Two Capacitor

In this analysis, we tried to use two capacitors in the system to balance the resistance ratio for BHCS system. In the previous analysis, using one capacitor is unbalancing the resistance ratio of the circuit, giving low output impedance at the lower frequency spectrum. By using two capacitors, we are trying to balance the resistance ratio to improve the output impedance at low frequencies while also blocking the DC. Figure 3.20 shows the circuit with two capacitors.
We know from equation (2.2), that the balance resistor ratio for BHCS is

\[
\frac{R_4}{R_3} = \frac{R_1}{R_2}.
\]

In this case, one pair of resistors are replaced with a series resistors and capacitors and we can write the new balance equation as

Figure 3:20 BHCS with two Capacitors
\[
\frac{R_1}{R_2} = \frac{R_1 + \frac{1}{SC_2}}{R_2 + \frac{1}{SC_1}}.
\] (3.3)

Now,

\[
R_1C_2(1+SR_2C_1) = R_2C_1(1+SR_2C_1)
\] (3.4)

Which reduces to

\[
R_1C_2 = R_2C_1
\] (3.5)

For the values given in figure 2.5, we find that

\[
C_2 = \frac{R_2}{R_1} C_1 = \left(\frac{1k\Omega}{4k\Omega}\right) \times (10\mu F) = \frac{10\mu F}{4} = 2.5 \mu F
\] (3.6)
In equation (3.5), we solved the resistance balanced ratio and find out the balance capacitor value of $C_2 = 2.5\mu F$ for this particular system. This approach allows one capacitor $C_1$ to block the DC output from the circuit and $C_2$ to maintain the appropriate ratio for high output impedance.

In this analysis, we used a $10\mu F$ capacitor to compensate for the low output impedance $Z_O$ in BHCS. In this way, we can get a high output impedance $Z_O$ for both low and high frequency spectrum. We have applied $V_3 = 1V$ in the load terminal of the circuit. The capacitors of $C_1 = 10\mu F/4 = 2.5\mu F$ (eq 2.13) and $C_2 = 10\mu F$ is inserted as shown in figure 3.20.

### 3.5.1 Simulation Analysis of BHCS for $R_O$ with two Capacitors

In figure 3.21 we see the output resistance when using the two capacitors, now we note that at low frequency output resistance $R_O$ is high. The results are approximately similar to BHCS without a capacitor. We can use this approach to block any DC in the circuit as well as compensate the output impedance at low frequencies.
Figure 3.21 Simulation Results of BHCS for $R_o$ with two Capacitors

Table 3.9 Results of BHCS with two Capacitors

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_o$</td>
<td>25.87 MΩ</td>
<td>25.86 MΩ</td>
<td>24.85 MΩ</td>
<td>5.06 MΩ</td>
</tr>
</tbody>
</table>
3.5.2 Simulation Analysis of BHCS for $C_O$ with two Capacitors

We note from figure 3.22 that, from frequency 1 kHz to 1 MHz, we are getting very low output capacitance in the system.

**Figure 3.22 Simulation Result of BHCS for $C_O$ with two Capacitors**
Table 3.10 Results of BHCS for $C_o$ with two Capacitors

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1kHz</th>
<th>10kHz</th>
<th>100kHz</th>
<th>1MHz</th>
</tr>
</thead>
</table>

From the above analysis, we noted that the output impedance at low frequencies is similar to that for the BHCS without a capacitor. That means that two capacitors are helping to block DC and improving the output impedance at low frequency spectrum.
Chapter 4 Noise Analysis

In our design, we use mixed-signal devices, including a 16-bit Digital-to-Analog Converter (DAC) and an 18 bit Analog-to-Digital Converter (ADC) and analog components. The digital interfacing devices, the DAC and ADC, introduce quantization noise [22] while the analog components introduce thermal and 1/f noise. Hence, the noise can be characterized in terms of noise power density (NPD) in the system. In this chapter, we are using a combination of PSpice and analysis to evaluate noise behavior for BHCS, IHCS, a 16 bit DAC (LTC1668, 24MSPS), and an 18-bit ADC (AD4002, 1.2 MSPS) so that we can determine whether the system is well-designed from a noise perspective and to see if a particular component is overly limiting the noise performance.

Figure 4:1 Block Diagram of Single Electrode System for NPD
4.1 NPD for Single Electrode System

Figure 4.2 shows the electronics for a single electrode in a thirty-two electrode EIT system. This circuit consists of a Difference Amplifier (Diff Amp), load resistance $R_{30}$, a Basic Howland Circuit with a capacitor, voltage buffer, and Instrumentation Amplifier (IA). This system generates the desired current in the specified load and measures the voltage that is produced in the system. For NPD analysis, we need to consider the overall system performance from the input signals to the output voltage. A transient analysis is used to first verify that the system is working properly.

![Figure 4:2 Schematic Diagram of Single Electrode System for NPD](image-url)
In our proposed system, two input current sources $I_1$ and $I_2$ are used to model the complementary DAC current outputs. $I_1$ and $I_2$ are opposite in sign but equal in magnitude. For the simulation, the sinusoidal input current sources are set to have amplitudes of $I_1 = 5 \text{ mA}$ and $I_2 = -5 \text{ mA}$. These two currents are converted into voltages using two resistors of $R_{24} = R_{28} = 52.3 \Omega$ and the results are fed into the difference amplifier in the circuit. This difference amplifier is the recommended design according to the manufacturer of the DAC (LTC1668) datasheet [18].

While doing the transient analysis for NPD calculation, we are looking at the output voltage on the load of the Howland Circuit which is $R_{30} = 1 \text{ k}\Omega$ as well as the voltage at the instrumentation amplifier’s load of $R_{29} = 1 \text{ k}\Omega$. The DC voltage of $V_3 = 2.5 \text{ V}$ applied in the buffer to bias the output at 2.5 V for ADC

4.1.1 Transient Analysis

The transient analysis will help to determine if the circuit is working properly according to the given input currents for the system. Figure 4.3 gives the output voltage on the load $R_{30} = V(R1:2)$ and instrumentation amplifier $R_{29} = V(VOUT)$ and are as we expected. The voltage on the load (bottom, red) has no DC component. The instrumentation amplifier’s output voltage is centered at 2.5 V in figure 4.3 as we assumed. This simulation verified that the circuit is functioning as expected.
4.1.2 AC Noise Analysis

The transient test affirmed that the system is performing as expected. Now, we will determine the NPD of the comprehensive system. For a high precision current source, it is highly important to make sure that the analog circuits are not creating so much noise that the least significant bits are meaningless with a high-resolution ADC and DAC. For noise density study, we performed the ac sweep/noise evaluation in PSpice, and the noises studied over the frequency range of 1 kHz to 100 MHz to examine the overall noise in the structure.
4.1.3 NPD at the IA

From figure 4.2, we evaluate the total noise at the IA input (pin 10) without a capacitor in the system. The total noise at the IA output is also measured with and without a capacitor in the system. The gain of the IA affects the noise at its output. The values of gain will be determined according to the logic input values of $A_0$ and $A_1$. A truth table relating the logic levels to the gain is given in Table 4.1.

Table 4:1 Truth Table of Transparent Gain Mode

<table>
<thead>
<tr>
<th>$\overline{WS}$</th>
<th>$A_0$</th>
<th>$A_1$</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-V_s$</td>
<td>Low</td>
<td>Low</td>
<td>1</td>
</tr>
<tr>
<td>$-V_s$</td>
<td>Low</td>
<td>High</td>
<td>2</td>
</tr>
<tr>
<td>$-V_s$</td>
<td>High</td>
<td>Low</td>
<td>4</td>
</tr>
<tr>
<td>$-V_s$</td>
<td>High</td>
<td>High</td>
<td>8</td>
</tr>
</tbody>
</table>

The table shows that when $A_0$ and $A_1$ are low the instrumentation amp presents a gain of 1. When both input levels are high it offers the gain of 8. Other conditions still established for one low and one high which showed the gain value of 2 and 4. The simulation results are discussed below.
4.1.4 NPD at the Input to the IA

Figure 4.4 shows the NPD at the input to the IA and it emphasizes that from 1 kHz to 1 MHz the NPD remains constant at \(0.519 \frac{fV^2}{Hz}\). After that, it starts falling off and eventually reaches \(0.320 \frac{fV^2}{Hz}\) at 10 MHz.

Table 4:2 NPD at the input of the IA

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1KHz (\frac{fV^2}{Hz})</th>
<th>10KHz (\frac{fV^2}{Hz})</th>
<th>100KHz (\frac{fV^2}{Hz})</th>
<th>10MHz (\frac{fV^2}{Hz})</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPD at the input of the IA</td>
<td>0.52 (\frac{fV^2}{Hz})</td>
<td>0.52 (\frac{fV^2}{Hz})</td>
<td>0.52 (\frac{fV^2}{Hz})</td>
<td>0.32 (\frac{fV^2}{Hz})</td>
</tr>
</tbody>
</table>
4.1.5 NPD at the output of the IA with and without a Capacitor

For the ADC, it is the noise at the output of the IA that matters. Figures 4.5 and 4.6 show the NPD at the output of the IA which is also the input to the ADC. For figure 4.2, a 10 µF capacitor is used in the BHSC between two resistors of $R_1$ and $R_2$ in the system. A voltage probe is attached in $R_{29}$ of the IA to measure the total noise of the system. In figure 4.6, the analysis is completed without a capacitor. The simulation results are discussed below.

![Graph showing noise power density (NPD) at the output of the IA with and without a Capacitor.](image)

**Figure 4:5** NPD at the output of the IA with a Capacitor
Figure 4.6 NPD at the output of the IA without a Capacitor

Figure 4.5, we observe that the total output noise NPD drops at low frequencies due to the presence of the capacitor. But for both figures 4.5 and 4.6, the total NPD at 1 kHz is $1.605 \frac{fV^2}{Hz}$ and stays near that same value until near 1 MHz. At 6.26 MHz increases to $2.163 \frac{fV^2}{Hz}$. This increase in noise is altogether reliant on the gain of the IA (AD8251). At unity gain, the AD8251 exhibits significant gain peaking at 6.26 MHz and this peaking disappears at higher gains. This effect is described in the manufacturer’s datasheet for the AD8251 [21].
Table 4.3 NPD at the output of the IA for the Gain of One

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1KHz</th>
<th>10KHz</th>
<th>100KHz</th>
<th>6.30MHz</th>
<th>10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPD with a 10 µF Capacitor</td>
<td>$1.6048 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.605 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.605 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$2.167 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.412 \left( \frac{f V^2}{Hz} \right)$</td>
</tr>
<tr>
<td>NPD without Capacitor</td>
<td>$1.605 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.605 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.605 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$2.167 \left( \frac{f V^2}{Hz} \right)$</td>
<td>$1.363 \left( \frac{f V^2}{Hz} \right)$</td>
</tr>
</tbody>
</table>

4.1.6 NPD at the output of the IA for a Gain of Eight

The gain peaking is reduced at a higher gain. For the results in figure 4.7, $A_0$ and $A_1$ are high, meaning that the gain is 8.
In figure 4.7, we noted that for total NPD analysis for a gain of eight, the overall noise increased, and gain peaking is reduced. A simple analysis of the expected NPD at the IA output at 1 kHz shows that the increase with a larger IA gain is primarily due to the additional amplification of the input noise. Assuming that the internal IA noise remains the same as its gain is increased, we can calculate the output NPD as

\[
\text{NPD} = (\text{NPD at the IA input}) \times (\text{Gain})^2 + (\text{NPD at the IA output} - \text{NPD at the IA input})
\]

\[
= \left(0.52 \frac{\text{fV}^2}{\text{Hz}}\right) \times (8)^2 + \left(1.604 \frac{\text{fV}^2}{\text{Hz}} - 0.52 \frac{\text{fV}^2}{\text{Hz}}\right) = 34.36 \frac{\text{fV}^2}{\text{Hz}}.
\]
In this equation, the first product multiplies the NPD at the IA input at 1 kHz by the voltage gain squared. The gain squared is used because we are working with power and need the power gain. The difference term computes the noise contribution of the IA when its gain is unity as found from the earlier simulation. This theoretical calculation predicts an NPD of 34.36 $\frac{fV^2}{Hz}$ (at 1 kHz).

However, the actual simulation NPD measured 38.56 $\frac{fV^2}{Hz}$ (at 1 kHz) because the IA noise increases slightly with a higher gain. However, the increase in IA output noise with a higher gain is primarily due to the amplification of the input noise and not the increased noise of the IA itself.

**Table 4:4 Results of NPD at the output of the IA for the Gain of Eight**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1KHz</th>
<th>10KHz</th>
<th>100KHz</th>
<th>6.30MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPD with a 10 $\mu F$ Capacitor</td>
<td>38.56 $\frac{fV^2}{Hz}$</td>
<td>38.56 $\frac{fV^2}{Hz}$</td>
<td>38.54 $\frac{fV^2}{Hz}$</td>
<td>36.78 $\frac{fV^2}{Hz}$</td>
</tr>
</tbody>
</table>
4.2 NPD Calculation for the ADC

In our analysis for AD4002 (ADC:18 bit, 2 MSPS) [19], the maximum input voltage is $V_{in} = 5$ V and the sampling frequency is 1.2 MHz. The theoretical noise power density using equation (2.12) is

$$\text{Noise Power Density} = \left( \frac{5}{\sqrt{12}} \right)^2 \frac{1}{1.2 \text{ MHz}^2} = 0.606 \frac{\text{fV}^2}{\text{Hz}}.$$  

But for AD4002, the typical RMS noise is given 30.4 µV in the manufacturer data sheet. If the NPD is flat, the corresponding power noise density for this ADC using equation (2.12) is

$$\text{Noise Power Density} = \left( \frac{30.4 \times 10^{-6}}{\sqrt{12}} \right)^2 \frac{1}{1.2 \text{ MHz}^2} = 1.54 \frac{\text{fV}^2}{\text{Hz}}.$$  

The measured noise power density is larger than the theoretical noise power density for an 18-bit quantizer because of the noise contributions of the remainder of the ADC circuits.

4.3 NPD Calculation for the DAC

For LTC1668 (DAC: 16 bit, 50 MSPS) [18], the maximum output current is 5 mA and the sampling frequency is 24 MHz. The way to calculate NPD for the proposed system is discussed below. The input current values are $I_1 = 5mA$ and $I_2 = -5mA$ are converted into voltages by the resistors
\( R_{24} = 52.3\,\Omega \) and \( R_{28} = 52.3\,\Omega \). The NPD in terms of output current can be calculated using equation (2.12).

\[
\frac{\left(\frac{5\,mA}{2.16}\right)^2}{24\,MHz} = 4.042 \times 10^{-23} \frac{A^2}{Hz}.
\]

This current NPD is converted into a voltage NPD by the 52.3 \,\Omega resistors and fed into the difference amplifier which has a gain of

\[
\text{gain} = \frac{R_6}{R_5} = \frac{1\,k\Omega}{200\Omega} = 5 \frac{V}{V}
\]

for each current from the DAC. We are interested in finding the DAC noise contribution at the IA output, so we need to multiply by the gains around the loop, i.e.

\[
\text{Power Gain} = \left( \frac{\text{Total Diff Amp gain load resistance} \times (\text{Howland Circuit Gain} \times \text{load resistance}) \times (\text{Buffer Gain}) \times (\text{IA Gain})}{2} \right)^2
\]

\[
= \left( (2 \times 5 \times 52\Omega) \times \left( 0.25 \frac{mA}{V} \times 1\,k\Omega \right) \times (1) \times (1) \right)^2 = 16900 \frac{V^2}{A^2}
\]

Total NPD for DAC = (Output Current NPD \times \text{Power Gain})

\[
= \left( 4.042 \times 10^{-23} \frac{A^2}{Hz} \times 16900 \frac{V^2}{A^2} \right) = 0.0000683. \frac{fV^2}{Hz}
\]
This result shows the NPD at the output of the IA due to the quantization noise of the DAC. Table 4.5 summarizes the noise components at the IA output due to the DAC and the analog circuits as well as the ADC noise.

**Table 4:5 Total NPD for the system**

<table>
<thead>
<tr>
<th></th>
<th>IA (gain = 1)</th>
<th>ADC</th>
<th>DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$1.605 \frac{fV^2}{Hz}$ (at 1kHz)</td>
<td>$1.54 \frac{fV^2}{Hz}$</td>
<td>$0.0000683 \frac{fV^2}{Hz}$</td>
</tr>
</tbody>
</table>

From the above table, the addition of both IA and DAC NPD presents $1.6050683 \frac{fV^2}{Hz}$, where the DAC noise is almost insignificant compared to the analog circuit noise. Our preference would be for the total NPD at the IA output (ADC input) to be significantly lower than that of the ADC, making the ADC the limiting component in the system. Instead, we find that the NPDs are nearly the same ($1.54 \frac{fV^2}{Hz}$ vs. $1.605 \frac{fV^2}{Hz}$), resulting in the loss of approximately 0.5 bit of ADC precision.

However, the NPD at the IA output due to the 16-bit DAC is very low and does not significantly impact the overall noise performance. Because of this, we could use a 12-bit DAC instead of the 16-bit DAC without any loss in noise performance, resulting in a simpler circuit.
Furthermore, from the above results, we see that increasing the gain of the IA does not provide any benefit since it just increases the NPD at the output of the IA further above the ADC quantization noise. Hence, we can use a fixed, unity gain IA instead of a programmable gain IA.
In this chapter, the implementation of a printed circuit board (PCB) for the electronics for a single electrode is presented. For the PCB board design, we used the design tools KiCAD 5.0 [23] and Ultra-Librarian [24]. In this chapter, we will show what components we used and the board layout.

Figure 5.1 shows the schematic for the single channel implementation. In the schematic diagram, we have used the footprints of FPGA CMOD ARTIX, low noise linear regulator ADP7118 (analog +5V, -5V, +3.3V), and Reed Relay Switch.

The reason for using reed relay switches instead of solid-state switches because it has very low capacitance and on resistance which is both good for our proposed system. We also used high precision low noise voltage reference (ADR4550), SMA connector, capacitors and resistors in 0805 packages.
5.1 Prototype

The parts used for the design are:

- FPGA CMOD ARTIX 7[17]
- 16-bit DAC (LTC1668)[18]
- 18-bit ADC (AD4002)[19]
- Howland( AD8034)[20]
- IA (AD8251)[21]
- Linear Regulator(AD7118AUZ)[25]
- Voltage Reference (ADR4550)[26]
- Reed Relay Switch(9001- Coto technology)[27]
- Relay Controller(ULN2003LVDR)[28],
- Screw Connector(Phoenix Contact 1985836)[29]
- Radio Frequency Interconnector(ACX1976-ND)[30]
- Capacitors and Resistors (0805)

5.2 PCB Layers : 4

The PCB is designed using 4 layers allowing us to have power and ground layers as well as 2 layers for routing signals. Each layer is discussed below.
5.2.1 Top Layer for Signal:

This layer provided signal paths and contained all of the components. Some signal traces connected to the bottom layer, also a signal layer, using vias.

Figure 5:2 Footprint of the Top layer
5.2.2 Ground Layer

We used mixed signal devices in the board 16-bit DAC(LTC1668) and 18-bit ADC(AD4002). The ground plane is divided into two parts to separate the digital ground and analog ground on the board. We joined the two grounds at one location so that there are no potential differences between the two grounds and ground currents for the digital components do not go by analog components.

Figure 5:3 Footprint of Ground Layer
5.2.3 Power Layer

Because of mixed signal devices, this layer is designed to provide the digital supply of 5V and the two analog supplies of 5V,-5V to the components. The digital and analog supply voltages have been separated in a way that they do not cross-talk with each other.

Figure 5:4 Footprint of Power Layer
5.2.4 Bottom Layer for Signal

The purpose of the bottom layer and the top layer was for routing the signals, with vias are used to easily pass through into the board without creating any problem. Hence it helps to avoid transmission line effects and stray capacitance and inductance effects in the board.

Figure 5: Footprint for Back Layer
5.2.5 3D Diagram of PCB

The 3D Diagram will help to understand the actual features of the board. The board is ready to be sent for manufacturing. This design will be used for further analysis of the EIT current source in the future.

Figure 5:6 3D Diagram
Chapter 6 Conclusion

Electrical Impedance Tomography (EIT) is a simple, inexpensive, portable, non-invasive, ionizing radiation-free medical imaging technology. A lot of research has been going on in order to improve the performance of EIT current sources. This thesis describes analyses that helped to optimize the processing blocks for one type of new current source.

The goal for examining two versions of the Howland Current Source (HCS) - Basic Howland Current Source (BHCS) and Improved Howland Current Source (IHCS) - was to compare their output impedance $Z_O$ across the frequency range of interest. This work investigated the gain, voltage compliance, output impedance $Z_O$, and noise power density (NPD) of these two models with and without a capacitor. The purpose of using a capacitor is to prevent any direct current (DC) at the output of the system because the load is going to be a human body. The conclusion from these evaluations is that the BHCS maintains a high $Z_O$ over a wider frequency bandwidth compared to the IHCS, making it better suited for our proposed system, despite that fact that the IHCS has better voltage compliance and lower power dissipation.
Introducing a second capacitor into the BHCS provided DC blocking without a loss in output impedance at lower frequencies. The study further helped to discover the appropriate DC blocking capacitor value of 10µF. Finally, analyzing NPD helped to find out we could use a 12-bit DAC instead of 16-bit DAC, and using a unity gain low noise instrumentation amplifier (IA) instead of a programmable gain IA would be better for the proposed system.
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