Novel two-dimensional devices for future applications

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Novel Two-Dimensional Devices for Future Applications

by

Pratik Agnihotri

A Dissertation
Submitted to the University at Albany, State University of New York
in Partial Fulfillment of
the Requirements for the Degree of
Doctor of Philosophy

College of Nanoscale Science and Engineering
2016
Novel Two-Dimensional Devices for Future Applications

by

Pratik Agnihotri

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To my family
Acknowledgements

During the course of my research, I was fortunate to receive the support of numerous people who with their kindness and honest suggestions enlightened my intelligence.

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Abstract

The scalability of field effect transistor has led to the monumental success of complementary metal-oxide-semiconductor (CMOS) technology. In the past, device scaling was not the major issue to a greater extent. Recently with current technology nodes, transistor characteristics show signs of reduced performance due to short channel effects and other issues related to device scaling. Device designers look for innovative ways to enhance the transistor performance while keeping up with device miniaturization. Successful inventions include the development of tri-gate technology, gate all around (GAA) field effect transistors, silicon-on-insulator substrate, and high-k dielectrics. These developments have enabled the device scaling that we are experiencing today. To continue the device scaling beyond Si-based technologies, other creative methods have to be explored to achieve even higher device performances. In this work, we investigate device properties in novel two-dimensional materials, graphene and tungsten diselenide, which have the potential for future electronics.

Using unconventional electrostatic gating method, we create a graphene $p$-$n$ junction to study its switching behavior. Graphene, with its high mobility and other unique properties, has the potential for next generation devices but with the lack of a band gap, novel device concepts need to be developed to implement them in logic applications. At the charge neutrality point graphene has a finite conductance which prohibits the transistor from turning off, resulting in a poor ON-OFF current ratio compared to silicon MOSFETs. We utilize the angle-dependent charge transport property in graphene $p$-$n$ junction, which is analogues to geometrical optics, to enhance the OFF-state resistance. We demonstrate that by physically blocking the low-angle transverse modes, a high off-state resistance of nearly $1000k\Omega$ is attained with ON/OFF current ratio $\sim 100$, a relatively
large value compared to a standard graphene FET. The measured data fits very well with our mode blocking analysis where we analyze conduction using Landauer transport formalism.

The discovery of graphene has led to exploration of other 2D materials, including transition metal dichalcogenides (TMDs), which can also exist in a monolayer form. One of the reasons for the sudden interest in TMDs is due to the fact that graphene is gapless while TMDs are gapped, whose values are determined by the number of layers. A significant portion of this dissertation is dedicated to understanding electronic devices based on $p$-$n$ junctions in two-dimensional tungsten diselenide, which belongs to the family of TMDs. We demonstrate the first bipolar junction transistor (BJT) formed on WSe$_2$ with a very high current gain of $\sim 1000$. The method of doping is similar to how we formed the graphene $p$-$n$ junction. We further extend the BJT configuration to show phototransistor properties with decent photocurrent gain.

Finally, we discuss a new device that can dynamically reconfigure to provide multi-functionality. The reconfigurability is possible by using the gating technique we employ, and allows us to create one device which can operate in different modes. We demonstrate one such reconfigurable device controlled by three buried coplanar gates to perform rectification, switching and current amplification. We anticipate this research will lead to new architectures that take advantage of the reconfigurability to make more compact circuits.
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Chapter 1

INTRODUCTION

1.1 Beyond CMOS technology

CMOS technology has swiftly evolved over the last few decades to become an essential component of our daily lives. Electronic devices have greatly improved our method of communication and provided us with tools of higher computational power. To achieve higher performance at a lower cost we look for ways to pack more devices in a single chip. This requires reduction in the size of the device, which in technical language means shrinking the gate length of the transistor and the gate pitch. The semiconductor industry has worked efficiently by adopting ways to support Moore’s Law\(^5\), which states that in an integrated circuit the number of transistors doubles after every two years. The scaling of CMOS technology, which parallels the scaling of MOSFET transistor, has continued for the last several decades, but it is expected to slow drastically due to fundamental physical limits.

For some time, the common scaling limits based on predictions were lithography challenges (Hoeneisen et.al.\(^6\)) and the scaling of gate dielectric (Chenming\(^7\), Stathis et.al.\(^8\)). These barriers have been successfully overcome by employing more sophisticated lithography techniques, for example, immersion lithography\(^9\) and double patterning\(^10\). To address the issue of gate tunneling for less than 1nm thick gate dielectric, materials with higher dielectric constant (Gusev et.al.\(^11\), Wilk et.al.\(^12\)) are being explored to enhance the gate control while maintaining the same thickness of the dielectric. Moreover, the mobility of the channel is enhanced using stress engineering (Rim
et al.\textsuperscript{13}, Thompson et al.\textsuperscript{14}, Yang et al.\textsuperscript{15}). With these solutions in place it is believed that CMOS scaling process can reach below 10nm gate length but uncertainties remain below the 5nm node.

In device miniaturization scaling is required in all dimensions, not just in lateral dimensions. This means that even though the gate length reduces in size, the channel dimension perpendicular to the transport direction has to be reduced, also. While reducing the device dimension, the emphasis should also be placed on fundamental issues which degrade device performance. One such consequence of device scaling is short channel effects, which develops as the gate length reduces. The degrading effects in device characteristics with scaling are poor sub-threshold slope and drain induced barrier lowering (DIBL), which increases the off-state leakage current. DIBL is a very common short channel effect that occurs with device scaling. In long channel FETs, since the gate has a strong control over the channel, the effect of lateral electric field in causing DIBL with drain voltage is insignificant. With reduced channel length, the lateral electric field from the drain encroaches into the channel to bring down the potential barrier near the source. This causes the off-state leakage current to increase, along with the shift in the threshold voltage.

To mitigate the short channel effects, progress has been made with the introduction of high-k dielectrics\textsuperscript{16} and silicon-on-insulator\textsuperscript{17} substrates, which provide better gate control over the channel compared to bulk devices. Beyond these devices, 3D device architecture has been introduced with the introduction of tri-gate\textsuperscript{18} and gate all around\textsuperscript{19} (GAA) technology, where the gate wraps around the channel region that further reduce DIBL.

Although the scaling trend will continue for several more transistor nodes, the continued demand to shrink the device size raises a fundamental question on how far transistor scaling can continue. In this work, I explore ‘beyond CMOS’ materials and devices to replace Si based CMOS
technologies. This holistic approach requires understanding the physical properties of new materials, which with their unique properties require a completely different device architecture. This in turn will lead to new switching mechanisms based on a radically different principle than that used in conventional MOSFETs.

1.2 Materials in consideration

1.2.1 Graphene - Background

Graphene is a two-dimensional monolayer of carbon atoms which are arranged in a honeycomb fashion. Graphene is a single atomic planar version of graphite and can exist in other forms. Graphene, therefore, can be thought of as a building block for these other forms, which have different dimensionalities. When a graphene is completely wrapped onto itself, it forms 0D fullerenes; when rolled to form a tube, it makes a carbon nanotube (CNT), and when it is arranged in stacks it forms graphite\(^1\). Graphene has a 2D hexagonal arrangement of carbon atoms which are \(sp^2\) hybridized. The in plane carbon atoms form \(\sigma\) bonds, and above and below the plane they form \(\pi\) bonds. The \(p_z\) orbitals are perpendicular and have delocalized electrons which contribute to conduction. About the \(z\)-axis these \(p_z\) atomic orbitals have rotational symmetry and are indistinguishable. The advantage of conjugated \(\pi\) orbital level is that electrons are delocalized and hence they can travel long distances with reduced scattering. Thus graphite has very good in-plane conduction. When these two-dimensional layers are stacked together, the weak van der Waals forces keep them in place. Because these layers have weak interactions, one can extract a single layer and understand its conduction properties.
Graphene crystal structure has two atom basis set (typically called A and B) and is made of two interpenetrating triangular lattices as shown in Figure 1.1. We can write the lattice vectors as

\[ a_1 = \frac{a}{2} (3, \sqrt{3}), \quad a_2 = \frac{a}{2} (3, -\sqrt{3}) \quad \ldots \text{(1.1)} \]

Here \( a \approx 1.42 \text{ Å} \) is the distance between the nearest neighbor carbon atoms. In the reciprocal space the lattice vectors are written as

\[ b_1 = \frac{2\pi}{3a} (1, \sqrt{3}), \quad b_2 = \frac{2\pi}{3a} (1, -\sqrt{3}) \quad \ldots \text{(1.2)} \]
There are two inequivalent points at the corners of the Brillouin zone which are also called the Dirac points. These Dirac points are labelled $K$ and $K'$ and are written as

$$K = \left( \frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a} \right), \quad K' = \left( \frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a} \right) \quad \ldots \quad (1.3)$$

In real space the nearest neighboring vectors are given as

$$\delta_1 = \frac{a}{2} (1, \sqrt{3}) \quad \delta_1 = \frac{a}{2} (1, -\sqrt{3}) \quad \delta_1 = -a (1,0) \quad \ldots \quad (1.4)$$

The Dirac point is equivalent to the $\Gamma$ point in a semiconductor like GaAs, which is a direct band gap material.

The electronic band structure (energy dispersion relation) of graphene was discussed by Wallace\textsuperscript{20} who used a tight binding model for the 2D graphite lattice structure. Wallace considered the $2p_z$ electrons to determine the band energies of the 2D lattice. The rationale behind this approach is that in $sp^2$ bonding only three of the four valence electrons participate. These electrons form the hexagonal lattice and have no role in the formation of the low-energy conduction or valence band. The low-energy bands are basically formed using the $2p_z$ orbital electrons. The weak interaction between the adjacent layers result in a large spacing between them. As such these interactions are neglected in the analysis. Thus, the band structure due to the $2p_z$ (also called $\pi$ bonds) electrons dominate and they are of primary interest. It should be noted that in a unit cell there are two basis and hence two kinds of $\pi$ bands are expected \textit{i.e.} $\pi$ and $\pi^*$. The tight binding Hamiltonian for electrons in graphene is written with the consideration that only the nearest-neighbor hopping interaction is involved. We discuss here the band structure based on
the model developed by Datta\textsuperscript{21}. The band structure is calculated by solving the following matrix eigenvalue equation

$$E(\phi_0) = [h(\vec{k})](\phi_0) \quad \ldots (1.5)$$

Here $E$ is the energy eigenvalue, $k$ is the wavevector, $\phi_0$ is the prefactor from the atomic ansatz wavefunction (For complete description refer to Datta\textsuperscript{21}), $h(\vec{k})$ is a $2 \times 2$ matrix of the form

$$h(\vec{k}) = \begin{bmatrix} 0 & h_0 \\ h_0^* & 0 \end{bmatrix} \quad \ldots (1.6)$$

Here $h_0 = -t \left(1 + e^{i\vec{k} \cdot \vec{a}_1} + e^{i\vec{k} \cdot \vec{a}_2}\right)$ where $t$ is the nearest neighbor hopping energy. The eigenvalues are given as

$$E_{\pm}(k) = \pm t \sqrt{1 + 4 \cos k_y b \cos k_x a + 4 \cos^2 k_y b} \quad \ldots (1.7)$$

The positive sign is for the upper band ($\pi^*$) and the negative sign is for the lower band ($\pi$). Note that Equation 1.7 is symmetric around zero energy. Figure 1.2 shows the plot for Equation 1.7.

The two bands are degenerate at $K$ and $K'$, close to the Dirac point. Using $k = K + q$ we can expand the band structure close to $K$ or $K'$ to rewrite Equation 1.7 for $|q| \ll |K|$

$$E_{\pm}(q) \approx \pm h v_F |q| \quad \ldots (1.8)$$

Here $q$ is the momentum with respect to the Dirac point, and $v_F$ is the Fermi velocity given as $3ta/2 \hbar$. Here, unlike a gapped material, fermi velocity is independent of energy or momentum. Close to the Dirac point ($K$ and $K'$) the two bands have linear dependence on wavevector. The linear dispersion relation in graphene allows us to consider the electrons in graphene as Dirac
particles, which are relativistic particles with zero rest mass and the Fermi velocity which replaces the velocity of light. The conical linear bands meet at the two inequivalent points at $K$ and $K'$. 

In pristine undoped graphene the Fermi level (energy) lies at the intersection of these cones, which implies that at $T=0$ there should be no carriers present and the graphene should be insulating. At a finite temperature, the broadening of the Fermi distribution gives finite conductivity and gives rise to the minimum conductivity of graphene, which is given as $4e^2/h$. 

Figure 1.2: Energy dispersion relation of graphene [Reprinted with permission from Beenakker, Reviews of Modern Physics, 80 (4), 1337-1354, 2008. © 2008 American Physical Society]
Graphene exhibits ambipolar transport (both electron and hole conduction) as depicted in **Figure 1.3**. With a bias applied on a gate, the number density and polarity of carriers can be tuned to achieve very high carrier concentration approaching $10^{13}$ cm$^{-2}$.

![Figure 1.3: Transfer characteristic of graphene FET shows ambipolar conduction](image)

**Figure 1.3: Transfer characteristic of graphene FET shows ambipolar conduction [Reprinted with permission from Geim et.al.\(^1\), Nature Materials, 6 (3), 183-191, 2007. © 2007 Nature Publishing Group]**

### 1.2.2 Tungsten diselenide - Background

Tungsten diselenide is another two-dimensional material which belongs to a family of transition metal dichalcogenides (TMDs)\(^{23, 24}\). Until recently research was mainly focused on graphene but since graphene does not have a band gap the attention has shifted to gapped 2D materials. To explore alternative channel materials, it is necessary to explore other two-dimensional materials, besides graphene, which can exist in a monolayer form and provide ultra-thin body channel. These materials have very large band gaps and have high mobility\(^{25}\), and have the potential to reduce
short channel effects by allowing better gate electrostatic control over the channel\textsuperscript{26}. The chemical, mechanical, electrical, thermal and optical properties of TMDs have been extensively studied over the last few decades\textsuperscript{27} \textsuperscript{28} \textsuperscript{29}. The discovery of graphene allowed researchers to exploit the same methodology to further understand the fundamental properties of single-layer TMDs. This includes sample preparation using similar exfoliation technique used previously for graphene\textsuperscript{30}. The advantage of TMDs over graphene is that most TMDs have band gaps which range from 1-2eV\textsuperscript{31} [Zhao \textit{et.al.}\textsuperscript{32}], which are in the useful range for electronic applications.

TMDs have a typical chemical structure written as MX\textsubscript{2}, where M represents the transition metal atom (such as Mo, Zr, Ta, W) and X is for the chalcogen atom (such as Se, S, Te). In our work we focus on tungsten diselenide with a chemical formula WSe\textsubscript{2}.

![Figure 1.4: Crystal structure of WSe\textsubscript{2} (Reprinted with permission from Pospischil \textit{et.al.}\textsuperscript{3}, Nature Nanotechnology, 9 (4), 257-261, 2014. © 2014 Nature Publishing Group)]
Figure 1.4 shows the crystal structure of WSe$_2$ which has a hexagonal P6$_3$/mmc symmetry. It consists of a layer of W atoms sandwiched between two atomic layers of Se atoms. Thus there is repetition of Se-W-Se layers along the c-axis. Within the layers each tungsten atom forms covalent bond with six Se atoms and each Se atom is covalently bonded to three W atoms. Each tri-layer has weak van der Waals interaction which makes it possible to exfoliate WSe$_2$ into a monolayer form. WSe$_2$ has no dangling surface bonds which minimize interface effects. The charge transport exists within the layer and the interlayer transport is weaker.

The bulk WSe$_2$ is has an indirect band gap, which increases as the layer number decreases. In the single layer form, it becomes a direct band gap semiconductor. The direct band gap position is located at the K point in the band structure\textsuperscript{33}. There is no change in the band gap at the K point as the layer thickness increases.

Another relevant characteristic of WSe$_2$, which makes it a promising semiconducting material for future electronics, is its ability to provide both electron and hole conduction (ambipolar transport)\textsuperscript{34}. This property can be utilized to build field effect transistors ($p$-channel and $n$-channel) to perform switching operations like conventional CMOS.

1.3 Scope of the work

The objective of this research is to understand the device properties of novel 2D materials (graphene, WSe$_2$), which can potentially provide us a pathway for future high performance electronic devices, to meet the challenges associated with device scaling. The devices based on these new materials have the potential to either replace the current technology or complement it to work in conjunction with CMOS. This work is based on the belief that “$p$-$n$ junction is the building block for electronic devices”. We demonstrate the unique properties of graphene $p$-$n$
junction, which has no analogue in semiconductor devices. In a graphene transistor, the finite conductance at the charge neutrality point means that the transistor does not turn off. In Chapter 2, we provide a solution to increase the off state resistance by forming a graphene $p$-$n$ junction and using the unique angle-dependent transport properties. This is accomplished by using device designs to block the low-angle transverse modes at the junction. We demonstrate that by physically restricting the modes, an enhanced off-state resistance is achieved with an on-off ratio of 100, which is about an order of magnitude larger than in devices made without such designs.

The bipolar junction transistor was one of the first solid state electronic devices. It was introduced in the late 40s and brought revolution to the field of electronics. Understanding the transistor effect enables us to define modern electronics based on new materials. We demonstrate in Chapter 3 the first bipolar junction transistor (BJT) realized in two-dimensional WSe$_2$ with a very high current gain ($\beta \sim 1000$). We further extend the BJT device to create a WSe$_2$ phototransistor.

With continued trend in device miniaturization, an aggressive approach is required to further enhance device performances. Besides adopting new materials that can replace Silicon, a reconfigurable device may lead to new architectures. Extending the work on the TMD device, we demonstrate a reconfigurable device that can perform three different functions — rectification, switching and amplification — in Chapter 4

We summarize in Chapter 5 the overall conclusions drawn from the current research and discuss new challenges and potential future directions.
References


Chapter 2

ENHANCED OFF STATE RESISTANCE IN GRAPHENE PN JUNCTION

2.1 Introduction

Graphene is a two-dimensional sheet of carbon atoms where atoms are arranged in a honeycomb fashion. It has a linear energy dispersion relation with zero band gap and can be described by one spinor wavefunction with two different components\(^4\). With these characteristics graphene show interesting phenomena such as inhibition of backscattering\(^6\), Klein tunneling\(^7\), and focusing of electrons like rays in geometrical optics\(^1\). For electronic devices \(p-n\) junction is the building block. With unique properties of graphene, graphene \(p-n\) junctions are likely to behave differently than conventional semiconductor bulk \(p-n\) junctions. With the potential of graphene-based devices to replace CMOS technology, it is important to understand the transport properties in graphene \(p-n\) junctions.

High carrier mobility in graphene makes it a promising material for post CMOS electronics but it suffers from the minimum conductivity problem which limits its role to replace silicon technology. Graphene demonstrates ambipolar conduction where carrier profile switches from electron to hole or vice-versa at the Dirac point\(^8\). The Dirac point is the charge neutrality point where maximum resistance occurs. In conventional semiconductors below the threshold voltage, when fermi level is in the band gap, the semiconductors behave as insulators. But in the case of graphene, at the Dirac point, it has a finite conduction with minimum experimentally observed\(^9\) conductivity given approximately as \(\sigma_{\text{min}} = 4e^2/h\) and the transistor does not turn off. Due to this behavior there is
not a well-defined off-state in graphene FETs, which limits its use in electronic applications. We address this challenge by creating a graphene $p$-$n$ junction, using buried electrostatic gating techniques, and introducing a device design which can efficiently block the modes that approach the junction at low angles.

In classical mechanics, a particle is confined if the height of the potential barrier is higher than the energy of the particle. In quantum mechanics, on the other hand, quantum tunneling happens where for non-relativistic particle the wavefunction appears in the classically forbidden region. The transmission through this potential barrier decays exponentially with barrier height and width. But for particles in graphene the transmission has weak dependence on barrier height and has an angle dependency. This prompts us to investigate an interesting phenomenon called Klein tunneling where the transmission along the normal to the junction is perfect, irrespective of the barrier height. By using a novel device design, we are able to block the normal transmission and thus demonstrate a large off-state resistance in graphene $p$-$n$ junctions.

2.1.1 Electronic transport in graphene field effect transistor

In this section we describe the transport properties in a graphene channel under low bias conditions. The discussion is based on the introductory lecture by Lundstrom et.al. The first electric field effect in graphene was demonstrated by Novoselov et.al. who showed that carriers in graphene behave as massless Dirac fermions. Using a gate voltage, the carrier concentration in graphene can be controlled. This allows us to study carrier density, mean free path, on-off ratio, mobility and other characteristics of graphene by changing the voltage on the gate, just as in a typical field-effect transistor. In graphene we use modulation of channel resistance with gate voltage to determine its electronic properties. In Figure 2.1 we consider an undoped graphene with no bias
applied on either side. As we apply a positive bias on the gate, a difference between the chemical potentials of graphene and the gate occurs, inducing negative charges into the channel.

\[ \text{Figure 2.1: Band structure of metal-oxide-graphene with } V_G=0 \text{ (left) and } V_G>0 \text{ (right)} \]

The increase in negative charge carrier density brings the fermi level into the conduction band. In other words, the bias applied on the gate can modulate the position of the fermi level which subsequently controls the polarity and the density of the carriers in the channel. Novoselov et al.\(^8\) have shown that with increasing gate voltage, either positive or negative, the number density of carriers increases linearly according to the relation

\[ n = \varepsilon_o \varepsilon V_G / dq, \]

where \( n \) is the carrier density, \( \varepsilon_o \) and \( \varepsilon \) are the permittivities in free space and the dielectric constant, \( V_G \) is the gate voltage bias, \( d \) is the thickness of the dielectric and \( q \) is the electronic charge.

Until now we assume that the charge neutrality point \( V_{CNP} \) is at \( V_G = 0 \) which is the gate voltage where minimum conduction occurs. In practical devices \( V_{CNP} \) is not zero and that correction has to be taken into account. This means that number density can be written as

\[ n = \varepsilon_o \varepsilon (V_G - V_{CNP}) / dq \quad \text{... (2.1)} \]
The dielectric capacitance $C_{ox} = \frac{\varepsilon \varepsilon_0}{d}$ is used in Equation 2.1. This capacitance relation is reasonable for gate oxides which are thick, but for thin oxides ($d<10\text{nm}$) the expression has to be modified to include the quantum capacitance\textsuperscript{12}. In our devices the dielectric thickness is 90\text{nm} and we ignore the quantum capacitance.

Next we calculate the density of states in the graphene channel with respect to the energy. As we learned before, graphene exhibits a linear energy dispersion relation for low field transport model. This is expressed as

$$E(\vec{k}) = \hbar v_F |\vec{k}| \quad \text{... (2.2)}$$

Here $|\vec{k}|$ is the length of the plane wave vector. When summed up over the $k$ space, the density of states can be written as

$$D(E) = \sum_{\vec{k}} \delta \left( E - E(\vec{k}) \right) \quad \text{... (2.3)}$$

Using integral to replace the summation we get

$$D(E) = \frac{WL}{4\pi^2} \int_{-\pi}^{\pi} d\theta \int_0^{+\infty} k dk \delta \left( E - E(\vec{k}) \right) \quad \text{... (2.4)}$$

Here $W$ and $L$ are the width and length of the graphene channel. Using Equation 2.2 we can rewrite Equation 2.4 as

$$D(E) = \frac{WL}{4\pi^2} 2\pi \int_0^{+\infty} \frac{E dE}{(\hbar v_F)^2} \delta \left( E - E(\vec{k}) \right) \quad \text{... (2.5)}$$

Using the definition for the Dirac function, we finally get

$$D(E) = \frac{WL}{2\pi} \frac{|E|}{(\hbar v_F)^2} \quad \text{... (2.6)}$$
Lastly including the spin and valley degeneracy we get the density of states in graphene as

\[ D(E) = \frac{2WL}{\pi} \frac{|E|}{(h\nu_F)^2} \quad \ldots \text{(2.7)} \]

Next we calculate the net carrier density \( n - p \) at \( T \neq 0K \) where \( n \) are the filled states when \( E > 0 \) and \( p \) are the empty states when \( E < 0 \).

\[ n - p = \int_0^\infty dE D(E)f(E) - \int_0^0 dE D(E)(1 - f(E)) \quad \ldots \text{(2.8)} \]

Using \( D(E) \) from \textbf{Equation 2.7} we get

\[ n - p = \frac{2}{\pi(h\nu_F)^2} \left( \int_0^{+\infty} dE \frac{E}{1+e^{(E-E_F)/kT}} - \int_0^{+\infty} dE \frac{E}{1+e^{(E+E_F)/kT}} \right) \quad \ldots \text{(2.9)} \]

At \( T = 0 \) we can simplify the above relation by approximating

\[ 1 + e^{(E-E_F)/kT} = 1 - \theta(E - E_F) \]

which gives

\[ n - p = \frac{2}{\pi(h\nu_F)^2} \left( \int_0^{+\infty} dEE(1 - \theta(E - E_F)) - \int_0^{+\infty} dEE(1 - \theta(E + E_F)) \right) \]

Finally, we arrive at

\[ |n - p| = \frac{E_F^2}{\pi(h\nu_F)^2} \quad \ldots \text{(2.10)} \]
The above expression provides us the number density depending upon the position of the Fermi level at T=0K. This implies that at zero energy there are no carriers present in the channel and an infinite resistance should be achieved. Theoretically due to quantum limitations the maximum resistivity is approximately \( \frac{\hbar}{4e^2} \approx 6.5\,\text{k}\Omega \), as shown by Geim et al.\(^{13}\) In practical devices the maximum resistivity close to charge neutrality point arises due to electron and hole puddles (Martin et al.\(^{14}\)) which are randomly arranged.

For a given energy \( E(\vec{k}) = \hbar v_F |\vec{k}| \) we can now calculate the number of current carrying modes in the graphene channel. The number of modes \( M(E) \) are calculated by summing over the k-space. We can write

\[
M(E) = \sum \delta \left( E - E(\vec{k}) \right) \frac{\pi \hbar}{L} |v_x(\vec{k})| \quad \ldots (2.11)
\]

Here \( v_x(\vec{k}) \) is the \( x \)-component of the group velocity given as

\[
v_x(\vec{k}) = \frac{1}{\hbar} \frac{dE}{dk_x} \quad \ldots (2.12)
\]

Following the similar integration process, we arrive at

\[
M(E) = \frac{Wk_F}{\pi} \quad \ldots (2.13)
\]

Taking spin degeneracy into account we can write total number of modes as

\[
M(E) = \frac{2Wk_F}{\pi} \quad \ldots (2.14)
\]
To define the conductance in a graphene channel we use the Landauer transport model\textsuperscript{15} which defines the conductance based on a transmission function using scattering theory. Using the equation defined by Datta\textsuperscript{16}, we can write the current as

\[
I = \frac{2q}{h} \int_{-\infty}^{+\infty} \bar{T}(E)(f_1(E) - f_2(E))dE \quad \text{... (2.15)}
\]

Here \(f_1(E)\) and \(f_2(E)\) are the fermi functions at the source and drain terminals and \(\bar{T}(E)\) is the total transmission. For low bias conditions \textbf{Equation 2.15} can be solved for the conductance as

\[
G = \frac{I}{V_D} = \frac{2q^2}{h} \bar{T}(E_F)
\]

\[
G = \frac{2q^2}{h} MT \quad \text{... (2.16)}
\]

This is the popular Landauer formula which is commonly used to study charge transport in a ballistic device. From \textbf{Equation 2.15} we interpret that the total current is proportional to the number of sub-bands present in the channel (\(M\)), the transmission probability of each sub-band (\(T\)) and the conductance quantum (\(2q^2/h\)). It should be noted that there is a finite conductance attached to a single mode and an infinite conductance cannot be achieved due to the fact that \textbf{Equation 2.16} contains both the interface resistance (resistance between metal contact and channel) and the device resistance.

\textbf{2.1.2 Angle dependent transport in graphene p-n junction}

The graphene p-n junction is formed by electrostatically doping two regions of graphene p-type and n-type, as shown in \textbf{Figure 2.2}. We discuss below the fabrication of buried split gates (gate 1 and gate 2). By changing the polarity of the bias on the gates, the bands in graphene can shift up and down to place the Fermi level either in the valence band or in the conduction band. The semi-
transparent gray sheet in Figure 2.2 is the fermi level. Unlike conventional semiconductors, carriers in graphene can easily tunnel from the conduction band into the valence band or vice-versa.

Looking top-down in Figure 2.2 we draw the Fermi surface in the two regions as shown in Figure 2.3. The electron in the conduction band, at the fermi level, has a wavevector \( k \) as \( (k_x, k_y) \) which tunnels into the valence band. In the \( y \)-direction there is no applied electric field and hence \( k_y \), the transverse momentum, is conserved. Now in the valence band (right side of Figure 2.3) we can have two states where the transverse momentum \( k_y \) is conserved. These states are \( (k_x, k_y) \) and \( (-k_x, k_y) \). To conserve the \( x \)-component of the group velocity, the electron in valence band will take (-
$(k_x, k_y)$ state. This implies that electrons in the conduction band when injected from a point source, bend at the $p$-$n$ junction and are focused at another point (Veselago lensing effect\(^1\)).

An electron in the conduction band approaching the junction with wave vector as $k = (k_c \cos \theta_c, k_c \sin \theta_c)$ comes out in the valence band with wave vector as $k = (-k_v \cos \theta_v, k_v \sin \theta_v)$. Conserving momentum in $y$-direction we get

$$\frac{\sin \theta_c}{\sin \theta_v} = -\frac{k_y}{k_c} \equiv n \quad \ldots (2.17)$$

This equation is similar to the Snell’s law but with a negative index of refraction. For a symmetric junction $n=1$. 

\[ \text{Figure 2.3: Lateral cross section of energy dispersion relation at the Fermi level in conduction band (left) and valence band (right)} \]
Next we calculate the transmission probability of an electron approaching the junction at an angle, based on the discussion by Cheianov et.al.\textsuperscript{2}. We consider a smooth potential step of the form $u(x) = \text{sign}(x)u_0/2$ for $|x| > d/2$ and $u(x) = Fx$ for $|x| < d/2$ where $F = vk_F/d$. Here $d$ is the distance between the split gates and $k_F$ as the Fermi wave vector for equally doped junction as shown in Figure 2.4. The junction is located at $x=0$.

The electron approaches the junction with $p_x = k_F\cos\theta$ and $p_y = k_F\sin\theta$. The x-component of the electron momentum can be written as

$$p_x = \sqrt{\frac{u^2(x)}{v^2} - p_y^2} \quad \ldots (2.18)$$

For a particle normally incident at the junction ($p_y = 0$) a classically forbidden region does not exist. Also backscattering is prohibited in chiral particles due to isospin conservation\textsuperscript{17}. We focus our attention to the case when ($p_y \neq 0$) for which a classically allowed region exists for $|u| >$
The classically forbidden region exists close to $x = 0$ with a width $l = v_p y / F$, obtained by solving Equation 2.18 for $p_x^2 < 0$. For waves which are travelling at an angle $\theta$, the tunneling probability is calculated using the WKB approximation where

\[ T \sim e^{-2S} \quad \text{... (2.19)} \]

Here,

\[ S = i \int_{-l}^{l} p_x(x) \, dx \quad \text{... (2.20)} \]

Solving the integral and applying the limits we write Equation 2.20 as

\[ S = -\frac{d}{2k_F} \left[ p_y^2 \left( \frac{\pi}{2} - \frac{3\pi}{2} \right) \right] \]

We finally have

\[ T(\theta) = e^{-\pi d k_F \sin^2(\theta)/2} \quad \text{... (2.21)} \]

The polar plot for this transmission function is shown in Figure 2.5 where transmission is perfect for modes travelling perpendicular to the junction and there is less transmission probability for modes that impinge the junction at an angle. The perfect transmission for the normal mode, which always exists, gives a finite off-state resistance. To address this there are two strategies that we can employ.

Surajit et al.\textsuperscript{3} have shown that a tilted junction gives a higher junction resistance compared to a non-tilted junction (Figure 2.6). With a tilted junction the angular transmission lobe is rotated which increases the number of modes with lower transmission probability. For a 45° junction we
observe that there is sharp increase in the resistance at low doping regime which is absent for the junction at $0^\circ$ angle. When the doping is low there are only a few momentum modes that determine the junction resistance.

In the case of $0^\circ$ channel these modes can easily tunnel through the junction and there is no peak in the resistance. But for a $45^\circ$ junction these modes at low doping will have a lower transmission probability and thus provide higher resistance. This is seen as sharp peak in the resistance for a $45^\circ$ junction. At high doping large number of momentum modes are supported and the two junction resistances ($0^\circ$ and $45^\circ$) are closer.

![Polar plot of the transmission function from Equation 2.21](image)

Figure 2.5: Polar plot of the transmission function from Equation 2.21
2.1.3 Device design to block the normal mode

The other strategy that can be used to block the normal (always conducting) mode is by physically placing a hole in the junction region (Figure 2.7). This is the main objective of the present work. At low doping there are very few modes traveling along the channel. In the ballistic regime (long mean free path) when these modes face the geometrical barrier, they are blocked and are sent back.

The red pie shaped area in Figure 2.7 shows the region of the modes that will blocked. In this regime the transmission probability is zero and by restricting the path of these modes we are expected to see very high resistance at low doping regime. Thus we can achieve a large on-off ratio in graphene without opening a band gap.

Figure 2.6: SEM image of the straight and tilted junction (left) and the corresponding junction resistance plot (right) [Reprinted with permission from Surajit et al., Nano Letters, 12 (9), 4460-4464, 2012. © 2012 American Chemical Society]
The design in Figure 2.7 can be further improved by employing different shapes for the cut region and also by defining the graphene tab regions at the ends to look more like point sources. These are discussed in detail in Section 2.3. Another property that is very important for angle dependent transport in graphene is the existence of ballistic transport. For this we use methods that provide very high quality graphene, discussed in Section 2.2. We also adopted the graphene transfer method that minimize polymer residue and the metal contamination.

2.2 Materials and Methods

In this section we describe the fabrication of the buried split gate structure which is used to selectively dope the graphene channel. Based on the bias polarity on the split gates we can create a p-type or n-type graphene channel to form a graphene p-n junction. We further discuss the graphene growth using chemical vapor deposition (CVD) along with graphene transfer on the substrate. Finally, we describe the fabrication of graphene p-n junction device for angle dependent transport study.

Figure 2.7: Physical cut placed at the junction to geometrically block the low angle traversing modes (left), red pie in the polar plot illustrates the blocked modes
2.2.1  Buried split gate fabrication

The split gate fabrication is done in the 300mm cleanroom facility. We start with a silicon wafer followed by wet thermal oxidation to grow 100nm of silicon dioxide as shown in Figure 2.8. The oxide layer serves as an isolation layer. For split gates we use a highly conducting poly-crystalline silicon which is deposited using CVD to achieve 100nm thickness. Using photolithography and reactive ion etching we define the poly-silicon gates with three different gate spacings of 100nm, 150nm, and 200nm. On the top surface we deposit 300nm of silicon dioxide using plasma-enhanced chemical vapor deposition process with a topography shown in Figure 2.8. We use chemical mechanical planarization process to remove the topography, and after CMP the surface is atomically flat. This is followed by deposition of 90nm of desired dielectric (SiO₂ in our case). Finally, to make electrical contacts to the poly-silicon split gates, we etch into SiO₂ over the bond pads. The split gate structure is now ready for graphene transfer and further device fabrication.

2.2.2  Graphene growth using chemical vapor deposition (CVD)

Until recently graphene devices were primarily fabricated by exfoliating graphite which is not a scalable technique. The advantage of exfoliated graphene is that the transfer process is very clean and very high quality graphene can be obtained. The electronic quality of the material is typically determined by the mobility of the carriers and very high mobility of nearly 200,000 cm²/Vs can be achieved. To improve on the exfoliation method, we use a new technique which is scalable while preserving the quality of graphene.

Both multilayer and single layer graphene has been previously produced by desorbing silicon from a silicon carbide crystal surface [Berger et.al., Emstev et.al.]. Also graphene has been synthesized by precipitating carbon on the surface of transition metals [Sutter et.al., Kanjaki.
Chemical deposition (CVD) technique is a very efficient method to grow large area graphene on a metal substrate. This method was adopted by Ruoff et al. to synthesize large area high quality uniform graphene on a copper foil. The process is highly reliable and was quickly adopted by many groups.

Figure 2.8: Buried split gate fabrication process, (a) patterning poly silicon gates, (b) depositing thick SiO2, (c) CMP process to planarize the top surface, (d) depositing required dielectric with specific thickness
For our work we use a modified process based on another report by Ruoff et.al.\textsuperscript{5} which gives large-size single-domain graphene. We start with a high purity 25\textmu m thick copper foil. The obtained copper has a thin layer of native oxide which is removed by etching in acetic acid for few hours. However there is a report by Gottardi et.al.\textsuperscript{24} where CVD graphene is directly grown on pre-oxidized copper to pave way for self-limiting graphene growth on dielectric, which can eliminate the subsequent transfer process. In our process after removing the copper oxide we rinse the copper foil with acetone and iso-propanol. Graphene growth is achieved inside a copper enclosure which is formed by bending the copper foil and crimping it on three sides. The copper pocket is shown in Figure 2.9. Before putting the pocket inside a CVD chamber, the chamber is baked at high temperature in the presence of hydrogen to remove contamination from the inner wall of the quartz tube.

Graphene growth is achieved at low pressure by first annealing the copper foil in flowing hydrogen at 1000\textdegree C which removes any oxide from the copper foil. The annealing step also helps to reduce the nucleation density\textsuperscript{25}. Typically, we anneal for 1 hour, after which 1sccm of methane is introduced into the chamber. The growth happens at 1050\textdegree C which is close to the melting point of copper. At high temperatures methane breaks down in the presence of copper through dissociative chemisorption which increases the active carbon content\textsuperscript{26}. At supersaturation level the nucleation begins which continues for a few minutes until the active carbon species are depleted. This is followed by nuclei growth and depending upon the carbon available the copper surface is covered with continuous film of graphene. Carbon has low solubility in copper and when the surface of
copper is fully covered with graphene, there the copper surface becomes no longer exposed to methane, resulting in a monolayer coverage over a large area.

Figure 2.9: Copper foil enclosure for pocket growth

[Reprinted with permission from Li et al.\textsuperscript{5}, Journal of the American Chemical Society, 133 (9), 2816-2819, 2011. © 2011 American Chemical Society]

Figure 2.10: Optical image of single domain graphene

In Figure 2.10 we show optical image of a single domain of graphene on copper using pocket growth technique. The size of the domain is nearly 300µm which is large enough to fabricate many devices. The growth is done for a short time and hence we do not see a complete coverage.
The next step is the fabrication of a graphene $p$-$n$ junction device with a hole etched in the middle. To do this we first clean the die in acetone and IPA to remove any contamination. Hexagonal boron nitride is then exfoliated on the top surface using the scotch tape technique\textsuperscript{8} and the device is cleaned again with acetone and IPA (Figure 2.11). To remove tape residue, we perform a high temperature annealing in air at 450$^\circ$C\textsuperscript{27}. The use of hexagonal boron nitride (h-BN) as a substrate for graphene was suggested by Dean et.al.\textsuperscript{28} who showed enhanced performance (mobility ~
100,000 cm²/V-s) of the graphene devices. h-BN is chemically inert and provide atomically flat surface with minimal surface charge traps. The graphene transfer is done using the method describe by Hu et al. The graphene, after transfer, covers the top surface of h-BN and also the surface of SiO₂. Using electron beam lithography, we pattern/etch the graphene channel with final metallization (Ti/Au) step as shown in Figure 2.11.

2.3 Results and discussion

The initial set of measurements after the device fabrication include determining the transfer characteristics of the device. For this both gates are tied together and swept from negative to positive voltages at for low drain bias $V_D=2$ mV. With the measured current the total resistance ($R_T$) of the device is calculated which has contribution from the contact resistances at source and drain ($R_C$) and also the channel resistance ($R_{CH}$). In Figure 2.12 we showed the typical resistance plot with changing number density. The number density $n$ is calculated assuming a parallel plate capacitor model as $n = V_G^* C_{ox}/q$ where $V_G^* = V_G - V_{Dirac}$. The resistance at high gate bias is roughly the contact resistance between the metal and graphene.

To fit the measured data, we use the method proposed by Kim et al., which is a constant mobility model where mobility does not depend on the carrier number density. We write

$$R_T = R_C + R_{CH} \quad \ldots (2.22)$$

$$R_T = R_C + \frac{L/W}{\sqrt{n_0^2 + n^2 q \mu}} \quad \ldots (2.23)$$

Here $L$ and $W$ are the length and width of the device, $n$ is the induced carrier density and $\mu$ is the number density independent mobility.
Figure 2.12: Transfer characteristic of graphene transistor

Figure 2.13: Schematic of a tilted junction fabricated on BN/graphene/BN stack
From the mobility fit we extracted the contact resistance $R_C = 700\, \Omega$ and $\mu = 7000\, cm^2/Vs$ at room temperature. We now discuss the characterization of a titled $p$-$n$ junction device (Figure 2.13) fabricated on h-BN/graphene/h-BN stack using the method described by Wang et.al.\textsuperscript{31}. The resistance plot of the device is shown in Figure 2.14 at room temperature (300K) and at liquid helium temperature (4.2K). At 300K we note that at the Dirac point the maximum resistance is close to the minimum conductivity $\left(\frac{h}{4e^2} \sim (6.5k\Omega)^{-1}\right)$. Cooling the device to 4K removes the broadening in the Fermi-Dirac distribution function and phonon scattering is inhibited. The resistance plot at 4K is much sharper compared to 300K data and the resistance at the Dirac point increases to $13.5k\Omega$. The mobility from Equation 2.23 gives $\mu_{4K} = 42,000\, cm^2/Vs$ which is quite large, thus confirming good graphene quality.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure2_14.png}
\caption{Transfer characteristics at 300K and 4K (left image) with mobility fit (red) using Equation 2.23 (right image)}
\end{figure}
Figure 2.15: (Top left) Resistance with respect to $V_{G2}$ at 300K obtained from the 2D resistance plot (top right) for different $V_{G1}$ values shows conductance asymmetry. (Bottom left) Resistance with respect to $V_{G2}$ at 4K obtained from the 2D resistance plot (bottom right)

**Figure 2.15** shows the two dimensional resistance plot for different values of $V_{G1}$ and $V_{G2}$. When $V_{G1}V_{G2}<0$, $n$-$p$ or $p$-$n$ junction is formed which has higher resistance than the case when $V_{G1}V_{G2}>0$. This is the characteristic conductance asymmetry\(^{32}\) observed when the doping changes from unipolar ($n$-$n$ or $p$-$p$) to bipolar ($n$-$p$ or $p$-$n$) regime; the colored lines show the section resistance plot along $V_{G2}$. 

---

\(^{32}\) Conductance asymmetry in semiconductor devices refers to the difference in electrical resistance depending on the direction of current flow. This phenomenon is crucial in understanding the behavior of materials under varying conditions, such as temperature and voltage, and plays a significant role in the design of electronic devices.
The black curves in **Figures 2.15 (top left) and (bottom left)** show the *pp-nn* transfer curve obtained by diagonally slicing the respective 2D resistance plots. We note that the charge neutrality point (CNP) at $V_{G1}=-1.5V$ and $V_{G2}=-1.5V$ and the maximum resistance value at the Dirac point is $\sim 13k\Omega$, close to $R_{Dirac}$ from **Figure 2.14 (left)**. For the unipolar case, pseudo spins match and there is no WKB tunneling but the tunneling factor and transmission probability function become important when we are in the bipolar regime. With a tilt in the junction the transmission lobe is shifted by the tilt angle and the modes have lower transmission, resulting in a higher resistance, as show in **Figure 2.15**. Strikingly this is what we observe in **Figure 2.15 (bottom)** for the 4K resistance plot where the highest resistance occurs away from the Dirac point ($V_{G1}=1V$, $V_{G2}=-1.5V$). The OFF state resistance obtained is $\sim 26k\Omega$, about 2x higher than the Dirac resistance (13.5kΩ). This represents the only known case in an engineered device where the highest resistance occurs away from the Dirac point, as expected from theory.

The second strategy that we employ to further enhance the OFF state resistance is by physically introducing a cut at the junction region, as described in **Section 2.1.3**. We first describe the case when there is no cut in the channel region. We call this structure the ‘no hole device’. The device schematic along with dimensions is shown in **Figure 2.16**. Here blue region is the graphene which has a narrower regions that make contact with the source and drain terminals, show in yellow. Not shown in the figure are the buried split gates. The graphene tab width is 500nm which acts as a broad point source of electrons. In future devices the tab width would be made smaller to act as perfect point source. The lengths of the tabs and the middle graphene region are 1µm and 2µm, respectively. As the first set of measurements we plot the transfer curve in **Figure 2.17** for this device at 4K.
For the device analysis we use the Landauer transport formalism to write a normalized conductance $G(e^2/h)$, considering valley and spin degeneracy, as

$$G(e^2/h) = 4 * T(E) * M(E) \quad \ldots (2.24)$$

Figure 2.16: Device schematic for a no hole device

Figure 2.17: Resistance plot with respect to sweeping gate voltages for no hole device at $T=4K$
Here the number of modes in the tab $M(E) = W k_F / \pi$ are calculated for $W=500\text{nm}$. We assume that the number of modes present in graphene tabs control the charge transport in the device and hence a uniform width $W$ is considered. From Datta\textsuperscript{33} the transmission probability through a conductor of length $L$ is given as $T = \lambda / (\lambda + L)$, where $\lambda$ is the mean free path. We consider the tab graphene region close to source (drain) as section 1 (section 3) with transmission probability $T_1=\lambda / L$ ($T_3=\lambda / L$). The middle region is section 2 with transmission probability $T_2=\lambda / 2L$.

For sections in series $(1 - T) / T$ is an additive property and hence we can write the total transmission probability through all the three sections as

$$T \cong \frac{\lambda}{4L} \quad \ldots \quad (2.25)$$

![Figure 2.18: Conductance as a function of number density, measured (black open circles) and fit (red line)](image)
We use the same transmission probability to analyze the ‘no hole’ and ‘hole’ device. We show in Figure 2.18 $G(e^2/h)$ for the ‘no hole device’. The measured conductance (black open circles) is obtained as the inverse of resistance plot from Figure 2.17 and the fit (red curve) is done using the Equation 2.24. Close to the Dirac point the fit has good agreement with the measured conductance for $\lambda = 100 \text{nm}$.

Next we discuss the ‘hole device’ shown in Figure 2.19. The hole device is identical to the no hole device with an exception of 600nm wide cut in the middle. The resistance plot with respect to gate voltage is shown in Figure 2.20 at 4K. The maximum resistance $R \sim 900k\Omega$ is obtained at $V_{G1/G2} = -0.6V$ which is the low doping regime with very few populated modes. Thus $f$ for the hole device

**Figure 2.19: Device schematic for the hole device**
the modes which are traversing at low angles are blocked by the cut, which increases the OFF state resistance by 20x compared to the no-hole case, as shown in Figure 2.17.

To analyze the hole device, we first plot in Figure 2.15 the normalized conductance \( G(e^2/h) \) as a function of number density. We introduced a model that accounts for the number of transmitted modes. For this we calculated the number of modes present in the tab with width \( W \sim 500 \text{nm} \). We also note from Figure 2.19 that with increase in number density, the fermi wave vector increases \( (k_{F2} > k_{F1}) \) to populate more modes within the fermi circle. We then calculate the angle associated with each mode and discard the modes that are travelling with \( \theta < 45^0 \) (black arrow) and also the ones with \( \theta > 75^0 \) (green arrow). Thus, we only accept the modes that are travelling between 45 and 75\(^0\). For our analysis we use the same transmission probability from Equation 2.25 for the modes which are allowed and the total conductance is calculated using Equation 2.24. The fit to the measured conductance for hole device is shown in Figure 2.21.
Assuming the same mean scattering length as used for the ‘no hole’ device ($\lambda = 100\,nm$) we find a very good fit (red) to the normalized conductance plot (black) for the hole device in Figure 2.21. The red filled dots correspond to the conduction due to modes that exist only for $45^0 < \theta < 75^0$. The goodness of the fit confirms that the high OFF state resistance is attributed to blocking of low angle travelling modes. Equation 2.23 cannot explain this large resistance based on the total number of squares that contribute to the total resistance.

Figure 2.21: Conductance with respect to number density, measures (black) and fit (red)

Figure 2.22 shows the 2D resistance plot for the ‘no hole’ device (top) and the hole device (bottom) at 4K. Compared to the ‘no hole’ device, the hole device (away from the Dirac point) has very high resistance peaks.
Finally, to confirm the high quality of graphene we perform magneto-transport measurements by applying a vertical magnetic field $B=2T$. Figure 2.23 shows the resistance versus gate voltage plot in the presence of magnetic field. The Landau levels (LL) with filling factors $n = \pm 1$ are clearly seen with signatures of higher filling factors. The change in gate voltage for each filling factor is calculated using $E_n = \text{sgn}(n)\sqrt{2e\hbar v_F^2|\vartheta|B}$ where $v_F = 10^6 m/s$ is the fermi velocity, $B$ is the magnetic field and $\vartheta$ is LL index and $E_n$ is the LL energy. Using $E_n$ we calculate the change in gate voltage for each LL level using $E_F = \hbar v_F\sqrt{n\pi}$ and $n = C_{ox}V_G/q$ where $n$ is the number
density. From this we calculated $\Delta V_G \sim 0.75$ for the consecutive LLs which matches well the LL positions obtained from Figure 2.23 (left) and plotted with respect to LL index in Figure 2.23 (right) to give a slope of 0.83V/LL.

![Graph showing resistance vs. $V_G$ and LL peaks vs. index $n$](image)

**Figure 2.23: Resistance as a function of $V_G$ for $B=2T$ showing Landau levels (left), LL position with respect to index $n$**

### 2.4 Summary

In conclusion we demonstrated graphene $p$-$n$ junction with increased OFF state resistance by geometrically blocking the low angle traveling modes. The highest OFF state resistance we have achieved is $\sim 900k\Omega$ to provide an ON/OFF current ratio of $\sim 100$. We performed preliminary measurements with a tilted junction on BN/graphene/BN stack to confirm the angle dependent transport and used a high quality pocket growth CVD technique to prepare high mobility graphene.

The quality of the graphene is further confirmed by the presence of Landau levels at low magnetic
fields. We analyzed our hole device using the mode blocking model which agrees with the angles defined in the device geometry.
References


Chapter 3

**WSe$_2$ BASED BIPOLAR JUNCTION TRANSISTOR AND PHOTOTRANSISTOR**


### 3.1 Primer on Bipolar junction transistor

Bipolar junction transistors have wide applications in analog circuits and are used for signal amplification\(^1\) which was previously done using vacuum tubes\(^2\)\(^-\)\(^3\). The bipolar junction transistor was invented in the late 40s at Bell Telephone Laboratories\(^2\). The first transistor was a point contact transistor\(^5\)\(^-\)\(^6\) developed by John Bardeen and Walter Brattain in 1947. This transistor was formed by pressing two strips of gold foils, hair-length apart, against a germanium block using plastic wedge held in place by a make shift spring. The design was fragile and difficult to commercialize which inspired William Shockley to develop a transistor based on junctions\(^7\). The junction transistor revolutionized the electronics industry which was not possible using vacuum tubes.

The bipolar junction transistor is a three terminal device which consists of two back-to-back $p$-$n$ junction diodes with three regions defined as emitter, base and collector. Emitter and collector regions are at the ends of the transistor with a thin base region in the middle. Two kinds of bipolar transistors can be realized, $n$-$p$-$n$ and $p$-$n$-$p$, as shown in Figure 3.1 along with their circuit symbols. The arrows indicate the direction of current in normal operation of the transistor. In an
In a $p-n$ junction under forward bias, holes are injected from the $p$-region into $n$-region and electrons are injected from the $n$-region into $p$-region to provide a large current, which increases with forward voltage\(^8\). When the junction is reverse biased, a small current flows which is due to the generation of minority carriers in the vicinity or in the space-charge region. The value of the reverse bias current does not necessarily depend on the strength of the reverse bias voltage (\textit{i.e.} the strength of electric field), but it depends upon the rate of generation of electron-hole pairs (EHPs) in the neighborhood of the junction \textit{i.e.} within the diffusion length of the junction. To increase the reverse saturation current EHPs can be optically generated by using photon energies that are

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{transistor_diagram.pdf}
\caption{(a) block structure of $n$-$p$-$n$ transistor with circuit symbol below, (b) block structure of $p$-$n$-$p$ transistor with circuit symbol below}
\end{figure}

\(n$-$p$-$n$ transistor, the emitter and collector regions are doped $n$-type with a $p$-type base in the middle; reverse is true for the $p$-$n$-$p$ configuration.
greater than the band gap energy of the material. The reverse current will then scale with the optical generation rate.

Another method to increase the reverse saturation current, which is also the fundamental working principle of a bipolar junction transistor, is by placing a forward biased junction adjacent to a reverse biased p-n diode. The forward biased junction in a BJT acts as a source of minority carriers, which travel across the base to be swept away in the collector region. The collector current is then controlled by the forward biased junction. The above mechanism where current in one junction is controlled by the bias applied on the other junction is called the transistor effect.

Illustrated in Figure 3.2 is the block diagram for an n-p-n transistor depicting the flow of electrons and holes. The emitter region on the left is highly doped which acts as an electron injector; the base region is a thin lightly doped p-type material, and the collector region is moderately doped as n-type, which also acts as sink. In normal operation, emitter-base junction is forward biased \( V_{EB} < 0 \) and the base-collector region is reverse biased \( V_{CB} > 0 \). The current flow terminology in the emitter due to electrons and holes is as follows:

\[ I_{En} \]: electron current due to diffusion of electrons across the base

\[ I_{Ep} \]: hole diffusion current due to holes diffusing into the emitter

In a well-designed transistor, the base current has a primary component from holes, \( I_{Br} \) which recombine with the electrons injected from the emitter. The second component of base current is due to holes diffusing into the emitter which is also equal to \( I_{Ep} \). Finally, the third component, which also reduces the base current, is due to reverse bias current from holes generated in the
collector region (not shown in Figure 3.2). Therefore, the collector current \( I_C \) is mainly composed of electrons injected from the emitter (or also source) across the base.

Figure 3.2: Schematic to illustrate hole and electron flow in an \( n^+p^-n \) transistor along with proper biasing conditions. Not shown is the reverse bias current at base-drain junction

### 3.1.1 DC characteristics

In this analysis we consider an ideal transistor model where no recombination occurs in the space charge region. The total current in each region is then

\[
I_E = I_{En} + I_{Ep} \quad \ldots (3.1a)
\]

\[
I_B = I_{Ep} + I_{Br} \quad \ldots (3.1b)
\]

\[
I_C = I_{En} - I_{Br} \quad \ldots (3.1c)
\]

This suggests that the emitter current \( I_E \) is the sum of the collector and the base current. Hence,
\[ I_E = I_B + I_C \quad \ldots \ (3.2) \]

Figure 3.3 shows the minority carrier concentrations in the quasi-neutral regions (qnr) for a short base where the diffusion length of the minority carrier is larger than the quasi-neutral region for a forward biased emitter-base junction with \( V_{CB} = 0 \text{V} \). In this situation the electron density changes linearly with position unlike in a long diode where electron density decays exponentially with position. From Zeghbroeck\textsuperscript{10}, Taur\textsuperscript{9}, assuming negligible electric field in the neutral regions where majority carrier concentration is uniform, we make the following assumptions before solving currents in each region:

a) Emitter current is mainly composed of electrons which diffuse toward the collector across the base.

b) Drift current is assumed to be non-existent in the base region

c) The reverse bias saturation current from the collector is negligible

d) The cross-sectional area is assumed to be uniform throughout the device

Figure 3.3: Schematic to illustrate minority carrier concentration profile in all the three regions (S, B, and D) of an \( n^*-p^-n \) BJT
With these assumptions electron and hole currents in the emitter region can be solved for short diode structure.

\[
I_{En} = qA \frac{D_n p}{w'_B} \left( e^{\frac{qV_{BE}}{kT}} - 1 \right) \quad \text{... (3.3a)}
\]

\[
I_{Ep} = qA \frac{D_p n}{w'_E} \left( e^{\frac{qV_{BE}}{kT}} - 1 \right) \quad \text{... (3.3b)}
\]

Here \(A\) is the cross-section area of the junction, \(k\) is the Boltzmann constant, \(T\) is the temperature, \(D_n\) is the diffusion coefficient of electrons in the base region, \(D_p\) is the diffusion coefficient of holes in the emitter region, \(w'_B\) and \(w'_E\) are the effective quasi-neutral widths of base and emitter regions, respectively. For short diodes the total excess minority carrier charge in the base region is given as

\[
Q_B \cong \frac{1}{2} qA \Delta n_E w'_B \quad \text{... (3.4a)}
\]

Equation 3.4a can be rewritten as

\[
Q_B \cong \frac{1}{2} qA n_p \left( e^{\frac{qV_{BE}}{kT}} - 1 \right) w'_B \quad \text{... (3.4b)}
\]

If this charge in the base region recombines in \(\tau_n\) seconds we can then write the base current as

\[
I_{Br} = \frac{Q_B}{\tau_n} \quad \text{... (3.5)}
\]

where \(\tau_n\) is the minority carrier lifetime, which can depend upon the doping in the base region. The emitter electron current can also be written as
\[ I_{En} = \frac{Q_B}{\tau_t} \quad \ldots (3.6) \]

where \( \tau_t \) is the transit time electrons take to cross the base region. It is also denoted as the time electrons spend in the base region. The transport factor \( \alpha_T \) (Muller) is a quantity which measures the electron loss due to recombination in the base region. This quantity is calculated as

\[ \alpha_T = \frac{|I_{En}| - |I_{BR}|}{|I_{En}|} = 1 - \frac{w_B^2}{2D_n\tau_n} \quad \ldots (3.7) \]

This suggests that the loss of minority carriers in the base region due to recombination can be reduced by forming a thin base layer, which is an important aspect of this present work. Finally, we define current gain as the ratio of collector current to the base current,

\[ \beta = \frac{I_C}{I_B} \quad \ldots (3.8) \]

The current gain \( \beta \) is defined when the transistor operates in a forward active mode, which means that \( V_{BE} > 0 \) and \( V_{CB} \) can be zero or negative (Muller\textsuperscript{11}). Under this condition the current into the base is the input current and output current is measured from the collector.

### 3.2 Materials and Methods

#### 3.2.1 Buried gates fabrication for tungsten diselenide BJTs

This section describes the process steps to create buried gate structures for electrostatic doping of WSe\(_2\) flake. The fabrication is carried out in CNSE’s 300mm cleanroom facility. Sample preparation and device fabrication are done on individual die.

The fabrication steps are schematically described in Figure 3.4. We start with a 300mm silicon wafer which is oxidized to grow 200nm silicon dioxide (SiO\(_2\)) using a thermal oxidation process
in Figure 3.4a. To create buried gates optical patterning and etching are performed to remove 50nm SiO$_2$ from the patterned regions, which creates recesses for split gates (SGs) in Figure 3.4b. The spacing between the split gates and also the width of the middle gate region are 100nm. This is then followed by physical vapor deposition of tungsten on the top surface which also covers the recessed area in Figure 3.4c.

![Figure 3.4: Buried split-gate process development](image)

Chemical-mechanical-planarization is performed to planarize the entire surface and to remove the tungsten in between the recessed regions, as shown in Figure 3.4d. The thickness of the tungsten after CMP is reduced to 30nm. The final step involves depositing a silicon nitride (Si$_3$N$_4$) gate.
dielectric as shown in Figure 3.4e. For planarization and to achieve the required dielectric thickness another touch-up CMP process is employed which reduces the silicon nitride thickness to 20nm (Figure 3.4f).

3.2.2 Sample preparation and device fabrication

In this section we discuss the additional experimental steps performed to prepare the two-dimensional WSe$_2$ channel material for the bipolar junction transistor device fabrication.

Sample preparation for device processing is performed on a die cleaved from a 300mm wafer. The die is rinsed with acetone and isopropanol (IPA) to remove unwanted organic residues after which the sample is analyzed under optical microscope to look for split-gate locations with minimum residue. Bulk tungsten diselenide crystals are obtained commercially. Mechanical exfoliation technique which has been previously used to exfoliate graphene$^{12}$ is employed to prepare two dimensional WSe$_2$ flakes on the buried gate structures. For this we use a piece of thermal release tape and several crystals of WSe$_2$ are placed on it. The two ends of the tape are brought into contact multiple times to thin down the crystals which eventually cover the tape surface. One end of the tape is placed against the top surface of the die at a specific location identified under the optical microscope. The sample with the tape on it is placed on a hot plate at 65$^\circ$C for 20 minutes. This allows the WSe$_2$ flakes to successfully stick onto the die surface. The tape is then gently removed and the sample is further studied under the microscope.

The above method often leaves tape residue contamination which degrades device performance. To overcome this issue pick-and-place method has been adapted by several groups$^{13}$ where exfoliated flakes are picked using a polymer and dropped at specific sites which are clean. The choice of tape is important because some tapes leave residue which are hard to remove even with
cleaning processes. For this work we use a thermal release tape which leaves very little residue and the die is further cleaned in acetone and IPA for several hours to remove any contamination. After rinsing with DI water the sample is dried with nitrogen gas. A final cleaning process is performed by annealing the sample at 450°C at ultra-high vacuum which satisfactorily removes any polymer residue.

Flakes are identified based on their thickness and location. For device fabrication thin flake is chosen with a requirement that it should be located above the buried gate region (Figure 3.5). Flakes are chosen based on the optical contrast which occurs due to interference from the dielectric layer underneath. The technique has the advantage of being a quick non-destructive method to identify large flakes with different thicknesses. The thickness of the flake can be further confirmed by using atomic force microscopy (AFM). When a desired flake is identified in the gated region, the sample is ready for further device processing.

Figure 3.5: Optical image of a thin flake located on split gates
For our bipolar junction transistor, we label the terminals source (S), base (B), and drain (D) as shown in Figure 3.6a to be consistent with the results of Chapter 4. These three metal regions are defined using electron beam lithography using predefined alignment marks. To accomplish this, the sample is first coated with MMA 8.5 EL6 resist at 6000rpm for 60 seconds followed by 160°C bake on a hot plate. A second resist layer PMMA 495K is spun at 5000rpm for 60 seconds with the same baking step. The expected thickness of the bilayer stack is estimated as 100nm.

The first metal layer is written at 300μC/cm² using 2nA beam current at 100keV. The sample is developed in MIBK: IPA (1:3) for 60 seconds with final rinsing in IPA for another 60 seconds. The features are examined in optical microscope. For contacts to WSe₂, 10nm silver (Ag) metal is evaporated in an e-beam evaporator, followed 20nm gold (Au) evaporation as a capping layer. The metal lift-off process is done in acetone at 65°C for few hours. Sonication is typically avoided for metal lift–off which can displace WSe₂ flakes. A second lithography step is performed to define the bond pads where electrodes probes are landed. This metal layer should be sufficiently thick to sustain repetitive probe landings. For the second lithography step, the sample is spin coated with PMMA 950K at 3000rpm followed by 170°C bake on a hot plate for 5 minutes. The resist layer thickness is estimated to be 300nm.

Exposure is done under 20nA beam current with 800μC/cm² dose. Final metallization for bond pads is done with a thick metal evaporation of Ti(10nm)/Au(50nm) to allow repetitive electrical measurements. After the metal lift–off, the sample is washed in IPA and dried with nitrogen before performing electrical and optical measurements.

Figure 3.6b shows the SEM image of the fabricated device showing the three terminals: source, base, and drain contacting the WSe₂ flake. Also seen in the image are the three split gates underneath which are well aligned with the respective metal layers. The base electrode is narrow.
(50-70nm) and contacts the side of the flake to prevent shunting of the device as explained in Section 3.3.

Figure 3.6: (a) WSe$_2$ BJT device model with buried split gates, (b) SEM micrograph of the fabricated structure with three metal terminals (S, B, and D) contacting a semi-transparent WSe$_2$ flake. The buried gates are also seen in the background.
3.3 Results and Discussions

This section describes the characteristics of a bipolar junction device (BJT) formed on exfoliated WSe$_2$ TMD semiconductor that show both current and photocurrent gains.

Unlike impurity doping techniques, where physical substitutional doping method is used to create individual $p$-type and $n$-type regions, the electrostatic doping technique has the advantage of allowing reconfigurability. This implies that the doping in a certain region can be interchanged from $p$-type to $n$-type and vice versa. This is achieved by changing the polarity of the voltage applied on the gate. A positive voltage on a buried gate populates the channel with electrons and thus $n$-type region is formed; a negative voltage attracts holes to create a $p$-type region. The electrostatic doping method was first introduced in 2004 to create carbon nanotube $p$-$n$ junction$^{16}$ diodes which has been further utilized to study $p$-$n$ diode and transistor properties of other two-dimensional materials$^{17-20}$.

In our work we use the reconfigurable doping method to create a BJT device with both $n$-$p$-$n$ and $p$-$n$-$p$ transistor configurations. From Figure 3.6 we see that for a BJT device a third terminal and thus a third gate is used, unlike in a $p$-$n$ diode which is a two terminal device. The three terminals are labelled source (S), base (B), and drain (D) and the respective gates underneath are labelled G1, G2, and G3 to create the three doped regions. The BJT device structure can be extended to study phototransistor properties for which the base terminal is left floating.

3.3.1 BJT device characteristics

An important requirement of electrostatic doping technique is ambipolar conduction, the ability to provide both hole and electron conduction into the channel. This characteristic feature of the
present doping mechanism allows metal contacts to inject both electrons and holes into the channel, depending on the polarity of the gate.

**Figure 3.7** shows the transistor transfer characteristic between the source and drain terminals. The three buried gates (G1, G2, G3) are tied together and gate voltage is swept from -2.5V to +2.5V with source voltage $V_S = 0V$ and drain voltage $V_D = 100mV$. The measurement is carried out in vacuum to minimize the external contamination due to adsorbates. For electrical characterization Agilent B1500A semiconductor parameter analyzer is used. The ambipolar conduction is clearly demonstrated in the device. For positive gate voltage ($V_G > 0$) electrons are attracted in to the channel to provide conduction due to electrons. As the voltage on gate is increased to more positive values the drain current increases. The situation is repeated when negative voltage is applied on the buried gates. For $V_G < 0$, holes are attracted to provide hole current which also increases as $V_G$ is increased more negatively. An interesting observation from this transfer curve is the asymmetry in the electron and hole currents. The asymmetry has been reported previously in semiconducting carbon nanotubes\textsuperscript{21-22}. The asymmetry could arise due to the modulation of a Schottky tunnel barrier between a metal-semiconductor junction\textsuperscript{23-24} or it can be due to adsorbates which provide unintentional doping\textsuperscript{23; 25}.

Demonstration of ambipolar transport in WSe$_2$ flake\textsuperscript{26} allows us to create a $p$-$n$ diode which is the building block for most semiconductor devices. To create a $p$-$n$ junction, one side of the flake is formed as $p$-type ($V_G < 0$) and the other side is formed as $n$-type ($V_G > 0$). The respective gate voltages are chosen sufficiently large relative to the minimum conductivity point of the transfer curve to minimize the contact resistance. The central property of a $p$-$n$ diode is that it allows large current under forward bias and little current when the junction is under reverse bias. The $p$-$n$ junction is forward bias when a positive bias is applied to the $p$-region which is equivalent to
applying negative voltage to the n-region. To create a reverse bias junction, the polarity of the bias voltage is switched.

In our work we demonstrate two diode configurations $p$-$p$-$n$ ($V_{G1,2} = -2.0V$, $V_{G3} = 2.0V$) and $n$-$p$-$p$ ($V_{G1} = 2.0V$, $V_{G2,3} = -2.0V$). The diode property is studied between source-drain terminals with $V_S = 0V$ and $V_D$ is swept from $+700mV$ to $-700mV$. Figure 3.8 shows the diode characteristic for $p$-$p$-$n$ and $n$-$p$-$p$ configurations. For $V_{DS} > 0V$, an $n$-$p$-$p$ diode is forward biased with a large current flowing between the terminals. The applied bias $V_{DS}$ acts against the built-in electric field which reduces the potential energy barrier at the junction. This allows large number of minority carriers to diffuse across the transition region. In case of an $n$-$p$-$p$ junction under forward bias, electrons

![Figure 3.7: Transfer characteristic to demonstrate ambipolar conduction in WSe$_2$ by sweeping all three gates together at $V_{DS}=0.1V$](image-url)
from the $n$-region diffuse toward the $p$-region and holes from the $p$-region travel to the $n$-type region. With increase in forward bias voltage minority carriers diffusing across the junction increase which results in large current at high $V_{DS}$ as seen in Figure 3.8. For the case when $V_{DS} < 0$, the $p$-side of the $n$-$p$-$p$ diode is more negatively biased compared to the $n$-side and the junction is in reverse bias. The small current flowing between the terminals is due to the generation of minority carriers which diffuse toward the junction and are swept away by the electric field. The reverse bias current for an ideal diode is independent of the bias voltage, which suggests that the current does not depend on how quickly the carriers are swept away by the electric field but upon the generation rate of the carriers. The number of minority carrier generation rate in the $p$ or $n$ region is small and hence very little current is seen in under reverse bias in Figure 3.8.

It is important to note that the metal-semiconductor junction is not necessarily ohmic and it typically follows a Schottky behavior. The Schottky barrier exists at the source and drain ends which can also give a rectifying $I$-$V$ response. To confirm that rectification originates from the

![Figure 3.8: Output characteristic for WSe$_2$ based $p$-$p$-$n$ and $n$-$p$-$p$ diodes](image)
middle junction region and not due to Schottky barrier at the ends, a corresponding diode is formed by reversing the doping profiles at the source and drain regions while keeping the middle region fixed. To achieve this, we create a \( p-p-n \) junction using the same voltage \( V_G = -2.0 \)V to create a \( p \)-region and \( V_G = 2.0 \)V to create an \( n \)-region. For this configuration it is observed from Figure 3.8 that large forward bias current exists for \( V_{DS} < 0 \)V which is consistent with the diode polarity. The diode curves for \( n-p-p \) and \( p-p-n \) are thus symmetric in nature which suggests that Schottky tunnel barrier is small.

The diode characteristics from Figure 3.8 confirm that rectification exists in our device between source and drain contacts. Additionally, to create a successful \( n^+ - p^- - n \) transistor, diode behavior was studied at the source-base junction (J1) with \( n^+ - p^- \) (\( V_{G1} = 2.5 \)V, \( V_{G2} = -0.25 \)V) doping configuration and at the base-drain junction (J2) with \( p^- - n \) (\( V_{G2} = -0.25 \)V, \( V_{G3} = 1.5 \)V) doping configuration (Figure 3.9). Both J1 and J2 show good rectifying behavior with exponential dependence of forward current on bias voltage (\( V_S \) for J1, \( V_D \) for J2). At high forward bias, current has a weak exponential dependence which is due to the voltage drop across the series resistance \( R_S \). This resistance consists of the \( p \) and \( n \) channel resistances adjacent to the junction, and also the contact resistances at the metal electrodes. A fit to the measured current-voltage characteristic was performed using the Shockley diode equation with adjustments to include the effects of series resistance and trap assisted recombination in the junction region. We thus have,

\[
I = I_o \left( e^{\frac{q(V-I R_S)}{nkT}} - 1 \right) \quad \text{(3.9)}
\]

where \( I \) (\( V \)) can represent \( I_{SB}(V_{SB}) \) or \( I_{DB}(V_{DB}) \), \( I_o \) is the reverse saturation leakage current, \( R_S \) is the series resistance, \( n \) is the diode ideality factor, \( k \) is the Boltzmann’s constant, and \( T \) is the temperature. The diode ideality factor \( n \) is 1 for an ideal diode where negligible electron-hole
recombination occurs in the junction region. \( n \) can range between 1 to 2, based on the recombination rate attaining higher values for large recombination in the junction region. We extracted \( I_o, R_S \) and \( n \) by fitting the diode equation to the measured data (solid lines). The obtained \( n \) for J1(J2) is \( \sim 1.37(1.3) \) which is higher than \( n=1 \) and is associated with the recombination due to defects. However, with adequate rectification observed in both diodes and low leakage current values at 0.2V, we are able to study the properties of an \( n^+ \)-\( p^- \)-\( n \) bipolar junction transistor.

Figure 3.9: (Top) \( n^+ \)-\( p^- \) junction between S-B, (bottom) \( p^- \)-\( n \) junction between B-D. The fits are shown as solid lines in red.
With the successful demonstration of the diode behavior for junctions J1 and J2 we now demonstrate the bipolar junction transistor. The equilibrium energy band diagram of an $n-p-n$ BJT is shown in Figure 3.10 (Top). The source and drain regions are $n$-type and the middle base is $p$-type. Under equilibrium the Fermi level is constant throughout the device and there is no net current flow. To analyze the BJT we maintain zero potential on base terminal which allows us to draw a direct comparison with the phototransistor where base contact is floating. We start by discussing the BJT for an $n-p-n$ configuration and discuss the phototransistor effect in the same device.

The purpose of this work is to demonstrate high current gain in tungsten diselenide BJT. The current gain is defined as

$$\beta = \frac{I_D}{I_B} \quad \ldots \quad (3.10)$$

where $I_D$ is the drain current and $I_B$ is the base current. It is a measure of the number of electrons that can transit from source to drain before recombining with a hole which enters through the base contact. The hole current from the base thus controls the flow of electrons from the source to the drain. To achieve high current gain $I_D$ has to be maximized and $I_B$ should be reduced. This can be accomplished by increasing the efficiency of the source to inject electrons; heavily doped source region injects a large number of electrons across the base region. To minimize $I_B$ the base region width is made smaller than the electron diffusion length across it.

The $n-p-n$ transistor is turned on when source-base junction (J1) is forward biased, which injects electrons from the source into the base and holes from the base into the source. To forward bias J1, we make $V_B = 0$ and $V_S < 0$ under normal operation, base-drain junction is reverse biased by making $V_D > 0$. The energy band diagram in Figure 3.10 (bottom) shows the normal operation
mode of an n-p-n BJT. The electrons injected from the source diffuse toward the base region as minority carriers. In an ideal BJT all the injected minority carriers reach the drain terminal. In practical transistors some of the diffusing minority carriers recombine in the base region to contribute to the base current.

Figure 3.11 shows the dc characteristic of an n⁺-p⁻-n BJT which is formed by using $V_{G1} = 2.5\text{V}$, $V_{G2} = -0.2\text{V}$, and $V_{G3} = 1.5\text{V}$. These gate bias configurations are based on the transfer curve and result in the source region being heavily n-type, base region lightly p-type, and drain region
moderately n-type. In Figure 3.11 we show the absolute currents from all the three terminals as we sweep $V_D$ for different $V_S$ values.

We begin our discussion for the case when $V_S = 0$ (curves in black) while keeping the base terminal at ground ($V_B = 0$) for all $V_S$ values. From Figure 3.11 we see that all the three currents from source, base and drain show a diode behavior as we sweep $V_D$ from 500mV to -250mV. With base terminal grounded and $V_D > 0$, J2 is reverse biased and the electrons in the drain region have large potential barrier to reach to the base region. The drain current has one component from the base which consists of the generation current. Base current $I_B$ is negative for this case where electrons (minority carriers) in the base diffuse toward the base-drain junction region. The other component to the drain for $V_D > 0$ comes from the source where electrons due to thermionic emission cross over the barrier at J1 and reach to the drain. The diode like behavior of the three currents is governed by the bias applied on drain $V_D$. For $V_D < 0$, both $I_B$ and $I_S$ increase with $V_D$ and show the forward bias characteristic of a $p$-$n$ diode. It is noted that the base current changes sign as confirmed by a dip in $I_B$ at $V_D = 0$.

To demonstrate gain we forward bias J1 by making $V_S = -0.1V$ with $V_B=0V$. As seen from the band diagram in Figure 3.10 (bottom), the barrier at J1 is lowered and more electrons should be able diffuse across the base. From Figure 3.11 for $V_S = -0.1V$ (forward bias J1), a large number of electrons travel across the base and are collected at the drain which is seen as an increase in $I_D$ and $I_S$. Now the base current $I_B$ maintains the same positive sign throughout the entire range of $V_D$ and is due to holes injected from the base contact. The electrons injected from the source recombine with the few holes in the base but are mostly collected in the drain region. For $V_S = -0.1V$, $I_S$ is nearly equal to $I_D$ because $I_B$ is very small. As discussed before in Section 3.1, in a well-designed BJT, the base current is primarily due to the holes which recombine with electrons, coming from
source, in the base region and also due to the diffusion current of holes in base into the emitter region. To minimize the second component, the base doping is kept low ($V_{G2}=-0.2\,\text{V}$) and also the source is highly $n$-type ($V_{G1}=2.5\,\text{V}$) which efficiently injects a large number of electrons. The third component to the base current is the generation current at J2 which has little contribution to the gain and is minimized by keeping the drain moderately doped as $n$-type ($V_{G3}=1.5\,\text{V}$). The gain from the dc characteristic is nearly 100 at $V_D=0.5\,\text{V}$.

![Figure 3.11: Current-Voltage characteristic showing currents from all the three terminals ($I_S$, $I_B$, $I_D$) for $V_S = [0\,\text{V}, -0.1\,\text{V} \text{ and } -0.3\,\text{V}]$](image)

While still keeping the base terminal grounded we increase the strength of forward bias on J1 by making $V_S=-0.3\,\text{V}$. From Figure 3.11 we observe that all three currents ($I_S$, $I_B$, $I_D$) are further enhanced with $I_B$ maintaining the same positive sign throughout the entire range of $V_D$. On the other hand, source and drain currents are nearly equal. With $I_B$ significantly lower than $I_D$ we extract high gain at $V_D=0.5\,\text{V}$. The dc characteristic confirms that bipolar transistor effect exists in
two dimensional WSe$_2$ flake where the drain current is governed by the strength of forward bias on the source-base junction. Increasing the forward bias characteristic of J1 increases the amount of current collected at drain region.

Besides the forward bias applied on the source to control the source-base barrier height, another parameter that controls the potential barrier is the doping of the base region. The electrostatic doping method, unlike substitutional doping, has the advantage that one can control the number density of the charge at the surface and thus controls the position of the fermi level. To study the effects from changing the base doping on transistor properties, we plot in Figure 3.12, the three-dimensional gain map with respect to forward bias voltage of J1 ($V_S$) and base region doping ($V_{G2}$). The gain values are calculated at $V_D$=200mV where all the three currents are saturated to provide reasonable data.

![Figure 3.12: Three dimensional gain plot ($\beta$) as a function of $V_{G2}$ and $V_S$. The gain is calculated at $V_D = 200\text{mV}$]
From the dc characteristic we extract the maximum gain of 100 at $V_S=-100\text{mV}$. Increasing to $V_S=-300\text{mV}$, we note from Figure 3.11 that the gain remains unchanged. This suggests that gain is independent of $V_S$ which is further confirmed from Figure 3.12 where $\beta$ is nearly independent of $V_S$. For a fixed $V_S$ as we step $V_{G2}$ to low negative values (low $p$-type doping), $\beta$ increases further to achieve values greater than 100. The high gain value obtained at low $p$-type (less negative $V_{G2}$) behavior in the base is associated with decreasing $I_B$ due to reduced recombination in base. Higher $V_{G2}$ (more negative) increases the recombination current $I_B$ and thus gain decreases, since gain is inversely proportional to $I_B$.

Another feature of an $n$-$p$-$n$ transistor that controls the gain is the effective width of the quasi-neutral base region. The importance of base width can be explained by rewriting the current gain $\beta$ in terms of the transit time $\tau_t$ and minority carrier lifetime in the base region $\tau_n$. In steady state charge distribution, the excess charge $Q$ is recombines in $\tau_n$ seconds in the base region to provide a base current

$$I_B = \frac{Q}{\tau_n} \quad \text{... (3.11a)}$$

Again the excess charge $Q$ has $\tau_t$ seconds to go across the base region and get collected at the drain. Thus the drain current

$$I_D = \frac{Q}{\tau_t} \quad \text{... (3.11b)}$$

As previously defined in Equation 3.10, $\beta = I_D/I_B$ which when solved by substituting $I_D$ and $I_B$ from Equation 3.11 gives

$$\beta = \frac{\tau_n}{\tau_t} \quad \text{... (3.12)}$$
The current gain from Equation 3.12 implies that $\tau_n/\tau_t$ number electrons from the source can go across the base region to the drain for each hole that enters from the base terminal\(^4\). Thus to maximize gain transit time has to be reduced and lifetime should be increased.

To show the dependence of transit time $\tau_t$ on effective base width $W_B$ we revisit the assumption made in Section 3.1.1 where dc characteristic is defined for short base diode. When the diffusion length $L_n$ of the minority carriers (electrons for $n$-p-$n$) in the base is larger than the width of the base region, the minority carrier density $\Delta n$ varies linearly across the base (between source and drain)\(^1\). Moreover, since J2 (base-drain junction) is in reverse bias and drain doping is high n-type, we can neglect the number of holes travelling from drain into the base region. Thus minority carrier density at the edge of J2 can be assumed to be zero and the drain current is entirely composed of electrons crossing the base. The diffusion current is then given as

$$J_{diffusion} = qD_n \frac{dn}{dx} = qD_n \frac{\Delta n}{W_B} \quad ... (3.13)$$

Also diffusion current can be expresses in terms of average velocity of diffusing electrons $v_n$ as

$$J_{diffusion} = qv_n \frac{\Delta n}{2} \quad ... (3.14)$$

Here, $v_n = W_B/\tau_t$ to rewrite Equation 3.14 as

$$J_{diffusion} = q \frac{W_B \Delta n}{\tau_t} \quad ... (3.15)$$

Comparing Equations (3.14 and 3.15) we have
\[ \tau_t = \frac{W_B^2}{2D_n} \quad \cdots (3.16) \]

Putting this in \textbf{Equation 3.12} we get

\[ \beta = \frac{2D_n \tau_n}{W_B^2} = \frac{2L_n^2}{W_B^2} \quad \cdots (3.17) \]

Here \( L_n = \sqrt{D_n \tau_n} \) is the minority carrier diffusion length which is calculated later in the chapter to define the figure-of-merit of an \textit{n-p-n} WSe\textsubscript{2} transistor.

In addition, we perform finite-element-modeling to investigate the behavior of effective base width \( W_B \) with respect to the strength of \textit{p} type doping in the base region, in particular the dependence of \( W_B \) on \( V_{G2} \). In bulk transistors the effective base width modulates with the bias applied on drain \( V_D \). A larger reverse bias on base-drain junction reduces the effective base width which increases the drain current and subsequently the current gain\textsuperscript{9}. In our device where we employ electrostatic gating to dope the channel regions, the effective base \( W_B \) depends not only on \( V_D \) but also on the magnitude of \( V_{G1}, V_{G2}, \) and \( V_{G3} \). Higher doping on gates \( G1 \) and \( G3 \) influence the doping in the source-base and base-drain transition regions and thus influence the doping of the middle \textit{p}-type base. This suggests that the base region which ideally should be 100 nm wide may shrink to provide a smaller \textit{p}-type region; thus, the gain will change with \( V_{G2} \).

To determine the effective base region width (\( W_B \)) with change \( V_{G2} \) we used a commercially available finite element modeling tool (TCAD) which self-consistently solves partial differential device equations. Two-dimensional device structure was generated based on the actual dimensions of the real device with fine meshing of 10 nm (both \( x \) and \( y \)) and 300 nm of vacuum region placed on top as shown in \textbf{Figure 3.13}. The thickness of the semiconductor is 5 nm which is close to the
actual thickness of the material measured from AFM. Buried tungsten gates are 100 nm wide with 100 nm of gate spacing.

Figure 3.13: TCAD device model with three split gates 100nm apart. The vacuum region (light blue) is define on top of the device

Figure 3.14: Cross section of the device to show 2D electrostatic potential profile due to bias applied on three SGs
Simulation was performed by solving the Poisson equation with source and drain maintained at zero potential to study the device at equilibrium. The gate biases are $V_{G1}=2.5V$, and $V_{G3}=1.5V$ for varying $V_{G2}$ (0 to -0.45V) to create an n$^+$/p$^-$-n configuration. The contact metal is chosen by adjusting its work-function to bring the threshold voltage close to 0V. Using iterative method, the solver provides electron and hole densities in the semiconductor using a fixed quasi-Fermi potential. Figure 3.14 shows the 2D electrostatic potential map.

In Figure 3.15 we plot the hole density profile along the length of the semiconductor for different $V_{G2}$ values from 0V to -1.0V. For $V_{G2}=0V$, the hole density is very low and its profile does not appear in the plot. Increasing the gate voltage on G2 to more negative values increases the hole density. Also seen from Figure 3.15 is that the hole density profile grows laterally outward by making $V_{G2}$ more negative. This behavior is quite obvious because higher p-type doping in the base essentially reduces the effects of G1 and G3 in the base region. Hence the effective width of the quasi-neutral base region is modulated with $V_{G2}$.

![Figure 3.15: Hole number density along the semiconductor for different $V_{G2}$ values](image-url)
To calculate the effective width of the base region we study the hole density variation along the middle of the semiconductor and calculated its full-width half maximum FWHM at the base region. This is plotted as function of $V_{G2}$ (Figure 3.16). By making the middle region low p-type (low $|V_{G2}|$), $W_B$ decreases from 85 nm to ~47 nm and flattens out near the threshold voltage. At low doping, side gates ($V_{G1}$, $V_{G3}$) have more effect in the base region due to fringe fields which reduces $W_B$. Additionally, it can be seen that $W_B$ has almost a linear dependence with $V_{G2}$ ($W_B \propto |V_{G2}|$).

![Figure 3.16: Dependence of effective base width $W_B$ on bias applied on gate G2 ($V_{G2}$)](image)

The lifetime of electrons $\tau_n$ has inverses relationship on $|V_{G2}|$ $^{29}$. Higher $p$ doping in the base region increases the recombination current which makes $\tau_n \propto \left(\frac{1}{|V_{G2}|}\right)$. Placing the dependence of $W_B$ and $\tau_n$ on $V_{G2}$ in Equation 3.17 we get
$\beta \propto \left( \frac{1}{|V_{G2}|} \right)^3$ ... (3.18)

To show this dependence we plot in Figure 3.17 the extracted mean of the gain from Figure 3.12. The mean $\beta$ is calculated for each $V_{G2}$ averaged over all $V_S$ values since $\beta$ shows weak dependence on $V_S$. The data is fitted with Equation 3.18 with appropriate fitting parameters to confirm the inverse cube dependence of current gain on $p$-type doping in the base region. The maximum gain we obtain for our device is nearly 1000, which is significantly higher than that of silicon based bipolar junction transistors$^{30}$. In the inset of Figure 3.17 we show that $I_D$ and $I_B$ have linear dependence, which is an important aspect of a properly functioning BJT.
Next we calculate the minority carrier diffusion length $L_n$ to further confirm the origin of the high gain achieved in WSe$_2$ BJT. As stated earlier in Section 3.2.1 the short base assumption is used to analyze the fabricated $n$-$p$-$n$ transistor. This holds true for the situation when $L_n$ is larger than the effective base width in which case the excess charge varies linearly with position. We refer back to Equation 3.16 to calculate the diffusion length and minority carrier lifetime $\tau_n$. The mobility in WSe$_2$ is nearly $100 \text{ cm}^2/\text{V-s}^{31-32}$. We use Einstein relation\(^{33} D = \frac{KT}{q}$ with $\mu=100 \text{ cm}^2/\text{V-s}$ to obtain $D = 2.6 \text{ cm}^2/\text{s}$ at $T=300K$. Here K is the Boltzmann constant ($1.38 \times 10^{-23} \text{JK}^{-1}$). The maximum gain achieved in our device is $\beta = \tau_n/\tau_e = 10^3$ at low $|V_{g2}|$. The effective base width $W_B = 50nm$ at this doping from the finite element modeling. Using these values in Equation 3.17 we determine the minority carrier lifetime $\tau_n \sim 5 \times 10^{-9}$s. To calculate diffusion length of electrons we use $L_n = \sqrt{D\tau_n} \sim 10^{-4}$ cm (nearly 1µm). This explains the large gain obtained in WSe$_2$ BJT where electrons from source have a diffusion length that is longer than the effective base width, which is smaller than the width of the corresponding gate.

From the device design in Figure 3.6 it is noted that the base gate region G2 is comparable with the split gate spacing of $\sim 100$nm. It is tempting to argue that the ungated transition region can potentially modify the band structure to introduce intrinsic regions in between. To confirm that the ungated transition region has effective gating effect from G1, G2 and G3, we plot in Figure 3.18 the energy band diagram along the semiconductor. The obtained band structure from the finite element modeling is very similar to Figure 3.10 and it can be concluded that the ungated region does not introduce intrinsic regions.
Another important feature of a bipolar junction transistor is the exponential dependence of base current \( I_B \) and drain current \( I_D \) on the forward bias characteristic of source-base junction (J1).

In an ideal diode the applied voltage drops completely in the junction region and the effects due to
series resistance and all the other parasitic resistances are negligible. Under these conditions the forward bias characteristic of an ideal diode depends exponentially on the applied external voltage\(^4\). In Figure 3.19 we show the current-voltage characteristic of \(I_B\) and \(I_D\) with applied voltage \(V_{BS}\). Both \(I_B\) and \(I_D\) have exponential dependence on \(V_{BS}\) over a certain range. The ideality factor \(n > 1\) is consistent with the individual diode characteristics.

### 3.3.2 Phototransistor characteristics

This section describes the phototransistor properties of the device which has been previously used in Section 3.3.1 as a bipolar junction transistor. The working principles of a phototransistor is quite similar to that of the bipolar junction transistor. The phototransistor works in the forward active region when the source-base junction is forward biased and base-drain junction is reverse biased. In the BJT we forward biased \(J1\) to demonstrate gain where as in a phototransistor a similar operation is accomplished by shining light\(^{34}\). Typical phototransistors have light absorption region and are generally two terminal devices with a floating base contact. In a two-terminal configuration the base does not draw any current \((I_B=0)\). There are reports of three terminal operation where an active base is present to enhance the performance of phototransistors\(^{35-36}\).

We now discuss the operation of an \(n-p-n\) phototransistor using the electrostatic doping mechanism. The two terminal mode of operation is presented where the base terminal is floating and only light is allowed to control the potential of the base\(^7\). The equilibrium energy band diagram of an \(n-p-n\) configuration in dark (black curve) is shown in Figure 3.20 for \(V_S = V_D = 0\). The incident light generates electron-hole pairs (EHPs) in the source-base and the base-drain regions. For an \(n-p-n\) case shown in Figure 3.20 the photo-generated electrons travel down the barrier and are collected at the drain and source regions. Holes on the other hand travel upward and are
collected at the base. The photo-generated holes build up the positive charge at the base and forward bias both junctions when \( V_D = 0 \)V. The energy barrier at J1, which was previously large, is now lowered due to the photo-generated holes collected at the base. The red curve in Figure 3.20 shows the illuminated energy band diagram which is lower than the one in dark because positive charge in the base essentially lowers the potential energy of the base region by \( \Delta E \). The total current after illumination is zero which is obvious because the total electron current and hole currents are zero.

To operate an \( n^+\text{-}p\text{-}n \) phototransistor we study two cases shown in Figure 3.21. In one case the base-drain junction is forward biased and in the other situation base-drain junction is reverse biased. The band diagram in the figure has the source terminal grounded and the drain terminal is used to study the current-voltage characteristics of the phototransistor. The \( n^+\text{-}p\text{-}n \) configuration has the same doping profile as used previously for the bipolar junction transistor in Section 3.3.1. The source doping is significantly larger than the base doping to efficiently inject electrons into
the device. The base doping is low to minimize the recombination current due to holes from the base. The drain region is moderately biased. We note in the band diagram in Figure 3.21 that the base is modeled as a virtual ground, which will be explained later in the chapter when we introduce the capacitance model to explain the current-voltage characteristics. The band diagrams in Figure 3.21 will be used to explain the current-voltage characteristics of the phototransistor.

![Band diagrams](image)

**Figure 3.21:** (a) Band diagram for the case when J2 is reverse biased under light, (b) band diagram when J2 is forward biased under light

The current-voltage characteristics of an $n^+\cdot p\cdot n$ are shown in Figure 3.22. Here $I_D$ is the source-drain current and $V_{DS}$ is the bias voltage applied on the drain terminal; the source terminal is
grounded and the base terminal is not connected. To generate the $I-V$ characteristic under illumination we use light source of wavelength $\lambda=658\text{nm}$ at different intensities. The drain voltage $V_D$ is swept from 500mV to -300mV with absolute current shown on the y-axis. The dark $I-V$ characteristic is shown in black circles, which serves as a baseline data to help characterize the phototransistor performance. Under illumination ($\lambda=658\text{nm}$), electron hole pairs are generated and the base is populated with the holes. The increased number density of holes in the base region increases the effective reverse leakage current of the phototransistor when $V_D>0$ (base-drain junction reverse biased) and we see large current flowing into the device (red circle for power density $= 2.5\text{mW/cm}^2$). For the same power density when drain bias is made negative (base-drain junction forward biased), current values are higher than the dark characteristics. Moreover, the current values are larger than when the base-drain junction is reverse biased ($V_D<0$). This suggests that the current-voltage characteristics of the phototransistor are controlled by the bias applied on the drain terminal and there is a characteristic asymmetry present, which is not expected.

The two situations are also shown in terms of band diagrams under illumination in Figures 3.21b and c. From Figure 3.21b we note that when the base-drain junction is reverse biased, the potential at the base region is pinned to the source terminal (constant fermi-level in source-base region) and does not considerably forward bias the source-base junction. There is definitely increase in current for $V_D>0$ due to EHPs but the barrier at the source-base junction is not lowered as a result of the bias to allow a large number of electron injection from the source region. The pinning of the base potential can be understood by using the capacitance model that is introduced later in the chapter. For the case in Figure 3.21c under illumination, base-drain junction is forward biased which further lowers the potential energy barrier to allow injection of electrons from drain. This allows a large number of electrons to travel across the base region and collected at the source. The large
current observed for $V_D<0$ results in an asymmetry in the current-voltage characteristic, which further confirms that the base is effectively grounded.

Progressively stepping up the intensity of the light increases $I_D$ for both $V_D>0$ and $V_D<0$. At higher light intensity the number of holes building up in the base region increase, which with their positive charge lowers the potential energy barrier at source-base junction further to increase the flow of electrons from source to drain ($V_D>0$) or from drain to source ($V_D<0$). The characteristic asymmetry in the $I$-$V$ characteristic is still present and is independent of the light intensity. Finally, another important feature of a successful phototransistor is the absence of open-circuit voltage which means that $I_D$ switches sign or achieves a minimum value at zero drain bias\textsuperscript{37}. When $V_D=0$ the photo-generated EHPs contribute equal currents in both junctions J1 and J2 to provide negligible total current. This feature is clearly observed in Figure 3.22 where all currents at different intensities achieve minimum value at $V_D \approx 0\,V$.

Assuming that the base potential is pinned, we can now derive the phototransistor current. In Figure 3.21 we considered base region to be at a virtual ground which means that with $V_D>0$, source-base will not be forward biased and the base-drain junction is reverse biased with $V_D>0$. Under illumination, the phototransistor current can be written as

$$I_{DS} = I_O^{light} \left( e^{-qV_{DS}/nkT} - 1 \right) - I_{PN,1} + I_{PN,2} \quad \ldots (3.19)$$

Here, $I_{PN,1}, I_{PN,2}$ are the photo-generated currents in junctions J1 and J2. Considering the largely symmetrical junctions, the photocurrents cancel each other and there is no open circuit voltage associated with the phototransistor ($I_{PN,1} = I_{PN,2}$).

The effective diode leakage current under illumination is given as
Here \( I_o \) is the diode leakage current for J2 in the dark and \( \Delta E \) is the lowering in energy barrier due to illumination, as shown in Figure 3.20.

\[
I_o^{\text{light}} = I_o e^{\Delta E / kT} \quad \ldots (3.20)
\]

In the absence of illumination, when \( \Delta E = 0 \) we obtain from Equations 3.19 and 3.20 the standard diode equation for base-drain junction as

\[
I_{DS} = I_o \left( e^{-qV_{DS}/nkT} - 1 \right) \quad \ldots (3.21)
\]
In a defect free material, we can write $\Delta E$ as

$$\Delta E = K T \ln \left( \frac{p}{p_0} \right) \quad \ldots (3.22)$$

Here $p$ and $p_0$ are the hole densities in the base region with and without illumination, respectively.

Using Equation 3.22 in Equation 3.20 we get

$$I_{O}^{light} = I_{0} \frac{p}{p_0} \quad \ldots (3.23)$$

Putting Equation 3.23 in Equation 3.19 we finally get

$$I_{DS} = I_{0} \left( \frac{p}{p_0} \right) \left( e^{-qV_{DS}/n k T} - 1 \right) \quad \ldots (3.24)$$

This equation is used to fit the measured current-voltage characteristic in Figure 3.22 at different light intensities. The ideality factor $n=2$ for all the fits. Equation 3.24 also explains the asymmetry observed in the phototransistor characteristic. The virtual ground thus results in a diode-like behavior, which is similar to the BJT characteristics observed in Figure 3.11 with the exception that in the case of phototransistor the leakage current depends on light intensity. The inset in Figure 3.22 shows that the leakage current increases linearly with intensity to validate Equation 3.23.

In Figure 3.23 we show the current-voltage characteristics of the corresponding photodiode. The photodiode is formed by switching the polarity of gate G3 ($V_{G3}<0$) while maintaining the same potential on the other gates. The photodiode created in this manner has $n^+\text{p}^-\text{p}^-\text{p}^-$ configuration. The $I-V$ characteristics are measured in dark and under illumination in a similar fashion as used for phototransistor in Figure 3.22. The $n^+\text{p}^-\text{p}^-\text{p}^-$ configuration has the characteristic diode behavior with all the features of a photovoltaic device. Under illumination the reverse saturation current
increases with intensity. Moreover, we observe the sizable open circuit voltage $V_{OC}$ ($I_D=0$) for $V_D>0$ which scales with intensity. At $V_{DS}=0$, there is a finite current flowing in the device which also scales with intensity. The electron hole pairs generated in the presence of light are collected at respective terminals due to built-in electric field and this is seen as the short-circuit current $I_{SC}$ at $V_{DS}=0V$.

To further demonstrate the advantage of electrostatic gating technique we plot in Figure 3.24 the doping dependent current-voltage characteristic of phototransistor and photodiode at one particular wavelength $\lambda=590\text{nm}$. To generate this three-dimensional plot for $n^+-p^--n$ phototransistor, shown

![Image](image-url)
as blue, we fixed the source and drain doping ($V_{G1}$, $V_{G2}$ fixed) and swept the drain voltage $V_D$ while stepping $V_{G2}$ from -500mV to 0V. Corresponding diode profile is generated for $n^+p^-p^-$, shown as red map, by fixing $V_{G1}$ and simultaneously stepping $V_{G2,G3}$ while sweeping $V_D$. The $V_{OC}$ profiles are shown as blue dots at the bottom for phototransistor and red dots for photodiode. The open-circuit voltage is close to zero for phototransistor and has negligible doping dependence. For photodiode there is considerable $I_{SC}$ and $V_{OC}$ which have weak dependence on $V_{G2}$. An interesting aspect of the doping dependent $I$-$V$ plot of phototransistor is the presence of characteristic asymmetry for all doping values. Thus for any $n^+p^-n$ base doping configuration, $I$-$V$ characteristic is governed by the bias applied on drain to show diode like behavior.

The gain of the phototransistor is defined as the ratio of the drain current to the current associated with either of the two diodes (source-base or base-drain)$^{38}$. This implies for any specific illumination

![Figure 3.24: $I$-$V$ characteristic of doping dependent $n^+p^-n$ phototransistor (blue) and $n^+p-p$ photodiode (red) at $\lambda = 590nm$ with open circuit voltages in blue and red circles respectively](image-url)
\[ \beta_{\text{photo}} = \frac{I_{DS}^{NPN}}{I_{PN,1}} \quad \ldots (3.25) \]

The photocurrent gain \( \beta_{\text{photo}} \) is similar to the current gain \( \beta_{\text{DC}} \) of the bipolar junction transistor which is the amplification obtained by forward biasing one of the junctions. In case of phototransistor, amplification is of the photo-generated current.

Using the gain definition from Equation 3.25, we plot in Figure 3.25 the photocurrent gain \( \beta_{\text{photo}} \) as a function of \( V_D \) while stepping \( V_{G2} \) under \( \lambda=590\text{nm} \) photon illumination. This plot is generated from Figure 3.24 by taking the ratio of phototransistor current and the reverse saturation current of the photodiode. In general, for any typical phototransistor large current gain occurs for \( V_D > 0 \) when source-base junction is forward biased. From Figure 3.25 it is observed that photocurrent gain is quite small (\( \beta_{\text{photo}} \approx 5 \)) when \( V_D > 0\text{V} \). This is expected based on the reasoning that for \( V_D > 0 \), source-base junction is not forward biased and the base potential is pinned at a virtual ground.

For \( V_D < 0 \) in Figure 3.25, base-drain junction is forward biased and large gain is observed. The maximum gain obtained (\( \beta_{\text{photo}} \approx 40 \)) is significantly lower than the current gain observed when the same device is behaved as bipolar junction transistor which is due to the large ideality factor \( (n > 1) \). The diode like behavior is characteristic of our device and this behavior is clearly seen in Figures 3.22 and 3.24.

Due to electron-hole pair generation in the presence of light, holes diffuse from source and drain into the base. We call the steady state hole density as \( p \). Using Equation 3.25 and assuming \( \tau_n = \tau_p = \tau \) we can write

\[ \beta_{\text{photo}} = I_0 \left( \frac{\tau}{qP_0} \right) \left| e^{-qVDS/nkT} - 1 \right| \quad \ldots (3.26) \]
Here \( p'_0 \) is the total hole carrier density in the base region. From Figure 3.25 we conclude that the prefactor \( I_0 \frac{(\tau_q)}{q p'_0} \) is \( \sim 1 \). Using this lifetime, we arrive at \( p_0 \sim 10^9/\text{cm}^2 \) at low doping regime. From Equation 3.26, we see that for \( V_{DS} < -3nKT/q \), \( \beta_{\text{photo}} \sim e^{-qV_{DS}/nkT} \) which further explains the characteristic asymmetry observed in the gain plot (Figure 3.25).

![Figure 3.25: Doping dependent photocurrent gain (\( \beta_{\text{photo}} \)) obtained from Equation 3.25](image)

We observed in Figures 3.24 and 3.25 that positive bias applied on drain side does not forward bias the source-base junction and negligible gain is observed for \( V_D>0 \). We now introduce the capacitance model to explain the pinning of the base potential when \( V_D>0 \). To explain the dependence of base potential \( V_B \) on drain bias \( V_D \), we study the circuit diagram for the device under test based on elemental capacitances shown in Figure 3.26a.

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Capacitors $C_{G1}$, $C_{G2}$ and $C_{G3}$ are associated with the three split gates and $C_{SB}$ and $C_{DB}$ are the parasitic capacitances between source-base and base-drain junctions respectively. They are expected to be smaller than the gate capacitances. The source potential is grounded and the base terminal is floating. The circuit simplifies from Figure 3.26a to in the one shown in Figure 3.26b.

We get

$$V_B = \frac{C_{DB}}{C_{G2}} V_D \quad \ldots (3.27)$$

The ratio $C_{DB}/C_{G2} \ll 1$ and the hence base potential can be considered as a virtual ground. This model satisfactorily explains the current-voltage characteristics of an $n^+\textit{-}p^-\textit{-}n$ phototransistor.
Figure 3.27: Intensity dependent $I$-$V$ characteristic of $n$-$p$-$n$ phototransistor

Figure 3.28: Band diagram of $p^+$$-n$$-p$ phototransistor when $J_2$ is forward biased (top), and when $J_2$ is reverse biased (bottom)
Until recently we studied the $I$-$V$ characteristic of an $n$-$p$-$n$ phototransistor and found that observed diode like behavior occurs mainly due to the pinning of the base potential. We confirmed from Figures 3.22 and 3.24 that the asymmetry in $I$-$V$ is not related to the intensity of light and neither depends on the base region doping. We explained this phenomenon using the capacitance model in Figure 3.26. To further support this argument we studied a symmetric phototransistor configuration by creating a symmetrically doped $n$-$p$-$n$ structure where source and drain doping values are equal ($V_{G1}=V_{G3}=2\,\text{V}$).

The base doping is $p$-type ($V_{G2}=-1\,\text{V}$). Figure 3.27 shows $I$-$V$ characteristic of the symmetric $n$-$p$-$n$ phototransistor in dark and under different light intensities ($\lambda=658\,\text{nm}$). It is quite interesting to notice that the asymmetry exists and continues to be independent of the doping configuration (end gates in this case).

**Figure 3.27:** $I$-$V$ characteristic of $p$-$n$-$p$ phototransistor (blue) and $p$-$p$-$n$ photodiode shows characteristic asymmetry in phototransistor

![Graph showing I-V characteristics](image-url)
The reconfigurability of the device allows us to extend the phototransistor configuration from \textit{n}-\textit{p-n} type to \textit{p-n-p} type. To form \textit{p-n-p} phototransistor all the gate polarities are reversed at source, base, and drain regions. From the band diagram in \textbf{Figure 3.28} under illumination, electrons are collected in the base region which due to their negative charge forward bias the source-base junction. When J1 is forward biased in presence of light, the energy barrier is lowered for holes coming from the source and current amplification is expected. Like \textit{n-p-n} case both cases are shown in \textbf{Figure 3.28} where in first case J2 is reverse biased and for second case J2 is forward biased.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{image}
\caption{Doping dependent photocurrent gain ($\beta_{\text{photo}}$) for \textit{p$^+$-n-p} phototransistor obtained from Equation 3.25}
\end{figure}

The current-voltage characteristics of a \textit{p$^+$-n-p} phototransistor and its corresponding diode \textit{p-p-n} are shown in \textbf{Figure 3.29}. For phototransistor there is almost zero open circuit voltage. The drain current is larger for the case when base-drain junction is forward biased ($V_D>0$) compared to the case where base-drain junction is reverse biased ($V_D<0$). This suggests asymmetry in the \textit{I-V}
characteristics and the current in device is again controlled by the drain voltage. Similar diode like behavior has been previously observed for n-p-n phototransistor in Figure 3.27. The photodiode under illumination has finite short-circuit current $I_{SC}$ and open-circuit voltage $V_{OC}$.

Finally, in Figure 3.30 we plot the doping dependent photocurrent gain for $p^+-n-p$ phototransistor calculated using Equation 3.25. The maximum photocurrent gain $\beta_{\text{photo}} \sim 15$ is achieved for $V_D>0$.

### 3.4 Summary

In summary, we demonstrate the first bipolar junction transistor along with phototransistor on a two-dimensional TMD material WSe$_2$. We used electrostatic gating technique to selectively dope the device regions. For phototransistor the base terminal is floating to allow the light to modulate the base potential. The highest current gain achieved in our device is $\sim 1000$ with photocurrent gain $\sim 40$. 
References:


Chapter 4

THREE FUNDAMENTAL DEVICES IN ONE: A RECONFIGURABLE TWO-DIMENSIONAL DEVICE USING WSe$_2$

4.1 Introduction

The invention of the bipolar junction transistor$^3$ by Shockley started the semiconductor industry and enabled device scaling technology to support Moore’s law$^4$. Gordon Moore predicted in 1965$^4$ that in an integrated circuit the number of transistors would double every two years. It has been observed that reducing the size of an electronic device leads to reduced device performance due to short channel effects$^5$. To control the short channel effects, one method is to reduce the thickness of the channel material by using ultra-thin body$^6$-$^7$ or silicon on insulator box techniques. Here, we used one candidate, tungsten diselenide, from a family of transition metal dichalcogenides which has a band gap$^8$-$^9$ (unlike graphene) and can exist in a two-dimensional monolayer form to provide ultra-thin body channel. Another advantage of these materials is that they are compatible with CMOS processing$^{10}$.

In this work we demonstrate a WSe$_2$ based semiconductor device which can dynamically reconfigure to perform different tasks. In CMOS architecture this kind of device is difficult to implement. The three main fundamental operations required in modern integrated circuits are: rectification, switching, and current amplification. The devices corresponding to these tasks are the $p$-$n$ junction, MOSFET, and bipolar junction transistor (BJT), respectively. We fabricated one
such device that efficiently performs all the three different tasks. The scope of this research is to provide an alternative method to increase device functionality. Our device does not address the scaling issue but its reconfigurability mechanism can be used in the future to implement complex computations with fewer devices.

Electrostatic doping mechanism\textsuperscript{11} is used by placing three buried tungsten coplanar gates under the semiconductor and the bias applied determines the polarity of the channel. The gates are reconfigurable to change the doping region from \textit{p}-type to \textit{n}-type or vice-versa. Using this gating method we demonstrate a reconfigurable device to show \textit{p-n} junction, MOSFET and finally BJT. To link the device properties of the three devices we use a single material parameter, the interface trap density of states, to analyze them.

### 4.2 Materials and Methods

The device is identical to the one described in Section 2.2 with three coplanar buried gates (G1, G2, and G3) and three metal electrodes (source, base, and drain). Figure 4.1 shows the AFM image of the flake.

![AFM image of the flake with thickness along the red line ~ 10nm](image)

\textbf{Figure 4.1:} AFM image of the flake with thickness along the red line ~ 10nm
4.3 Results and Discussions

4.3.1 Electrical Characterization of Reconfigurable Device

Figure 4.2 shows the transfer characteristic of the device to confirm ambipolar transport. In the future graphene can be used as a contact metal because it can be doped\textsuperscript{12-13} and its Fermi level can be tuned depending on the carrier concentration. To study the three different types of devices (diode, field effect transistor, and bipolar junction transistor) we follow the biasing configurations summarized in Table 1.

\begin{center}
\begin{tabular}{|c|c|}
\hline
Device Type & Biasing Configuration \tabularnewline
\hline
Diode & $V_{ds} = 0.1V$ \tabularnewline
\hline
Field Effect Transistor & $V_{gs} = 0V$, $V_{ds} = 0.1V$ \tabularnewline
\hline
Bipolar Junction Transistor & $V_{ce} = -0.1V$, $V_{be} = 0V$ \tabularnewline
\hline
\end{tabular}
\end{center}
Table 1: Examples of bias configurations used to achieve different device types

<table>
<thead>
<tr>
<th>Devices</th>
<th>Bias Configurations for $V_{G1}$, $V_{G2}$, $V_{G3}$</th>
<th>Circuit Symbols</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p-n$ diodes</td>
<td>$p-p-n$ (Source-Drain; Base floating): $V_{G1}=V_{G2}=-2.0, V_{G3}=0.2$</td>
<td>![Diode Symbol]</td>
</tr>
<tr>
<td></td>
<td>$n-p-p$ (Source-Drain; Base floating): $V_{G1}=0.2, V_{G2}=V_{G3}=-2$</td>
<td>![Diode Symbol]</td>
</tr>
<tr>
<td>MOSFETs</td>
<td>$n$-MOSFET: $V_{G1}=V_{G3}=2.5, V_{G2}=$ gate</td>
<td>![MOSFET Symbol]</td>
</tr>
<tr>
<td></td>
<td>$p$-MOSFET: $V_{G1}=V_{G3}=-2.5, V_{G2}=$ gate</td>
<td>![MOSFET Symbol]</td>
</tr>
<tr>
<td>BJTs</td>
<td>$n-$+$-p-n$ (the heavily doped region is source): $V_{G1}=2.5, V_{G2}=-0.2, V_{G3}=1.5$</td>
<td>![BJT Symbol]</td>
</tr>
</tbody>
</table>

Table 1: Summary of the device when reconfigured as a diode, MOSFET, and BJT along with their circuit symbols

4.3.1.1 Diode Characteristics

For diodes we form $p-p-n$ ($V_{G1}=V_{G2}=-2V, V_{G3}=-0.2V$) and the corresponding $n-p-p$ ($V_{G1}=-0.2V, V_{G2}=V_{G3}=2V$) configuration while keeping the middle region fixed as p-type. The diode properties are studied between source-drain terminals with floating the base contact. The current-voltage
characteristics \((I_{DS-VDS})\) from Figure 4.3 show that WSe\(_2\) has rectifying behavior for both \(p-p-n\) (red dotted curve) and \(n-p-p\) (blue dotted curve) configurations with forward current \(I_{DS}\) that increases exponentially with \(V_{DS}\). The symmetry in the diode curves explains that rectification occurs from the junction region and not from the Schottky contacts which are unlikely to be symmetric.

The fit to the measured current-voltage characteristic was performed using the Shockley diode equation with adjustments to include the effects of trap assisted recombination in the junction region. For this case, \(I_{DS} = I_o \left( e^{q(V-R_S)/nkT} - 1 \right) \) where \(I_o\) is the reverse saturation leakage current, \(R_S\) is the series resistance, \(n\) is the diode ideality factor, \(k\) is the Boltzmann’s constant, and

![Figure 4.3: Diode characteristics of \(p-p-n\) (blue circles) and \(n-p-p\) (red circles) along with the fits (solid lines with corresponding color)](image)
$T$ is the temperature. The diode ideality factor $n$ equals to 1 for an ideal diode when negligible electron-hole recombination occurs in the junction region. It can achieve values from 1 to 2 based on the recombination rate with higher values for large recombination in the junction region. We extracted $I_o$, $R_S$ and $n$ by fitting the diode equation to the measure data (solid red and blue curves). The $n$ for $p$-$p$-$n$ ($n$-$p$-$p$) diode is $\sim 2.6$ ($3.0$) which is higher than the value for an ideal diode and is associated with the recombination due to defects. In Chapter 3 we showed diode with $n=1.3^{14}$.

4.3.1.2 Field Effect Transistor Characteristics

The distinguishing feature of our device is the reconfigurability. By rearranging the bias polarity applied on the split gates we are able to convert the same device (previously used for a diode) into a MOSFET which is the building block for a CMOS inverter. There are previous reports of TMDC FETs$^{15-17}$ which typically use global back gate to control the carrier type and density in the channel region. This adversely affects the transfer characteristic by simultaneously modulating the metal-semiconductor Schottky barrier.

To mitigate this effect, we use doped end contacts (source and drain) by using gates G1 and G3, which are biased high to reduce the Schottky tunneling barriers so that the tunnel barrier is largely ohmic$^{18}$. The true charge transport property of the channel can now be successfully studied by changing the gate bias on G2.

In our work we demonstrate $p$-channel and $n$-channel FETs, the two basic ingredients of a CMOS logic switch. For $p$-channel FET source-drain regions are created as $p$-type ($V_{G1}, V_{G3} < 0$) for hole injection and for $n$-channel electrons are injected by making $n$-type ($V_{G1}, V_{G3} > 0$) region under the source-drain. The biasing configuration is tabulated in Table 1 with $V_{G1}=V_{G3}=-1.5V$ for PFET and $V_{G1}=V_{G3}=1.5V$ for NFET with sweeping $V_{G2}$. Figure 3 shows $I_{DS}$-$V_{G2}$ transfer characteristics of an
$n$-channel and a $p$-channel FET at different source-drain bias $V_{DS}$. In NFET, source-drain current is very small ($I_{DS} \sim 10pA$) for $V_{G2}<0$ and transistor is in the off state. Applying a positive bias on G2 ($V_{G2}>0$), electrons are populated into the channel which reduces the potential barrier at G1/G2 and G2/G3 regions for electrons. At a fixed bias of $V_{DS} = 100mV$ on drain, electrons are injected into the channel and $I_{DS}$ increases for positive $V_{G2}$. At high $V_{G2}$, $I_{DS}$ saturates due to the series resistance, which includes the channel and the contact resistances. Changing the drain bias $V_{DS}$ shows no apparent change is the subthreshold $I_{DS}$-$V_{G2}$ characteristics.

![FET characteristics](image)

**Figure 4.4:** FET characteristics ($p$FET and nFET) at different $|V_D|$ values, along with their band structures. The subthreshold slopes are 117 and 120mV/decade respectively.

The subthreshold slope (SS) extracted for this configuration is 117mV/decade with an on/off current ratio of nearly $10^4$. The FET has $n\sim2$, obtained using the equation $SS =$
(60mV/decade) * n. A value for n larger than 1, for both FETs and diodes, reflects defect mediated transport. For the PFET, on the other hand, the off state occurs for $V_{G2}>0$ with $I_{DS}$ which ranges from 20pA to 200pA. Increasing the negative bias on G2 ($V_{G2}<0$) makes the channel conducting by attracting holes. $I_{DS}$ increases until it is limited by the series resistance. The subthreshold slope and on/off current ratio obtained for this configuration are 120mV/decade and $10^5$ at $V_{DS} = -0.1V$. Comparing Figures 4.2 and 4.4 we note that there is a significant improvement in the subthreshold slopes for PFET and NFET. This suggests that sweeping all the three gates together (Figure 4.2) essentially modulates the metal-semiconductor Schottky barrier and the true channel transport property is not captured; hence the subthreshold slope degrades when the Schottky contacts are modulated.

### 4.3.1.3 BJT Characteristics

We can further extend the gate reconfigurability to create the third kind of device, the bipolar junction transistor (BJT) as was discussed in Chapter 3. Even though current microelectronics is dominated by CMOS, BJTs still have wider applications in analog circuits, communication and power systems. With the ongoing research on novel 2D materials, realization of bipolar junction transistors on TMDs make it even more significant.

A detailed discussion of BJT has been provided in Chapter 3. Here we briefly discuss the current-voltage characteristics of the reconfigurable device when operated as a BJT. For our work we consider an $n-p-n$ type of transistor which is formed by making source-drain as $n$-type ($V_{G1}, V_{G3}>0$) and base as $p$-type ($V_{G2}<0$). We refer the source-drain junction as J1 and base-drain junction as J2. In normal operation J1 is forward biased and J2 is reverse biased which turns on the $n-p-n$ transistor. With forward biased J1 electrons are injected from the source into the base. These
electrons diffuse toward the drain giving rise to the drain current. Holes are injected from the base which either diffuse toward the source or recombine with the injected electrons from source, giving rise to the base current.

![Diagram](image)

\[ \beta = \frac{I_D}{I_B} = \frac{\tau_0}{\tau_1} \]

\( V_D \) (V)

\( I \) (A)

\( V_G2 \) (V)

\( V_S \) (V)

**Figure 4.5**: (Top) I-V characteristics with currents from all three terminals at different \( V_S \) values, (bottom) 2D contour plot of the current gain as a function of \( V_S \) and \( V_G2 \)

The main objective of the bipolar transistor is to maximize the drain current which is achieved by making the source doping high to efficiently inject electrons into the base. **Figure 4.5 (top)** shows the absolute current from all the three terminals (\( I_S, I_B \) and \( I_D \)) versus \( V_D \) for different \( V_S \) values. A
two-dimensional contour plot of gain $\beta$ (calculated at $V_D=200mV$) for an array of $V_{G2}$ and $V_S$ values is shown in Figure 4.5 (bottom).

4.3.2 Device Analysis

To understand the characteristic of each device we use a single parameter, the interface defect density of states $D_{it}$, which plays an important role in the generation-recombination processes, to characterize all three devices. It should be noted that all the three devices are surface conducting and hence it is meaningful to use the interface trap density of states to understand the figure-of-merit of all three devices.

We start with the diode analysis. We use the Shockley-Read-Hall model\textsuperscript{19-20} to determine the reverse saturation current density $J_o$. The SRH model is described in Section 4.5 of this chapter. For a non-ideal diode $J_o = qx_dU$ where $x_d$ is the depletion width of the junction and $U$ is the generation rate of carriers. From Sze\textsuperscript{21} we have

$$U = \int D_{it} v_{th} \sigma n_i \, dE/2 \cosh\left(\frac{E}{k_B T}\right) \quad (4.1)$$

Here $\sigma$ is the capture cross-section $v_{th}$ is the thermal velocity, and $n_i$ is the intrinsic carrier density. Equation 4.1 can be solved to provide

$$U = \pi k_B T D_{it} v_{th} \sigma n_i / 2 \quad (4.2)$$

From SRH we find that generation is most efficient when the localized states are near the middle of the band gap. Thus we ascribe $N_t$ as the density of trap states which is equal to $\pi k_B T D_{it}$. We take $v_{th} = 10^7 \text{ cm/s}$ and $\sigma = 2 \times 10^{-15} \text{ cm}^2$, for typical semiconductor\textsuperscript{21} and $x_d = 10^{-5} \text{ cm}$ which is the spacing between the two adjacent gates. In our analysis we assume bulk characteristics.
of WSe$_2$ flake. From AFM image in Figure 4.1 we determined the flake thickness to be 10nm which is thick to exhibit bulk characteristics. Moreover, for thicker flake the band gap does not change with thickness\textsuperscript{22}. We calculated intrinsic carrier density $n_i = 2 \times 10^{10} cm^{-3}$ for bulk semiconductor with band gap as 1.2eV\textsuperscript{21}. From the MOSFET characteristic we obtained $D_{it} = 2 \times 10^{12}/eV cm^2$ which is further discussed later. Using the values of $v_{th}, \sigma, n_i, D_{it}$ in Equation 4.2 we get $I_o \sim 10^{-14}$ for a device with a width of 2µm. The achieved value of $I_o$ is close to the leakage currents we see in our diodes (Figure 4.3).

Further from SRH theory we can write the generation rate as $U = Sn_i$, where $S = \pi k_B T D_{it} v_{th} \sigma / 2$ is the surface recombination velocity\textsuperscript{23}. We calculated $S = 1.6 \times 10^3 cm/s$, which is typical for many semiconductors\textsuperscript{21}. To calculate the minority carrier lifetime, we use $\tau_0 = d / 2S$, where $d$ is the thickness of the flake. For our device with $d = 10nm$, we calculated $\tau_0 = 3 \times 10^{-10} s$. This recombination lifetime will be used later to relate to the current gain of BJT.

From the MOSFET characteristics we observe that in the subthreshold region $I_{DS} \sim \exp(q|V_{G2}|/nk_BT)$. Unlike the diode characteristics there is a unipolar conduction in field effect transistors with almost similar expression for $I_{DS}$ . With channel potential defined as $\varphi_s$ we have $I_{DS} \sim \exp(q \varphi_s/k_BT)$, where $q \varphi_s$ is the potential energy barrier for the electrons coming from the source. The equivalent circuit relating $\varphi_s$ to the gate potential $V_{G2}$ is shown in Figure 4.4, with the inclusion of effects from $D_{it}$. The equivalent circuit has $C_{ox}$ for the gate capacitance and an additional capacitance $C_{it} = q^2 D_{it}$\textsuperscript{24} to consider the charge trapping centers at the interface. We can rewrite $\varphi_s = V_{G2} / (1 + C_{it}/C_{ox})$ from the equivalent capacitance circuit where the factor $n = 1 + C_{it}/C_{ox}$. Additionally, at room temperature the inverse of subthreshold slope is defined as $SS = \frac{dV_{G2}}{d(\log(I_{DS}))}$, i.e. $SS = (60n) \frac{mV}{decade}$. For the p-channel and n-channel MOSFETs we obtained
SS values as 117mV/decade and 120mV/decade, respectively, which give $n \sim 2$ for both FETs. This means that the capacitance due to interface traps is nearly equal to oxide capacitance ($C_{it} = C_{ox}$). For our device the gate dielectric capacitance is $C_{ox} = 3 \times 10^{-7} F/cm^2$, from which we calculate $D_{it} = 2 \times 10^{12} / eVcm^2$. This $D_{it}$ value was used earlier to analyze the reverse leakage current of diodes and to calculate the lifetime of minority carriers.

We can extend the discussion to link $D_{it}$ to the BJT current gain. In our analysis from Chapter 3, we calculated $\tau = 5 \times 10^{-12} s$ using mobility value of $\mu=100 \ cm^2/Vs$ $^{14; 25-26}$. At minimum conductivity in Figure 4.5, $\beta \sim 50$ which is the same gate voltage used to calculate the $D_{it}$ for the FETs in Figure 4.4. This gives us $\tau_0 = 2.5 \times 10^{-10} s$, which is nearly what we obtained as $\tau_0 = 3 \times 10^{-10} s$ from the diode analysis.

### 4.4 Summary

In summary, we created a device which is reconfigurable to perform the functions of three fundamental devices i.e. p-n junction for rectification, FET for switching and BJT for current amplification. We use the interface density of states to unify the characteristics of the three devices.
In this section we describe the Shockley-Read-Hall theory which is used to unify the three device characteristics (rectification, switching and amplification) based on the interface defect density of states of TMD films. The theory discussed here is based on equations reproduced from [Taur\textsuperscript{27}, Muller\textsuperscript{23}, Schröder\textsuperscript{24}, Streetman\textsuperscript{28}, Sze\textsuperscript{21}]. In a perfect semiconductor crystal, there are no quantum mechanically allowed energy levels between the conduction band and the valence band. With the introduction of defects into the crystal structure discrete energy levels appear the band gap. These energy levels become generation or recombination sites for minority carriers. These centers may lie deep in the band gap, which are called as deep-level impurities, and may lie at the interface. In a reverse biased $p$-$n$ junction, the carrier number density in the space-charge region is below the equilibrium value, and these centers act as generation sites. Moreover, when there are excess carriers present in the semiconductor these deep level impurities then act as centers of recombination.
Figure 4.6 illustrates the generation-recombination process for a deep-level impurity. We consider a uniform distribution of impurities with total number density $N_T$ (impurities/cm$^3$) at energy $E_T$. Also there are $n$ electrons/cm$^3$ and $p$ holes/cm$^3$ present in the semiconductor. We first consider an electron in the conduction band that is captured by the impurity site with the capture coefficient of $c_n$. After this event there are two possibilities for the captured electron. In the first case the trapped electron can be emitted back into the conduction band, which is characterized by an electron emission $e_n$ as shown in Figure 4.6. The other possibility is that a hole can be captured from the valence band with a capture coefficient of $c_p$. The end result for both cases is an impurity site that is occupied by a hole. Similarly, this hole can go into the valence band with emission coefficient $e_p$ or it can capture an electron from the conduction band. The last process where the hole is sent back to the valence band is in general sense perceived as electron emission from the valence band to the impurity level and is shown by the dashed arrow. These are the four possible processes that exist between the impurity level and the conduction and valence bands.

The recombination event is defined as an event where an electron is captured by an impurity level followed by hole capture from the valence band. Subsequently the generation event happens when an electron is emitted to the conduction band followed by a hole emission to the valence band. There is also a third kind of event which is commonly called the trapping process. This event happens when an electron is captured by the impurity level followed by emission to the conduction band or a hole capture from the valence band and then followed by hole emission to the valence band. In these events the carrier is captured and then subsequently sent back to where it came from. This means that one band (either conduction or valence) takes part in the trapping process along with the trap level.
Whether the impurity will behave as a trap or a generation-recombination center is determined by the position of the Fermi level in the band gap and the energy level of the traps themselves. The other parameters that can define whether an impurity level behaves as a trap or a generation-recombination center are temperature and impurity capture cross section. Typically, the impurities that are near the middle of the band gap act as generation-recombination centers and the ones that are close to the band edges behave as trapping centers. Again it should be noted that the electron emission rate is not always equal to the hole emission rate. The impurity centers which are present in the upper section of the band gap has higher electron emission probability and the centers which are at the bottom half have higher hole emission probability.

We now derive the expressions for the generation and recombination mechanisms by considering carrier interactions with localized states within the band gap. In Figure 4.7 we indicate the four processes defined earlier. There are $N_t$ states with energy $E_t$ within the band gap. $r_1$ is the electron
capture rate, \( r_2 \) is the electron emission rate, \( r_3 \) is the hole capture rate, and \( r_4 \) is the hole emission rate.

Next we define an electron capture event when an electron in the conduction band is captured by an empty localized state. The volume sweep rate is given as

\[
c_n = \sigma_n \cdot v_{th} \quad \ldots (1)
\]

Here \( \sigma_n \) is the electron capture cross section and \( v_{th} \) is the electron thermal velocity. \( \sigma_n \) depends upon the charge state of the generation-recombination center, i.e. whether the charge state is being positive, negative, or neutral. A negative charge on the center would repel the electron to provide smaller capture cross section. A positively charged state when it is empty \( e \), on the other hand, would attract the electron with a large capture cross section. The rate at which electron capture happens depends on the number density of electrons which are in the conduction band, the number density of localized states which are empty, and \( c_n \). We can write

\[
r_1 = n\{N_t[1 - f(E_t)]\}\sigma_n v_{th} \quad \ldots (2)
\]

Here \( n \) is the number density of electrons in the conduction band, \( N_t \) is the density of empty localized states, and \( f(E_t) \) is the probability of occupation of the localized states.

The electron emission process, on the other hand, is emission of electron from the localized state to the conduction band. This rate is given as

\[
r_2 = N_t f(E_t) e_n \quad \ldots (3)
\]

Here \( N_t f(E_t) \) is the density of localized states filled with electrons and \( e_n \) is the probability that electron will make a transition from the localized state to the conduction band. Now the rate of
emission is equal to the rate of capture at thermal equilibrium where $f(E_t)$ is equivalent to $f_D(E)$.

This gives us for $r_1 = r_2$

$$n\{N_t[1 - f_D(E_t)]\} \sigma_n v_{th} = N_t f_D(E_t) e_n \quad \cdots (4)$$

Solving for $e_n$ we get,

$$e_n = v_{th} \sigma_n n_t \exp \left( \frac{E_t - E_i}{kT} \right) \quad \cdots (5)$$

From the above equation we understand that if $E_i$ is near the conduction, the exponential term is large and the emission of electrons from the localized state has high probability.

The third event is the hole capture where hole is captured by a localized state filled with electron. This rate is given as

$$r_3 = N_t f(E_t) p v_{th} \sigma_p \quad \cdots (6)$$

Here the capture cross section of hole is $\sigma_p$ and $p$ is the number density of holes. Finally, the hole emission event happens when an electron from the valence band makes a jump to an empty localized state with an emission probability $e_p$. This rate process is written as

$$r_4 = N_t [1 - f(E_t)] e_p \quad \cdots (7)$$

At thermal equilibrium $r_3 = r_4$ and we get

$$e_p = v_{th} \sigma_p n_t \exp \left( \frac{E_i - E_t}{kT} \right) \quad \cdots (8)$$

This implies that the emission probability is higher for a hole making a jump from the localized state which is closer to the valence band edge. Next we describe the behavior of the localized state
when it acts as a recombination center. This is true when the localized state is near the middle of
the band gap.

The net steady state recombination rate $U$ can be written as

$$U = R - G = r_1 - r_2 = r_3 - r_4 \quad \ldots (9)$$

Solving for $U$ and putting expressions for all the rates we get

$$U = \frac{N_t \nu th \sigma_n \sigma_p (pn - n_i^2)}{\sigma_p [p + n_i \exp \left( \frac{E_i - E_L}{kT} \right)] + \sigma_n [n + n_i \exp \left( \frac{E_t - E_i}{kT} \right)]} \quad \ldots (10)$$

Or

$$U = \frac{(pn - n_i^2)}{\tau_{no} [p + n_i \exp \left( \frac{E_i - E_L}{kT} \right)] + \tau_{po} [n + n_i \exp \left( \frac{E_t - E_i}{kT} \right)]} \quad \ldots (11)$$
Here $\tau_{no} = (N_t v_{th} \sigma_n)^{-1}$ and $\tau_{po} = (N_t v_{th} \sigma_p)^{-1}$. For net recombination $U > 0$ and $pn > n_i^2$ and for net generation $U < 0$ with $pn < n_i^2$. For the case where $\sigma_n = \sigma_p$ we get

$$U = \frac{pn-n_i^2}{(p+n+2n_icosh(E_t-E_i/kT))\tau_o} \quad \cdots (12)$$

From the above equation we see that $U$ is symmetric around $E_i=E_i$ where maximum value is achieved. The normalized equation $U/U(E_i=E_i)$ is plotted in Figure 4.8 where $U(E_i=E_i)=U_o$. $U_o$ is the maximum value of $U$ which occurs near the middle of the semiconductor band gap.

We will now discuss surface states which also act as sites for generation and recombination processes. Kinetically the surface states have similar G-R mechanism as that of bulk. The only difference exists in the number density interpretation. For bulk we considered volume density but for surface G-R we use area density $N_{st}$ (cm$^{-2}$). Typically, the surface centers exist over a few atomic layers which for analysis can be taken as an equivalent number of states present on the surface. The surface recombination rate can be written as

$$U_s = \frac{N_{st} v_{th} \sigma_n \sigma_p (ps_n-s-n_i^2)}{\sigma_p [ps+n_iexp(E_t-E_{st}/kT)]+\sigma_n [n_s+n_iexp(E_{st}-E_i/kT)]} \quad \cdots (13)$$

Here subscript $s$ refers to the parameters used for surface G-R. We can rewrite Equation 12 as

$$U_s = N_{st} v_{th} \sigma_p \frac{ps_n-s-n_i^2}{[ps+n_s+2n_i cosh(E_{st}-E_i/kT)]} \quad \cdots (14)$$

In a $p$-type semiconductor if we assume that $p-n$ is constant throughout the space charge region then we can write
\[ p_s n_s = p_p(x_d)n_p(x_d) = N_A n_p(x_d) \quad \ldots (15) \]

This makes

\[ U_s = N_{st} v_{th} \sigma \frac{N_A[n_p(x_d) - n_{po}]}{[p_s + n_s + 2n_i]} = N_{st} v_{th} \sigma \frac{N_A n'_p(x_d)}{[p_s + n_s + 2n_i]} \quad \ldots (16) \]

From **Equation 16** the coefficient of \( n'_p(x_d) \) is called as \( s \)

\[ s = N_{st} v_{th} \sigma \frac{N_A}{[p_s + n_s + 2n_i]} \quad \ldots (16) \]

The parameter \( s \) has dimension as \( cm/s \) and also called as the surface recombination velocity.
References


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Chapter 5

SUMMARY AND FUTURE DIRECTIONS

The aim of this work is to understand how ‘beyond CMOS’ materials and devices can be used to replace Si based CMOS technology. We used angle dependent transport property of graphene to demonstrate enhanced OFF state resistance in graphene p-n junction, without opening a band gap. To achieve that we first studied a tilted p-n junction in h-BN/graphene/h-BN sandwich structure to attain 2x increase in OFF state resistance. Subsequently we introduced a new device design concept which can efficiently block the low angle transverse modes to further increase the OFF state resistance by 20x. For future work we would scale down the tab width to make it a near ideal point source of electrons. The device size also needs to be reduced to have mean free path comparable to the length of the device. Finally, we can examine other the cut designs to efficiently block the low angle traversing modes to achieve even higher OFF state resistance.

In the second part of this work we demonstrate a two-dimensional WSe$_2$ based bipolar junction transistor. For doping we use buried electrostatic gating techniques. The highest current gain achieved in our device is $\sim 1000$. We further extend the BJT architecture to demonstrate a phototransistor with a photocurrent gain of $\sim 40$. The gain in our devices can be further increased by creating ideal diodes ($n=1$) and this would be the motivation of future work.

Finally, we introduce a single device that can be reconfigured to perform operations of three fundamental modern electronic devices i.e. p-n junction, field effect transistor and bipolar junction transistor. This multi-gated device is expected to minimize processing complexity, and its
reconfigurability mechanism will require less number of devices for performing complex computations. We used the interface density of states as the only parameter to link the properties of the three fundamental devices. For future work, it will be interesting to understand the potential of this device by implementing it into circuits to perform logic operations. Moreover, to minimize the series resistance, graphene can be used at the contact material which can be doped to lower the Schottky tunnel barrier.
Appendix A

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