High frequency signal transmission in through silicon via based 3D integrated circuit

Min Xu

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HIGH FREQUENCY SIGNAL TRANSMISSION
IN THROUGH SILICON VIA BASED
3D INTEGRATED CIRCUIT

by

Min Xu

A Dissertation
Submitted to the University at Albany, State University of New York
in Partial Fulfillment of
the Requirements for the Degree of
Doctor of Philosophy

College of Nanoscale Science and Engineering
2015
HIGH FREQUENCY SIGNAL TRANSMISSION
IN THROUGH SILICON VIA BASED
3D INTEGRATED CIRCUIT

by

Min Xu

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“There is only one thing that makes a dream impossible to achieve: The fear of failure.”

- Paulo Coelho, The Alchemist

Dedicated

To

My parents

Yangwen Xu & Zhihua Guan

And

My husband

Xiaolong Zheng
ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisor, Prof. Robert E. Geer, for his continuing guidance, support and encouragement during my Ph.D. journey. He cultivated in me the ability of critical thinking, analyzing and presenting. His patience and motivations has helped me many times and strived me to the best. My research experiences with him have brought about immerse positive transformation in my scientific and technical capabilities. I will always be grateful for the lessons, advices and humor he shared with me along the way.

I would like to thank Prof. Michael Liehr, Prof. Douglas Coolbaugh, Prof. James Castracane, and Dr. Pavel Kabos (NIST) for providing helpful suggestions, reviews and serving as my dissertation committee. I am grateful to Prof. Michael Liehr, Prof. Nate Cady and Prof. Ji Ung Lee for letting me use the electrical characterization tools in their labs. I thank Sematech 3D group and CNSE CSR 3Di group for fabricating the 3D test structures used in this dissertation. My great appreciations would go to Dr. Harika Manem for her helpful advices, encouragement and sharing in my research and life. I am also thankful to my group members Robert Carroll, Dr. Steve Adamshick, for their help and contributions to my dissertation. Thanks to Dr. Thomas Murray and Dr. Jiajun Mao for their help with FIB and SEM characterizations, to Dr. Wei Wang, Dr. Tong Jing, Dr. Sansiri Tanachutiwat, Dr. Argyrios Malapanis along with all faculty and students I have interacted with at CNSE during my study and research.

I would also like to thank Dr. Pavel Kabos and Dr. Thomas Mitchell Wallis for their help and fruitful discussions during my two trips to NIST for RF characterizations and simulations. They made my lab trips so fruitful and also, introduced me to the beautiful Boulder. And I also want to thank my intern manager Jim and all colleagues at Broadcom CCX team during my internship. I have learned a lot from everyone there and enjoyed working with you guys so much. The half-year internship brought me so much more than I expected. I am looking forward to going back soon.

My gratitude also goes to my friends for being there and caring for me as always. Thanks to my brother for having always supported me. The last and toughest part of this journey, the dissertation phase,
would have been impossible without the motivation and encouragement from Xiaolong, my loving husband. Thank you for your love and support.

Last but most importantly, I thank my parents for their endless love and care. This dissertation is dedicated to you. Especially to my father, thank you so much for being such a great dad and friend. I miss you so much and wish you could see this moment. I will be brave as you taught me to and I know you are still there for me as always. My heart is always being with you, ever and forever.
# TABLE OF CONTENTS

ACKNOWLEDGEMENTS ........................................................................................................... iv

LIST OF FIGURES ..................................................................................................................... x

LIST OF TABLES ......................................................................................................................... xvi

LIST OF ABBREVIATIONS .......................................................................................................... xvii

ABSTRACT ................................................................................................................................. xx

CHAPTER 1 Introduction and Research Motivation ................................................................. 1
  1.1 3D integration and TSV technology .................................................................................. 1
  1.2 Introduction to heterogeneous 3D integration ................................................................. 3
  1.3 Introduction to high speed signal transmission in a 3D system ....................................... 4
  1.4 Dissertation motivation and organization ....................................................................... 10

References .................................................................................................................................. 13

CHAPTER 2 TSV and 3DIC fabrication ..................................................................................... 17
  2.1 TSV based 3DIC integration process ............................................................................... 17
  2.2 TSV fabrication process ................................................................................................... 19
    2.2.1 Via etching .................................................................................................................. 19
    2.2.2 Via insulation .............................................................................................................. 20
    2.2.3 Via filling and front side metallization ...................................................................... 21
    2.2.4 Via reveal and back side metallization ...................................................................... 22
  2.3 3D stacking and bonding techniques .............................................................................. 23
    2.3.1 Wafer alignment ........................................................................................................ 24
    2.3.2 Wafer bonding .......................................................................................................... 25

References .................................................................................................................................. 28

CHAPTER 3 Characterization and Simulation Fundamentals .................................................. 30
  3.1 Scattering parameters ....................................................................................................... 31
CHAPTER 5 High Frequency Signal Transmission in a Multi-layer Stacked 3D System ................................................................. 88

5.1 Introduction .................................................................................. 88

5.2 Test structures in a multi-layer stacked system .................................. 89

5.2.1 Layout and schematics ............................................................. 89

5.2.2 SEM images ............................................................................ 91

5.3 Experimental characterization for 3D channels in a multi-layer stacked system ........ 92

5.3.1 Test reproducibility ................................................................. 93

5.3.2 Substrate conductivity’s impact ............................................... 94

5.3.3 Stacking impact ...................................................................... 95

5.3.4 In-plane RDL’s impact .......................................................... 97

5.3.5 Bonding pad impact ............................................................. 98

5.4 Equivalent element model simulation for 3D channels in multi-layer stacked system 99

5.4.1 Test structures with channel model representation .................. 99

5.4.2 Model optimization with least square error function ............... 101

5.4.3 Systematic model validation with various test structures .......... 104

5.5 Analyses of electrical characteristics of a high speed 3D channel ......... 106

5.5.1 TSV design ........................................................................... 107

5.5.2 RDL design ........................................................................... 113

5.5.3 Bond pad design ................................................................. 116

5.5.4 Summary of 3D channel design .......................................... 117

References ........................................................................................ 120

CHAPTER 6 High Speed Signaling in a Stacked 3D System: Circuit Perspective .122

6.1 Introduction .................................................................................. 122

6.2 Transmitter and Receiver circuitry .................................................. 123

6.2.1 Single ended signal transmitter and receiver ............................ 123

6.2.2 Differential signal full swing transmitter ................................ 124

6.2.3 Differential signal reduced swing transmitter ....................... 125

6.2.4 Differential signal receiver .................................................... 126
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.3</td>
<td>Reduced circuit models for 3D channels</td>
<td>128</td>
</tr>
<tr>
<td>6.4</td>
<td>Circuit simulation results</td>
<td>131</td>
</tr>
<tr>
<td>6.4.1</td>
<td>Eye diagram results</td>
<td>131</td>
</tr>
<tr>
<td>6.4.2</td>
<td>Timing parameters</td>
<td>133</td>
</tr>
<tr>
<td>6.4.3</td>
<td>Power consumption</td>
<td>134</td>
</tr>
<tr>
<td>6.5</td>
<td>Conclusions</td>
<td>135</td>
</tr>
<tr>
<td>References</td>
<td></td>
<td>136</td>
</tr>
<tr>
<td>CHAPTER 7</td>
<td>Conclusions and Future Directions</td>
<td>138</td>
</tr>
<tr>
<td>7.1</td>
<td>Conclusions</td>
<td>138</td>
</tr>
<tr>
<td>7.2</td>
<td>Future directions</td>
<td>140</td>
</tr>
<tr>
<td>APPENDIX A</td>
<td>Fabrication Process Flow for Multi-layer Stack 3D IC</td>
<td>141</td>
</tr>
<tr>
<td>APPENDIX B</td>
<td>Layout for passive 3-tier stack test vehicle</td>
<td>144</td>
</tr>
<tr>
<td>APPENDIX C</td>
<td>Layout for circuits’ perspective high-speed signaling test vehicle</td>
<td>145</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

Figure 1.1 Application Development for 3D integrated Products[12] ................................................................. 2
Figure 1.2 Schematics of future 3D heterogeneous integration of InfoTech, NanoTech and BioTech systems – a new paradigm for future technologies[9] ................................................................. 4
Figure 1.3 Conventional 2D IC migration towards 3D heterogeneous IC driven by shorter electrical connections[10] .................................................................................................................. 5
Figure 1.4 an example of high speed digital signal relation to high frequency signal components[21]...... 7
Figure 1.5 Typical high frequency transmission lines in 2D system[23] ................................................................. 9
Figure 1.6 Summary of performance predictions of various high-speed 3D links................................. 11
Figure 2.1 3D TSV integration methodologies [5].............................................................................................. 18
Figure 2.2 SEM image of the undulating sidewall of a silicon structure fabricated using photolithography and deep reactive-ion etching (Bosch process) [9] .............................................................. 20
Figure 2.3 Cross sectional SEM image of a fabricated TSV dual chain test structure ......................... 24
Figure 2.4 cross sectional SEM image of bonded wafer showing tolerable bonding misalignment...... 25
Figure 2.5 Cross sectional SEM image of a Cu-Cu bond between stacked wafers................................. 26
Figure 2.6 Tilted angle SEM image of 3 tier stack wafer by direct Cu-Cu bonding[7]............................. 27
Figure 3.1 EM wave propagation in: (a) a typical Ground/signal twin pair wire; (b) an example of test structure in this study- a 3D channel with 1S2G TSV array. ................................................................. 30
Figure 3.2 a 2 port network represented by S-parameters for electrical characteristics ......................... 32
Table 3.1 Typical values for dB and notes for results presented in this dissertation ................................. 34
Figure 3.3 Insertion loss S21 and return loss S11 data for a low loss transmission line ............................ 35
Figure 3.4 An HFSS model example for isolated 1S2G TSV simulation. The circles on top and bottom of center signal TSV are assigned as excitation wave ports ....................................................... 37
Figure 3.5 The representation of detailed field quantities at each tetrahedron during numerical calculation[12] .................................................................................................................................. 38
Figure 3.6 Schematic of a signal ground TSV pair with landing pad for vertical to horizontal connection and their geometrical parameters ........................................................................... 41
Figure 3.7 Equivalent circuit model for signal/ground TSV pair ................................................................. 42
Figure 3.8 Equivalent circuit model for a signal/ground RDL connecting to TSVs ......................................... 45
Figure 3.9 Equivalent circuit model for Cu-Cu bonding pad that including capacitance from both pad and via connecting pad to the last metal layer ................................................................. 46
Figure 3.10 Diagram of a typical VNA/[21] ............................................................. 48
Figure 3.11 Characterization setup with Agilent VNA and Cascade Semi auto RF probe station in (a); Zoomed picture of probing on DUT in (b) ................................................................. 49
Figure 3.12 Full two port, 12 term error model used for TRL calibration[24] .............................................. 50
Figure 3.13 Optical microscopic image of test structures. On wafer TRL calibration structures are located on the left and right columns. ................................................................. 51
Figure 3.14 Equivalent models of the test structures for Open/Short de-embedding technique .......... 53
Figure 4.1 Test structure schematics in a 2-tier system. (a) is the cross-section view of dual chain test structure; (b) is the perspective view of TSV dual chain test structure (using 1S2G as an example); (c) is zoomed 1SXG TSV structures ........................................................................................................ 58
Figure 4.2 SEM image for top view of TSV dual chain test structure ........................................................... 59
Figure 4.3 FIB cross-section SEM image of TSV dual chain test structure .................................................. 59
Figure 4.4 IV measurement results for 60 via chains for electrical continuity confirmation .................... 60
Figure 4.5 Test reproducibility validation with 1S2G TSV array dual chain structure on different dies over the wafer ....................................................................................................... 61
Figure 4.6 Statistical averaged S-parameters for 1SXG TSV array dual chain structures comparison ...... 62
Figure 4.7 Isolated TSV full wave simulation results predicted by Yu et al: 1S4G TSV array has lower signal insertion loss and return loss compared to 1S2G TSV array. [20] .................................................. 63
Figure 4.8 HFSS simulation model for TSV+CPW 3D test structure ............................................................ 65
Figure 4.9 Electric field distribution on CPW wave port at the GSG probe pad ........................................... 65
Figure 4.10 Circuit model simulation diagram based on lumped circuit models in chapter 3.2 .............. 66
Figure 4.11 Comparison between measurement and simulation with full wave and circuit model for 1S2G TSV dual chain signal transmission and reflection S-parameter characteristics .................... 67
Figure 4.12 Results show good agreement between full wave simulation and measurement results for 1SXG TSV dual chains’ S-parameters ........................................................................... 68
Figure 4.13 Reproduce Yu’s simulation results: (a) is transmission insertion loss $S_{21}$ (b) is the simulation models for 1S2G and 1S4G.

Figure 4.14 Port size impact on S-parameter results for signals from DC to 10GHz

Figure 4.15 Port size impact on $S_{21}$ at 10GHz

Figure 4.16 Calculation for $S_{21}$’s sensitivity to port size

Figure 4.17 Isolated TSV simulation results for 1SXG TSV structures in this study that are consistent with Yu’s prior prediction

Figure 4.18 Electric field contour plots for 1SXG TSV configurations at middle point of TSV. The circles on plot 1S6G TSV configuration are representing the integration surface for EM power calculation.

Figure 4.19 HFSS post simulation field calculator panel

Figure 4.20 Calculated transmitted EM power around signal TSV for various 1SXG TSV configurations

Figure 4.21 Power flow calculation with vertical location for 1S2G TSV on different resistive substrate.

Figure 4.22 Time domain impedance for 1SXG TSV array configuration indicates adding ground TSVs reduces the impedance so as increases impedance mismatch to reference impedance.

Figure 4.23 Equivalent capacitance models for 1SXG TSV array configurations

Figure 4.24 Generated finite element meshes for capacitance calculation in COMSOL

Figure 4.25 1SXG TSV array models used to calculate capacitance in COMSOL

Figure 4.26 Comparison of simulated capacitance of 1SXG TSV array configurations

Figure 5.1 Cross-sectional schematic for various TSV chain test structures in 2-tier and 3-tier stacked wafer to investigate impacting factors for signal transmission property in a multi-layer stacked system

Figure 5.2 Tilted angle SEM image for 3-tier stacked wafer system

Figure 5.3 Cross-section SEM image of a 3-tier V chain that shows good die to die and die to wafer alignment and connections between layers.

Figure 5.4 Test reproducibility validation on the same test structure on different dies over the stacked wafer

Figure 5.5 S-parameter characterization results for 2-tier U chain test structure fabricated on different resistive substrates
Figure 5.6 S-parameter characterization results for U chain structure in 2-tier and 3-tier stacked system that represent stacking impact on signal transmission property ................................................................. 96

Figure 5.7 S-parameter characterization results for 2-tier W chain and 3-tier V chain that represent stacking impact on signal transmission property ............................................................................ 96

Figure 5.8 S-parameter characterization results for 2-tier and 3-tier U chain test structures with different bottom RDL lengths for in-plane connection ........................................................................ 97

Figure 5.9 S-parameter characterization results for 3-tier V chain test structures with different middle tier RDL lengths for in-plane connection ........................................................................ 98

Figure 5.10 S-parameters characterization results for 3-tier U chain test structures with various bond pad sizes ............................................................................................................................ 99

Figure 5.11 3D component model representations for various TSV chain test structures in multi-layer stacked system .............................................................................................................. 100

Figure 5.12 Equivalent circuit models for TSV and RDL component .................................................................................................................. 101

Table 5.1 Least square error function optimized model parameters .................................................................................................................. 103

Figure 5.13 S21 Magnitude and phase of measured and simulated results for 2-tier and 3-tier U chain with 32µm bottom RDL connection ..................................................................................... 104

Figure 5.14 S21 Magnitude and phase comparison between measurement and model simulation results for 2-tier long U chain with 64µm RDL connection and 2-tier W chain test structures to validate 3D component models .................................................................................. 105

Figure 5.15 Magnitude and phase of transmission coefficient comparison between measurement and model simulation results for 3-tier long U chain with 64µm RDL bottom connection and 3-tier V chain test structures to validate 3D component models .................................................................................. 106

Figure 5.16 Channel’s signal transmission S21 with variation with TSV’s insulation layer oxide capacitance ........................................................................................................................... 108

Figure 5.17 Channel’s signal transmission S21 with variation with TSV’s coupling capacitance ........................................................................................................................... 109

Figure 5.18 Channel’s signal transmission S21 with variation with TSV’s inductance .................................................................................. 110

Figure 5.19 Channel’s signal transmission S21 with variation of silicon substrate conductance between G/S TSVs ........................................................................................................................... 111

Figure 5.20 Channel’s signal transmission S21 with variation with TSV’s resistance .................................................................................. 112

Figure 5.21 Channel’s signal transmission S21 with variation with landing pad capacitance .................................................................................. 113
Figure C.1 Superimposed layouts of all 3 tiers of the MPW, with Circuit perspective high-speed signaling test vehicle at the bottom section.................................................................................................................................................. 145

Figure C.2 Different transmitter and receiver circuits multiplexed to the IO................................................................. 146
LIST OF TABLES

Table 3.1 Typical values for dB and notes for results presented in this dissertation .................................. 34

Table 5.1 Least square error function optimized model parameters .......................................................... 103

Table 6.1 Layout information for reduced swing differential transmitter ................................................. 126

Table 6.2 Layout information for differential receiver circuit ................................................................. 127
# LIST OF ABBREVIATIONS

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV</td>
<td>Through silicon via</td>
</tr>
<tr>
<td>3D ICs</td>
<td>3-dimensional integrated circuits</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>1SXG TSV</td>
<td>One signal with multiple ground TSVs</td>
</tr>
<tr>
<td>1S2/4/6G TSV</td>
<td>One signal with 2/4/6 ground TSVs</td>
</tr>
<tr>
<td>G/S TSV</td>
<td>Signal TSV with one ground TSV</td>
</tr>
<tr>
<td>1S TSV</td>
<td>Single signal TSV</td>
</tr>
<tr>
<td>RDL</td>
<td>Redistribution layer interconnects</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>CIS</td>
<td>CMOS image sensor</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field programmable array</td>
</tr>
<tr>
<td>HMC</td>
<td>Hybrid memory cube</td>
</tr>
<tr>
<td>DDR</td>
<td>Dual Data Rate</td>
</tr>
<tr>
<td>SDRAM</td>
<td>Synchronized Dynamic Random Access Memory</td>
</tr>
<tr>
<td>HBM</td>
<td>High bandwidth memory</td>
</tr>
<tr>
<td>IoT</td>
<td>Internet of things</td>
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<tr>
<td>RF</td>
<td>Radio frequency</td>
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<td>Hz</td>
<td>Hertz</td>
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<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>Gbps</td>
<td>Giga bits per second</td>
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<tr>
<td>S-parameters</td>
<td>Scattering parameters</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector network analyzer</td>
</tr>
<tr>
<td>TEM</td>
<td>traverse electromagnetic</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>CPW</td>
<td>Coplanar waveguide</td>
</tr>
<tr>
<td>BEOL</td>
<td>Back-End-Of-Line</td>
</tr>
<tr>
<td>FEOL</td>
<td>Front End Of Line</td>
</tr>
<tr>
<td>DRIE</td>
<td>deep reactive ion etch</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical vapor deposition</td>
</tr>
<tr>
<td>TaN</td>
<td>tantalum nitride</td>
</tr>
<tr>
<td>ECD</td>
<td>Electrochemical deposition</td>
</tr>
<tr>
<td>CMP</td>
<td>chemical mechanical planarization</td>
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<tr>
<td>ILD</td>
<td>inter level dielectric</td>
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<tr>
<td>FIB</td>
<td>focused ion beam</td>
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<tr>
<td>KGD</td>
<td>known good die</td>
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<tr>
<td>ESD</td>
<td>Electrostatic discharge</td>
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<td>IR</td>
<td>infrared radiation</td>
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<td>SEM</td>
<td>Secondary electron microscopy</td>
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<td>I/O</td>
<td>input/output</td>
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<tr>
<td>Abbreviation</td>
<td>Definition</td>
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<tr>
<td>IL</td>
<td>insertion loss</td>
</tr>
<tr>
<td>RL</td>
<td>return loss</td>
</tr>
<tr>
<td>dB</td>
<td>decibel</td>
</tr>
<tr>
<td>DUT</td>
<td>device under test</td>
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<tr>
<td>FEM</td>
<td>finite element modeling</td>
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<tr>
<td>HFSS</td>
<td>High frequency structure simulator</td>
</tr>
<tr>
<td>RLCG</td>
<td>resistance, inductance, capacitance and conductance</td>
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<tr>
<td>ADS</td>
<td>Advanced design system</td>
</tr>
<tr>
<td>TRL</td>
<td>thru reflect line</td>
</tr>
<tr>
<td>SOLT</td>
<td>Short Open Load Thru</td>
</tr>
<tr>
<td>LRRM</td>
<td>Line Reflect Reflect Match</td>
</tr>
<tr>
<td>GSG</td>
<td>Ground signal ground</td>
</tr>
<tr>
<td>ISS</td>
<td>impedance standard substrate</td>
</tr>
<tr>
<td>Tx/Rx</td>
<td>Transmitter and receiver</td>
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ABSTRACT

Through silicon vias (TSVs) enable 3-dimensional (3D) integrated circuits (ICs), which have the potential to reduce the power consumption, interconnect length and overall communication latency in modern nanoelectronics systems. High-speed signal transmission channels through stacked silicon substrates are critical for 3D heterogeneous integration. This work presents systematic analyses of fabricated 3D IC test structures. This includes test structure design, fabrication, experimental characterization, equivalent circuit modeling and full wave simulations for high-speed signal transmission of the TSV based 3D IC channels.

In a 2-tier stack system, three distinct signal/ground TSV configurations (1SXG TSV) were investigated. Scattering parameter measurements showed low signal loss of the channels. Both full wave simulation and equivalent circuit models exhibited excellent agreement with measurement results. The systematic analyses indicates that proper interconnect design needs to be considered that takes into account the tradeoffs between ground TSV capacitance-induced impedance change and EM shielding effects. Fewer ground TSVs are preferred considering both 3D channel transmission efficiency and die area consumption for 3D ICs.

Test structures were also designed and fabricated to investigate high-speed signaling in a multi-layer stacked die system. Experimental characterization of the 3D systems was conducted to investigate the impacts of substrate conductivity, redistribution layer (RDL) interconnects, and multi-tier stacking on the high-speed signal transmission of 3D IC channels. Equivalent circuit models for key components (TSV, RDL, bond pad) in 3D IC channels were developed and validated by experimental results. Comprehensive analyses with validated circuit models provided critical insights and guidance to key component design for a 3D channel in a stacked system.

For complete 3D IC channels with active transmitters and receivers, simulation-based analyses were performed for high-speed single-ended and differential signaling schemes. Signal integrity, timing
parameter and power consumption analyses were performed with various transceivers and channel configurations.

This work provides comprehensive analyses for high-speed transmission considerations ranging from the component to circuit level perspectives. Such an analysis will prove invaluable for future designers and aid in the design of heterogeneous 3D IC systems.
CHAPTER 1 Introduction and Research Motivation

1.1 3D integration and TSV technology

In recent decades, the semiconductor industry has been driven by Moore’s law to scale down the transistor size thereby increase the transistor density in integrated circuits to enhance the performance of electronic products and reduce their cost. The well known Moore’s law was an observation from the co-founder of the Intel Corporation, Gordon Moore, in 1965, that the number of transistors in an integrated circuit doubles approximately every two years [1]. For the last half century, the semiconductor industry has followed the prediction very well and this observed ‘Moore’s law’ had become the driving force for the semiconductor industry’s research and development. The exponential growth of many related integrated circuit performance parameters dramatically enhanced the impact of digital electronics benefitting technology, industry productivity, people’s social lives and economic growth around the world.

Currently, transistor sizes have scaled down to below 20nm[2]. As the transistor dimension approaches atomic size and faces physical limitations beyond 10nm, scaling with Moore’s law has slowed down[3][4]. But, as a result of this process scaling, the interconnect resistance and capacitance has increased, leading to increased latency and power consumption. The trend in the semiconductor industry is therefore transforming from a device focused era to an interconnect or ‘communication’ focused era[5]. In order to extend Moore’s law to keep improving electronics performance, researchers and engineers have started exploring the so-called third dimension beyond the traditional two-dimensional integrated circuit (2D IC) to accommodate increasing connectivity demands[6]. This approach, typically referred to as ‘3D integration’, allows for vertically stacking and interconnection of multiple chips to form highly integrated micro-nano systems. Instead of traveling across a 2D chip, the signal travels vertically through the vertical interconnects which are bonding pads, solder balls, and through silicon vias (TSVs) etc. For example, transforming a single planar platform to a 4 chip 3D stack has been predicted to reduce length of
the longest wires by 50%, with corresponding improvement of 75% in propagation delay and 50% in power dissipation[7], [8]. The small form factor and high device density possible with 3D integration can contribute to cost advantages and overall miniaturization that meet industry and market demands[9]. Therefore, 3D integration is currently seen as a leading candidate to extend Moore’s law and is a driving force in future semiconductor industry development.

There are many approaches being investigated and applied to 3D integration such as wire bonding chip to package, flip chip with micro bumps, stacked multi chip with wire bonding, package on package with solder balls, 3D IC with TSVs etc.[8], [10]. In recent years, 3D ICs with TSV technology has been attracting more and more attention because it is believed to be the best and densest approach to realize 3D integration[11]. Currently, 3DIC/packaging with TSV technology has already undergone development and demonstrations in applications including CMOS Image Sensors (CIS), memory, Field Programmable Gate Arrays (FPGA) etc. that has shown its feasibility in terms of manufacturing. Figure 1.1 illustrates a representative road map and market trends for applications with 3D integration technology[12].

![Figure 1.1 Application Development for 3D integrated Products][12]

Limited in part by manufacturing constraints, large scale TSVs with ~ 50 µm diameter were first applied in CMOS image sensor (CIS) application starting in 2005[13]. In recent years, due to the memory...
bandwidth limit, a consortium backed by several major technology companies including Samsung, Micron Technology, ARM etc., proposed stacked memory in a 3D system called Hybrid Memory Cube (HMC) that promised a 15× speed improvement compared to the third generation Dual Data Rate Synchronized Dynamic Random Access Memory (DDR3 SDRAM)[14]. HMC combined TSV and micro bumps to connect multiple dies of memory cell arrays on top of each other. In addition, high bandwidth memory (HBM), another form of high performance memory proposed as an industry standard by AMD and Hynix, targeted high performance graphics accelerators and network devices [15]. Xilinx also announced the world first 3D Field Programmable Gate Array (FPGA) using 28nm node technology featuring up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers[16]. While realization of 3D integration with TSV technology on homogeneous memories and FPGA stacks ensures its feasibility and manufacturability, the ultimate goal is the heterogeneous 3D integration for ultra-compact system integration of different technologies into a single 3D stack [17].

1.2 Introduction to heterogeneous 3D integration

Beyond the relatively straightforward ‘memory-on-logic’ or ‘logic-on-logic’ 3D integration, heterogeneous integration refers to densely interconnected stacking of dies of various functionalities in a compact 3D system. This approach is being driven by industry and consumer product upgrades in nearly every device and electrical product wherein an increased number of functionalities and faster data transmission is required, as well as a shrinking of the size of the electronic product. Figure 1.2 shows the schematics of possible future 3D heterogeneous integration schemes to integrate diverse emerging technologies into a chip sized 3D stack[9]. Functional chips such as bio/chemical sensors, image sensors, MEMS, analog ICs, memories and digital processors etc. can be vertically stacked and connected in a heterogeneous 3D system.
The applications of 3D heterogeneous systems cover many diverse fields such as ambient assisted living, smart buildings, safety and security, smart medical systems, mobile and defense applications, etc. The hardware in these systems integrates sensors with ICs and passive components, energy harvesters, and batteries into a single tiny package. Heterogeneous 3D integration is expected to become increasingly important for the high growth market areas of distributed wireless sensor systems, which will likely constitute the key connected hardware infrastructure of the upcoming Internet of Things (IoT) era [18].

1.3 Introduction to high speed signal transmission in a 3D system

In a traditional 2D heterogeneous system, transmission lines on chip or on a circuit board are used to support high speed digital and analog/RF signal transmissions between the processors, memories and other functional components such as antennas, sensors etc. With the scaling of the chip and package into the 3D paradigm, those channels were shortened and transformed to the third dimension as the vertical
connections, as shown in Figure 1.3[10]. Migrating from a conventional 2D IC/package to a 3D IC/package, the communication channels for various signals between functional chips must be transformed from on chip or on board planar transmission lines to 3 dimensional channels including TSV, bond pad, and redistribution layer interconnects (RDLs) within silicon stacks. This transformation of the traditional interconnection-wiring paradigm is critical for the technical success and manufacturability for all 3D IC applications – especially for high-bandwidth/high-frequency communication. This latter topic is the focus of this dissertation study.

Figure 1.3 Conventional 2D IC migration towards 3D heterogeneous IC driven by shorter electrical connections[10]

Specifically, in this dissertation, high-frequency communication channels in a custom-designed and fabricated 3D interconnected IC system are extensively investigated to determine the dominant design and fabrication elements determining high-frequency signal transmission. The channel here refers to a physical transmission medium (2D and 3D transmission components) used to convey a data or information (carrier) signal from one or several transmitters to one or several receivers at different locations on different layers in the 3D stack. A channel has certain capacity for transmitting various types of information, often measured by its bandwidth in Hertz (Hz) or its data rate in bits per second (bps). For analog/RF applications, the communication channels are always characterized in the frequency domain to
investigate the channels’ transmission performance over a wide range of frequencies[19]. On the other hand, digital data and information is composed of binary digits or bits (0s and 1s). For low speed digital or electric systems, simple wires and cables are adequate connection schemes, but for high speed digital signals this is not the case[20]. Data rate is defined as the total number of bits transferred per unit of time. For example, Gbps denotes $10^9$ (Giga) bits per second. Faster bit rates are required for many data intensive applications to deliver quicker computation and higher quality signals such as high-resolution video streams, etc. Along with high data rates, fast edge rates at the rising and falling edge relative to the data rates are also a desired metric in high-speed digital transmission. Digital pulses are comprised of high-order harmonic frequencies that determine the shape of the pulse. A short pulse with steep edges has a signal spectrum with relatively high power levels at high frequencies. A high-speed digital signal cannot be considered only in the digital regime. These signals contain frequency components that are much faster than the data rate of the signals (which also must be taken into account when designing/fabricating on-chip or 3D interconnection schemes). For example, consider the decomposition of a square wave signal as shown in Figure 1.4[21]. The figure illustrates the fast rising and falling edges of a high-speed digital signal, which is composed of the fundamental wave plus a large number of higher-order harmonics. An ideal square wave with vanishing or ‘0’ rise and fall times requires an infinite number of higher-frequency harmonics. All those harmonic frequency signal components will suffer some level of signal attenuation and losses in actual fabricated communication channels. Hence, fully understanding the high-frequency domain performance of a given 3D interconnection scheme is essential for digital as well as RF signal applications.
Figure 1.4 an example of high speed digital signal relation to high frequency signal components[21]

In high speed digital systems, the so-called knee frequency is related to the frequency spectrum and required bandwidth of a channel[22] and characterizes the high-end frequency range over which the channel can support effective digital signal transmission. For example, the -3dB bandwidth is calculated by Equation 1.1.

\[ F_{knee} = \frac{k}{T_r} \]  

(1.1)

Where \( T_r \) is the time of transition from 10% to 90% of the rise time, and \( k \) is a constant of proportionality related to the pulse shape, in most cases, equal to 0.35 for an exponential rise. For example, if the rise time is 10ps, the knee frequency calculated from the formula is 35 GHz.

Therefore, for both analog/RF signal and high-speed digital signal, frequency domain analyses with scattering parameters (S parameters) are used to characterize signal transmission properties of 3D communication channels. The S parameters are a mathematical construct that quantifies how RF energy propagates through a network over the frequency range of interest[23]. A frequency domain analysis with S parameters on the channel is necessary and helpful for analog/RF systems, high-speed digital systems, as well as mixed signal systems. The detailed information and derivation of S-parameters to be used to characterize and analyze the fabricated 3D IC connectivity test structures for this dissertation will be
presented in Chapter 3. For decades, vector network analyzers (VNAs) have been used to directly measure S-parameters. In addition to frequency domain analysis, time domain analysis is also commonly used for high-speed signal transmission characterization and is often more straightforward by presenting the signal voltage change in the time domain. The eye diagram characterizations for signal integrity of high-speed channels with circuits’ perspectives that will be presented in Chapter 6 are based on time domain analyses.

For high frequency signal transmission in conventional 2D ICs and systems, the traditional cable and on-board/package transmission lines are used in different scenarios depending on system performance need and configuration. Figure 1.5 illustrates two examples of such cable transmission lines – a coaxial cable configuration and a twin Ground/Signal (G/S) lead cable configuration (upper two illustrations in Fig. 1.5). For both examples the EM field distributions are also shown in a cross section view[23]. Coaxial cables are widely used in long distance RF and millimeter wave signal transmission due to its complete EM field shielding and transmission of mainly traverse electromagnetic (TEM) wave mode. The bottom four schematics of Fig. 1.5 show typical planar transmission lines that are usually used on printed circuit boards for connecting different chips and functional modules like RF antennae, analog devices, processors, memories, etc. The planar type transmission lines include parallel plate, microstrip, stripline, and coplanar waveguides. Micro strip lines and coplanar waveguides can be used on the top layer of a circuit board while strip lines can be used in the middle layers of a multi-layer PCB. The electric field distribution of each type of transmission line is also shown in Fig. 1.5[23]. With the increasing data transfer speed demand of modern IC systems, high-speed serial links have succeeded the older parallel links to provide more efficient data transfer. Differential signaling is widely used in high-speed serial data transmission approach because it can support a very high digital data rate. Differential signaling is an approach for electrically transmitting information using two complementary signals (and will be discussed in more detail in this dissertation). It has many advantages such as ground offset tolerance, suitability for low voltage electronics and resistance to electromagnetic interference etc.
As noted earlier in this section, to realize high-speed signal transmission within 3D channels, respective 3D channel design and fabrication approaches need to be evaluated to support the communication demands for 3D homogeneous and heterogeneous ICs. Unlike the traditional planer transmission lines in layered metal/insulation structures in a 2D system, the 3D channels’ key components include vertical elements, most commonly surrounded by a uniform conducting silicon substrate. It is difficult to simply transform parallel plate, micro-strip line, and strip-line type transmission lines into 3D geometries. However, coaxial cable, G/S twin pair and coplanar waveguides can be migrated to a manufacturable 3D platform with various TSV configurations. Comparable to G/S twin pair, Ground/Signal TSV (G/S TSV) pair has been studied by a number of groups[24]–[26]. Besides, using the common plug-type TSV process, configuration of signal TSV surrounded by multiple ground TSVs (1SXG TSV) can be fabricated, which is comparable to coaxial cable. The dense ground TSVs around signal TSV act as ground shielding, comparable to coaxial cable’s ground shell. Yu et al. has investigated 1SXG TSV’s RF characteristics by full wave simulation[27]. In addition, coaxial type of TSV can be fabricated with sacrifice of higher cost.
by adding extra processing steps[28]. Those novel TSV based vertical high-speed channel components demand a systematic design and fabrication-based investigation to accelerate high-speed design for 3D integration. It leads to this dissertation’s motivation to evaluate 3D high-speed channels with various TSV configurations for high-frequency/high data-rate 3D communication.

### 1.4 Dissertation motivation and organization

A variety of TSV configurations for high-speed signal transmission have been proposed and studied by full wave simulation approaches and lumped circuit models by many groups[24]–[27], [29]. Related wave theories and electrical parameter simulation and analyses were also carried out by several researchers to understand the intrinsic wave propagation and electrical properties of TSVs[30]–[33]. A selected summary of the predicted performance metrics for various TSV configurations based on this literature is shown in Figure 1.6. Single signal TSV (‘1S’ TSV in the taxonomy used in this dissertation) is shown at the top of Fig. 1.6 and can transmit low speed digital signals but has limited bandwidth for high-speed signal transmission. However, a 1S TSV only consumes 1X TSV area on the silicon die which includes the TSV’s area as well as the required keep out zone which is dictated by manufacturing process needs. Simulation studies of a ‘one signal with two ground return’ TSV array (‘1S2G’ TSV) predicts an averaged bandwidth capability of 4-6Gbps, which is slightly higher than 1S TSV because the ground TSVs’ shielding effect as predicted by full wave simulation[27]. The chip area cost is 2 TSV unit areas considering ground return TSV shared by adjacent 1S2G arrays. Similarly with 1S4G TSV arrays (i.e. 4 ground TSVs per 1 signal TSV), the bandwidth has been predicted to be a little higher than the 1S2G array due to enhanced more shielding from the two additional ground TSVs. However, as a tradeoff, the 1S4G TSV array consumes more silicon area than 1S2G TSV array.

Beyond the ‘1SXG’ TSV approach, migrating from differential signaling in 2D high-speed links to differential signaling in 3D systems is also expected to yield higher bandwidths up to 40Gbps (4th row in Fig. 1.6). Because such vertical differential signaling only needs a single pair of TSVs per differential signal channel, it only consumes 2 TSV unit areas plus the differential transmitter and receiver circuits.
which are relatively small compared to micrometer scale for TSVs. Finally, the proposed coaxial cable TSV (5th row of Fig. 1.6) has been shown to exhibit extremely high signal bandwidth because of its full shielding that effectively reduces the signal loss into silicon substrate[28], [34]. The chip area consumption is around two TSV unit areas depending on the coaxial shield geometry and the keep out zone areas respectively. However, because of the unique configuration, it requires extra fabrication processes and increases the manufacturing complexity to realize the vertical shielding inside the silicon substrate. Except for special applications, due to the short length of the TSVs, most applications do not necessarily need the coaxial type of TSV in a typical 3D system considering the extra steps in processing and higher fabrication costs. Therefore, in this study, we only focus 3D connectivity designs and fabricated test vehicles incorporating TSV configurations with plug type TSV components using standard 3D integration processes.

<table>
<thead>
<tr>
<th>TSV Configuration</th>
<th>BW</th>
<th>TSV number</th>
<th>Chip Area</th>
<th>Schematics</th>
</tr>
</thead>
<tbody>
<tr>
<td>1S</td>
<td>1-3Gbps (Low)</td>
<td>1</td>
<td>1x (TSV)</td>
<td><img src="image1" alt="TSV Schematics" /></td>
</tr>
<tr>
<td>1S2G</td>
<td>4-6Gbps (Avg)</td>
<td>2</td>
<td>2X</td>
<td><img src="image2" alt="TSV Schematics" /></td>
</tr>
<tr>
<td>1S4G</td>
<td>4-8Gbps (Avg)</td>
<td>2-3</td>
<td>2-3X</td>
<td><img src="image3" alt="TSV Schematics" /></td>
</tr>
<tr>
<td>Differential TSV</td>
<td>10-40Gbps (High)</td>
<td>2</td>
<td>2X+ (TSV+ Circuits)</td>
<td><img src="image4" alt="TSV Schematics" /></td>
</tr>
<tr>
<td>Coaxial TSV</td>
<td>84Gbps (High)</td>
<td>2</td>
<td>2X</td>
<td><img src="image5" alt="TSV Schematics" /></td>
</tr>
</tbody>
</table>

Figure 1.6 Summary of performance predictions of various high-speed 3D links

In order to evaluate the literature performance predictions and investigate the high-speed signal transmission performance of various types of TSV-based, 3D connections for this dissertation, multiple 3D high-speed channel test structures were designed and fabricated. These included both single-stack, 2-
tier and 3-tier integrated 3D IC platforms. For each fabricated test structure a VNA was used to characterize the high-speed communication properties in the 3D connectivity structures of interest. Furthermore, each 3D channel design was modeled and simulations were undertaken to more thoroughly understand channel behavior for comparison with experimental measurement. For each 3D transmission channel design the complementary modeling/simulation results and experimental measurement dataset were combined to construct an overall design guidance for 3D high-speed interconnect design.

The remainder of the dissertation is organized as follows:

In Chapter 2, the key processes for the 3D test structure fabrication utilized for this dissertation are introduced and briefly described. The so-called ‘via middle’ 3D integration processing and Cu-Cu direct bonding techniques that were applied in the fabrication of the 3D stacked wafers are presented and reviewed.

In Chapter 3, details on the RF signal transmission and test fundamentals such as S-parameters, VNA characterization techniques, and simulation principles involved in this study are presented and discussed. Detailed equivalent lumped element modeling of high-frequency signal transmission in key 3D interconnection channel components is also presented as a reference for modeling results presented in later chapters.

In Chapter 4, the experimental characterization and comparison of S-parameter measurement results of fabricated 1SXG TSV array configurations in a single-stack system is provided. Full wave electromagnetic simulation and lumped element modeling are carried out and evaluated to quantitatively analyze the measured results and provide key insights for corresponding 3D interconnection channel design considerations.

In Chapter 5, investigation and performance evaluation of 3D high-speed interconnection channels are extended from the single stack system discussed in Chapter 4 to a true, multiple-tier stacked system. In an actual, fabricated 3D interconnection system, the 3D channels include not only TSVs, but also bonding
components and planar interconnections. The study presented in Chapter 5 analyzes multiple stacked 3D channels and investigates various sets of specifically designed, multi-tier TSV-based test structures to compare and study the impact of each component on the complete 3D channel. At the same time, the lumped element models (introduced in Chapter 3) were validated with multiple test structures to ensure their accuracy. With detailed analyses on validated electrical circuit models, critical design considerations for 3D channels in a multi-die 3D stack are presented and evaluated.

In Chapter 6, by adding active high-speed transmitters and receivers, the passive-only 3D channel study is extended to a complete 3D channel investigation with a circuits’ perspective. Both differential and single-ended signal transmission schemes were investigated based on circuit simulations. Signal integrity, timing and energy consumption were characterized using Cadence Spectre simulations to investigate the high speed signaling performance with single-ended and differential signaling in stacked 3D systems. These designs have been incorporated into a full, 3-tier, TSV-based 3D IC with active CMOS-based circuitry. This structure is currently undergoing fabrication and its test and evaluation will be the subject of future work.

Chapter 7 concludes the work and proposes future directions.

References


CHAPTER 2 TSV and 3DIC fabrication

2.1 TSV based 3DIC integration process

3D integration provides various potential benefits for higher system performance such as reduced delay, power consumption and increased data bandwidth. Among many 3D integration approaches such as wire bond, flip chip, TSV etc., TSV technology is the most efficient 3D integration methodology in terms of interconnection density. It continues to attract substantial research and development from universities, government and semiconductor industry towards commercialization[1]–[3]. Because TSVs are Back-End-Of-Line (BEOL) processed metal interconnects for vertical connection, they can be integrated into conventional CMOS integrated circuit fabrication processes in a variety of ways[4]. In a conventional TSV process a deep via (10-50 µm) is etched into the silicon substrate. Then an insulation liner is deposited to block current leakage between the via and the substrate. A barrier layer and a seeding layer for copper plating are then deposited, followed by via fill with conductive material (typically copper or tungsten). The excess metal is then polished using conventional BEOL chemical-mechanical planarization and another thick layer of dielectric is deposited as an insulation layer for planar metal lines. Depending on the nature of the TSV process flow, the wafer is, at some point, thinned from the backside until the ‘bottom’ of the TSVs are exposed at which point backside BEOL processing is carried out to enable the thinned silicon to be bonded to another silicon IC or handle wafer.

The overall process flow by which TSVs are processed and integrated into a mature, Si-based IC flow can vary substantially. Various process integration methods have been proposed. As shown in Figure 2.1, there are mainly four types of TSV integrations: via first, via middle, via last and via after bonding[5]. The first three types of integration incorporate TSV formation combined with planar IC fabrication process before the wafer bonding process, while the last ‘via after bonding’ utilizes TSV formation after the wafer bonding and thinning process. ‘Via first’, ‘Via middle’ and ‘Via last’ terms refer to the relative order between TSV formation and CMOS IC Front End Of Line (FEOL) active transistors process and
BEOL metal interconnects process. If the TSV is fabricated first before FEOL, it is referred to as a ‘Via first’ process. If the TSV is processed after FEOL but before BEOL, it is referred to as a ‘Via middle’ process. If the TSV is processed after BEOL completion, it is referred to as a ‘Via last’ process.

Figure 2.1 3D TSV integration methodologies [5]

The test vehicles in this dissertation study were based on three types of stacked wafer structures. The test vehicle discussed in Chapter 4 was fabricated with a single thinned TSV wafer stacked on a handle wafer. For horizontal connection metallization, front side and back side processing was carried out on the TSV thinned wafer while the stacked blank handle wafer acted only as mechanical support for the fragile thinned TSV wafer[6]. The TSV test structures studied in Chapter 5 were carried in a 3-tier 3D wafer stack (TSVs in two of the three tiers) bonded with Cu-Cu bonding process. In this structure the top two thinned tiers were fully processed with TSVs, underwent front-side and back-side metallization, and bonded to a bottom, conventionally processed silicon stack (with appropriate BEOL metallization to provide bonding and horizontal connections). To fabricate the complete high-speed channels that contain both active and passive components, a true 3D IC integration flow with TSV processes, FEOL and BEOL
CMOS processes and wafer bonding processes is being employed[7]. In this chapter, details for TSV fabrication process and stack bonding process will be presented in the following sections.

2.2 TSV fabrication process

For the studies carried out for this dissertation, all 3D and TSV test vehicles were fabricated with a ‘Via middle’ integration process through collaboration with Sematech and the CNSE Center for Semiconductor Research (CSR) 3D integration group. The CNSE 3D and CMOS process derivatives team have successfully developed a full 3D process for a 3D multi-tier stack wafer system. As mentioned earlier, after FEOL processing, deep TSV via holes are etched in the Si substrate, followed by deposition of an insulating liner, barrier layer, and seeding layering for via fill (Cu). Lastly the extra copper is polished away utilizing CMP. The TSV processing is followed by a conventional Cu-based BEOL process for front side metallization. Detailed processes are reviewed below.

2.2.1 Via etching

To enable through silicon electrical connection with TSV fabrication, via etching is the first step. After FEOL processing for active transistors’ patterning and fabrication, a photolithography process is used to define the TSVs. A conventional photoresist material is typically used, often in combination with a dielectric ‘hard mask’. The light source for lithographic processes for TSVs may incorporate g-line, i-line, KrF and ArF sources depending on the TSV dimension resolution requirements. For TSV’s with 5µm and 10 µm feature sizes in this study, an i-line photolithography tool with a 365nm wavelength light source was used. To form the TSVs with a hard mask pattern, there are several methods to remove the silicon substrate. These include wet etch, dry etch, laser drilling, reactive ion etch (RIE) and deep reactive ion etch (DRIE)[8]. DRIE is a highly anisotropic etching process to create deep penetration, steep-sided holes in the Si substrate. Due to its ability to create high aspect ratio vias, it is often used for TSV etching for 3D IC/package processing. For test structures in this study, we used the DRIE process (commonly referred to as the Bosch etching process) to create vias in the silicon substrate. The Bosch etching process
alternates repeatedly between two modes: standard isotropic plasma etching using SF₆ and deposition of a chemically inert passivation layer of C₄F₈ to protect the sidewalls[6]. Each step lasts for several seconds and the cycle time affects the overall etch rate and via sidewall profile. Shorter cycles yield smoother walls with a lower overall etch rate. Figure 2.2 presents the typical ‘scallop’ shape of TSV side walls due to this cyclic process[9]. The TSVs in our study had a target depth of 50µm, thus the etching depth is a slightly more than 50µm to leave sufficient space for backside reveal during wafer thinning process.

![Figure 2.2 SEM image of the undulating sidewall of a silicon structure fabricated using photolithography and deep reactive-ion etching (Bosch process)](image)

**2.2.2 Via insulation**

After TSV via etching, a dielectric liner layer is required to insulate the via-fill metal from the conducting silicon substrate. Several materials and process choices can be used such as chemical vapor deposited (CVD) SiO₂, polymer materials, wet deposit organic liner etc. The goal of the TSV insulator is to form a zero leakage, low stress layer at a reasonable process temperature and good step coverage and uniformity[8]. The via middle approach limits the TSV insulator deposition temperature to less than 400 °C to prevent compromising the FEOL fabricated transistors. CVD SiO₂ is selected for TSV insulation in our process due to its good isolation properties and conformality.
Even with an insulation oxide liner between the copper via and the silicon substrate, it is still quite common for copper to diffuse through the oxide into silicon, especially in the presence of a voltage bias. Therefore, following SiO$_2$ insulation layer, a diffusion barrier comprised of tantalum nitride (TaN) is sputtered onto the dielectric layer. To improve adhesion between the barrier material and the copper, a tantalum (Ta) adhesion layer is subsequently sputtered onto the TaN. A CVD Ru adhesion promoter is also applied in this process flow to provide robust conformal coverage for satisfactory 10:1 aspect ratio via isolation[6]. A copper seed layer is then deposited for efficient copper plating during the via filling step.

### 2.2.3 Via filling and front side metallization

For TSV metal fill, electrochemical deposition (ECD) of copper is used comparable to conventional BEOL damascene copper electroplating for CMOS. The electroplating of copper is based on an electrochemical reaction in an electrolytic solution bath containing CuSO$_4$ and other additives. In the electrolytic solution, a voltage is applied between the cathode (Cu seed layer) and an anode (an inert metal). The voltage difference drives a current in the anode or copper ions in the chemical bath to be reduced as neutral copper deposited on surface of the cathode (seed layer). Solution additives can be accelerators aiding the deposition rate and film quality. A strong accelerator can help plate copper at the bottom of the via much faster than at the top for a so-called bottom up process [10]. The bottom up deposition method can fill the via without ‘seam’ voids and with minimum overburden (extra Cu plated on the top surface) [6]. Copper is usually used as an anode because it can be dissolved into the chemical solution to replenish the copper ions for deposition. For high aspect ratio vias (our TSVs incorporate a 1:10 aspect ratio), reverse pulse plating is used where the current is applied in short pulses to give the plating chemical enough time to refresh its concentration at the surface [8].

To remove the overburden from Cu electroplating, chemical mechanical planarization (CMP) is applied after Cu ECD. CMP is a standard process used for removing excess surface materials in CMOS IC fabrication. It uses nano-abrasive and corrosive chemical slurries in conjunction with a rotating polishing
pad. The pad and wafer are pressed together by a dynamic polishing head, which is rotated in an inverse direction to the pad’s rotating direction. This process removes material and tends to mitigate irregular surface topography induced by the Cu ECD process.

After polishing, the front side metallization process (conventional BEOL damascene process) is carried out for horizontal interconnect fabrication. The test structures studied in Chapter 4 have one layer of metal on the front side that directly connects to the TSVs. The multi-tiered 3D wafer stack studied in Chapter 5 incorporates two layers of metal on front side with the second layer metal utilized for purposes of Cu-Cu bonding. The full 3D CMOS test structure outlined in Chapter 6 has 5 1× metal and 2 2× metal layers on the front side for signal routing and power ground network wiring.

### 2.2.4 Via reveal and back side metallization

After completion of the front side metallization, the TSVs are revealed from the backside through a wafer thinning process. This is a multi-step process that includes aligning, bonding, grinding and final polishing. Before grinding, the handle wafer is aligned to the device wafer with bond pattern marks to ensure accuracy of the backside lithography process. The bare thin wafer is not sufficiently mechanically stable to be handled for grinding, thus the TSV wafer must be supported by a handling substrate. The front side of the TSV wafer is first temporarily glued to the handling wafer by applying an adhesive material. After joining with the handling wafer, the TSV wafer is ready for backside grinding. A coarse grind is first applied to remove most of the bulk silicon, followed by a fine grind to ensure global planarization and refine the surface [11]. The temperature during the grinding process is kept under 200 °C to avoid wafer de-bonding from the handling wafer. The grinding is terminated several micrometers above the TSV and a polish step is applied to remove the remaining thin layer of silicon together with any residual crystal defects. The final TSV ‘revealing’ process step removes silicon from above and around the TSV to leave the TSV protruding from the surface of the wafer[12]. Etching technology with good selectivity to the via dielectric liner materials can be used to remove the remaining silicon above the TSVs[13].
After the TSV reveal step, the backside metallization process follows. Less than 1µm thick SiO$_2$ is first deposited on silicon surface and polished with CMP process to form the inter level dielectric (ILD) below the metal layer. TSV protrusion heights of 0.5 to 1µm are required to ensure a robust contact between the first metal layer and the TSV [14]. Lastly, the backside metal layer is processed using a conventional damascene process. Due to the challenges inherent in processing the backside of the wafer, all test structures in this study were limited to one or two layers of metal on the backside, utilized primarily for forming the Cu-Cu mechanical bond between stacked wafers. The routing metal interconnects are primarily processed on the ‘front side’ of the wafer tier.

Figure 2.3 shows the cross sectional focused ion beam (FIB) SEM image of a fabricated TSV dual chain test structure (discussed in detail in Chapter 4). The complete dual chain test vehicle was fabricated using a Cu-based TSV process followed by front side and backside metallization processes[15]. The backside metal layer was used for electrical probing to perform electrical characterization. As evident in Figure 2.3, voids occasionally formed inside the TSVs during electroplating process (Section 2.2.3). A handle wafer was bonded to the front side to facilitate backside metallization and to mechanically support electrical characterization on the final, thinned 50µm TSV wafer.

### 2.3 3D stacking and bonding techniques

Distinct from traditional 2D IC fabrication, wafer stacking and bonding are critical processes for 3D IC fabrication. Different stacking methodologies have been proposed to realize 3D IC including wafer-to-wafer, die-to-wafer, or die-to-die stacking[8], [16]. Each approach has its own advantages, disadvantages and applications. The die-to-die method has the highest yield because each die is prescreened to be a ‘known good die’ (KGD) before stacking and bonding. However, it suffers from low throughput due to the prescreening process. Similarly, die-to-wafer approaches can integrate KGDs to a wafer with higher throughput due to the wafer scale process. Electrostatic discharge (ESD) is an intrinsic problem for these two approaches during the pick-and-place process. Lastly, the wafer-to-wafer approach has the potential to provide high throughput, better reliability and low cost.
However, without prescreening, the wafer level integration suffers from loss of yield due to lack of KGDs and less design flexibility. In most cases, the die sizes are different for each stack for different functionalities. For high volume manufacturing in the near future, wafer-to-wafer stacking is seen as the most promising approach for large-scale 3D integration[17]. In our study, die-to-wafer bonding on a 300mm wafer was used to balance yield and throughput. In the following section, two critical steps are discussed including wafer alignment and bonding process.

### 2.3.1 Wafer alignment

For both the backside lithography process and multi-stack wafer packaging, the wafer alignment accuracy determines the functionality, reliability and yield of the 3D integration approach. TSV diameter and bond pad size impact the alignment tolerance. During the design phase, alignment marks are typically inserted into layouts and transferred onto the fabricated masks for lithographic alignment. Optical alignment and infrared radiation (IR) alignment are often used to align the wafers prior to bonding. The choice of alignment approach depends on the misalignment tolerance, the feature sizes and substrate conditions. For the test vehicles in this study, optical alignment is used for the 5.5µm diameter TSVs (discussed in
Chapter 5) with various sized bond pad. Figure 2.4 shows the tolerable misalignment (less than 0.5\(\mu\)m) between stacked dies. The misalignment is much smaller than the feature size of the TSV and the bond pad and doesn’t affect the electrical connection of the bonding.

![Cross sectional SEM image of bonded wafer showing tolerable bonding misalignment](image)

Figure 2.4 cross sectional SEM image of bonded wafer showing tolerable bonding misalignment

### 2.3.2 Wafer bonding

For the 3-tier 3D wafer stack discussed in Chapter 5, each of the top two wafer ‘tiers’ are processed for TSVs, front side metallization, and handled for thinning and backside metallization. The bottom ‘tier’ in the 3-tier stack is a full-thickness wafer possessing only topside metal layers for bonding and routing. When all three tiers are completed with respect to full-wafer processing, the top two tiers are diced to single dies and tested to select KGDs for bonding on the bottom wafer. Before the bonding process, the first step is preparation of the wafer surface in terms of cleanliness and flatness to ensure bonding quality.

Wafer bonding is the process by which the electrical and mechanical connections between stacked the dies and wafers is formed. There are many approaches that have been utilized to form these connections including solder with different materials, polymer bonding, copper pillar connections, direct Cu-Cu bonding etc. [16], [18]. For the 3-tier 3D wafer stack discussed in Chapter 5 we utilized direct Cu-Cu bonding because it is reported to be able to provide reliable electrical connections (and thermal
connections) without introducing other materials and extra processing steps as would be required for solder bonding or polymer bonding. The fundamental mechanism for Cu-Cu thermo-compression bonding is metal ion diffusion[19]. Pressure, time and temperature impact the diffusion rate and bonding quality. The Cu-Cu bonding temperature is constrained by thermal budget to avoid damaging the processed devices and on-wafer interconnects. The bonding process requires uniform pressure and temperature to ensure good bonding yield over the die and wafer[20]. Mechanical die-to-wafer alignment is sensitive to temperature gradients, thus a low heating ramp rate is critical. To avoid copper oxidation before or during the bonding, the die/wafer is contained in an ambient of nitrogen or other reducing gas during heat up. Figure 2.5 shows a SEM cross-section of a ‘good’ uniform Cu-Cu bond between stacked wafers. From the SEM image, the bonding interface is not visible. This lack of contrast indicates good contact between the Cu bond pads from the two wafers and promotes good electrical connectivity.

![SEM image of a Cu-Cu bond](image)

**Figure 2.5 Cross sectional SEM image of a Cu-Cu bond between stacked wafers**

The die constituting the three ‘tiers’ of the stacked 3D test structure evaluated in Chapter 5 were fabricated with distinct die sizes of 7mmx7mm, 7mmx10mm, and 7mmx11mm, respectively (listed in order from the top tier die to the bottom tier die). The extra area at the edges of the middle and lower dies
provides extra I/O and probing pad area for testing purposes. Figure 2.6 is a tilted angle SEM image of our fabricated Cu-Cu bonded 3-tier stack[7].

![Tilted angle SEM image of 3 tier stack wafer by direct Cu-Cu bonding[7]](image)

As can be seen in Figure 2.6, linear arrays of front side probing pads and interconnects are accessible on the surface of each die to facilitate intra-tier and inter-tier electrical measurements. The high-speed via chain test structures’ probe pads are on the top tier of the stack to enable paired RF probes to test multi-stacked via chains.
References


of TSVs and RDLs fabricated from the backside of a thin wafer,” in *2013 IEEE International 3D Systems Integration Conference (3DIC)*, 2013, pp. 1–5.


CHAPTER 3 Characterization and Simulation Fundamentals

As the chip to chip data transfer speed and data throughput for many chip-based applications continue to increase with the performance scaling of semiconductor devices, it is important to investi-gate the high speed signal transmission properties of signal channels in 3D IC systems[1]–[5]. For the high speed digital and RF/microwave signals required in high-performance 3D heterogeneous systems, the 3D communication channels carries signals over a broad range of frequencies. All high frequency signal transmission utilize electromagnetic (EM) wave propagation based on Maxwell’s equations[6]. Figure 3.1 (a) shows an illustration of EM wave propagation in a typical ground/signal twin pair for a macro-scale, traditional high frequency signal transmission application. Figure 3.1(b) shows one example from our study of a 3D signal transmission line configuration incorporating TSVs in a 3D IC system. In that figure the orange vertical cylinders are TSVs for inter-die connections, while the blue lines represent coplanar wave guides (CPWs) on the top and bottom surfaces of a thinned silicon wafer. The black arrows indicate the wave propagation direction. In Chapter 4 and Chapter 5, we present investigations of the signal transmission performance within such 3D channels utilizing both experimental and simulation results.

Figure 3.1 EM wave propagation in: (a) a typical Ground/signal twin pair wire; (b) an example of test structure in this study- a 3D channel with 1S2G TSV array.

An electrical circuit is a network consisting of a closed loop, giving a return path for the current. Network analysis is a useful mathematical circuit analysis technique to isolate portions of larger circuits under
study. A two-port network is an example of such an analysis where the network itself is regarded as a ‘black box’ with signal transmission and reflection properties specified by a defined numerical matrix[7]. One particularly useful network analysis construct for high frequency signal transmission is the so-called S-parameter matrix. Distinct from other electrical circuit matrices such as the Y, Z matrices that are derived from terminal voltages and currents (problematic for high-frequency signal analysis), the S-parameters relates to the traveling EM waves that scattered or reflected at the network port. The S-parameter is a more straightforward approach to measure and analyze high frequency signal transmission[8]. In this study, a Vector Network Analyzer (VNA) was used to experimentally characterize S-parameters of 3D Channels. In addition, finite element modeling and lumped equivalent circuit modeling were employed to simulate S-parameters frequency dependence for various 3D channel models corresponding to the fabricated 3D test structures. In this chapter, we will review the fundamentals of S-parameters, how simulation software calculates S-parameters and how we use the VNA instrument to measure S-parameters for our 3D channel test structures.

### 3.1 Scattering parameters

#### 3.1.1 S-parameters derivation

In a two port network system as shown in Figure 3.2, each port has two terminals where the normalized complex voltage waves $a_i$ and $b_i$ are incident on and reflected from the port of the network. The S-parameters can be derived from Maxwell’s equation and the phasor form of voltage and current[9]. The reference impedance of the system is $Z_0$, which is typically designed to be 50Ω.
Considering the wave property of the signal, the phasor form of voltage and current at each port are:

\[ V(x) = V^+(x) + V^-(x) \]  \hspace{1cm} (3.1)
\[ I(x) = \frac{V^+(x)}{Z_0} + \frac{V^-(x)}{Z_0} \]  \hspace{1cm} (3.2)

We can normalize the amplitude of phasor ‘waves’ to \( Z_0 \):

\[ a(x) = \frac{V^+(x)}{\sqrt{Z_0}} \]  \hspace{1cm} (3.3)
\[ b(x) = \frac{V^-(x)}{\sqrt{Z_0}} \]  \hspace{1cm} (3.4)

The independent variables \( a_1 \) and \( a_2 \) are normalized incident voltages, as follows:

\[ a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{Voltage wave incident on port 1}}{\sqrt{Z_0}} \]  \hspace{1cm} (3.5)
\[ a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{Voltage wave incident on port 2}}{\sqrt{Z_0}} \]  \hspace{1cm} (3.6)

Dependent variables \( b_1 \) and \( b_2 \) are normalized reflected voltages:
\[ b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{Voltage wave reflected from port 1}}{\sqrt{Z_0}} \quad (3.7) \]

\[ b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{Voltage wave reflected from port 2}}{\sqrt{Z_0}} \quad (3.8) \]

We define the 2x2 S matrix for a two port system as follows:

\[
\begin{pmatrix}
  b_1 \\
  b_2
\end{pmatrix} =
\begin{bmatrix}
  S_{11} & S_{12} \\
  S_{21} & S_{22}
\end{bmatrix}

\begin{pmatrix}
  a_1 \\
  a_2
\end{pmatrix} \quad (3.9)
\]

The S-parameters are:

Input reflection coefficient with the output port terminated by a matched load:

\[ S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad (3.10) \]

Output reflection coefficient with the input port terminated by a matched load:

\[ S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad (3.11) \]

Forward transmission coefficient (insertion loss) with output port terminated in a matched load:

\[ S_{21} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (3.12) \]

Reverse transmission coefficient (insertion loss) with input port terminated in a matched load:

\[ S_{12} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (3.13) \]

A network is reciprocal if it is passive and contains only reciprocal materials that influence the transmitted signal. In this dissertation study, we focus primarily on passive interconnects in a 3D system which are reciprocal. Since \( S_{12} = S_{21} \), \( S_{11} = S_{22} \) and the S matrix is equal to its transpose, we only show simulated and measured results for \( S_{11} \) and \( S_{21} \).

S-parameter matrices are complex numbers that are expressed in either real/imaginary number format, or magnitude/angle format. Magnitude/angle format is used more frequently because it directly provides
information about loss/gain and phase. The S-parameter magnitude may be expressed in linear form or logarithmic form. When expressed in logarithmic form, magnitude has the dimensionless unit of decibels (dB). In this study, we display S-parameters (calculated or measured) of our 3D test structures in dB/degree format. Because our structures are passive devices, the $S_{21}$ matrix element denotes the insertion loss in dB format as:

$$IL = -20 \log_{10} |S_{21}| dB$$

(3.14)

The insertion loss can be introduced as an intrinsic loss in the device under test (DUT) and/or mismatch. The $S_{11}$ matrix elements denotes the return (commonly referred to as reflection) loss in dB format as:

$$RL = -20 \log_{10} |S_{11}| dB$$

(3.15)

The cofactor of 20 is included because the loss is a power ratio while the S-parameters are calculated as a voltage ratio[9]. For a clear intuitive understanding of dB level representation of power, we list representative dB ratings and the corresponding power ratio and amplitude ratio in Table 3.1 for several 3D channel elements utilized in our 3D test structures. The Table also includes the typical value range of the loss characterized from our test structures.

Table 3.1 Typical values for dB and notes for results presented in this dissertation

<table>
<thead>
<tr>
<th>dB</th>
<th>Power ratio</th>
<th>Amplitude ratio</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>No loss</td>
</tr>
<tr>
<td>-1</td>
<td>0.794</td>
<td>0.891</td>
<td>2 TSV chain IL below -1dB up to 65GHz</td>
</tr>
<tr>
<td>-3</td>
<td>~0.5</td>
<td>0.708</td>
<td>-3dB cutoff frequency (half power drop)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Stacked 4 via chain IL range &gt;50GHz</td>
</tr>
<tr>
<td>-10</td>
<td>0.1</td>
<td>0.316</td>
<td>Return loss range</td>
</tr>
<tr>
<td>-20</td>
<td>0.01</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>-30</td>
<td>0.001</td>
<td>0.032</td>
<td></td>
</tr>
</tbody>
</table>
3.1.2 Examples of S-parameters plot

S-parameters can be used to characterize and analyze various types of passive as well as active devices and networks in microwave and RF electronic circuits. In this dissertation study, we focused on passive 3D high frequency and high-speed channels. Figure 3.3 shows the simulated frequency dependence of a typical insertion loss parameter, $S_{21}$, and return loss parameter, $S_{11}$, in dB scale for a low loss transmission line from DC to 50GHz (plotted over a linear frequency scale). The S-parameter matrix frequency dependence is typically cast as a 3D matrix that the third component representing frequency.

![Graph showing S21 and S11 parameters](image)

Figure 3.3 Insertion loss S21 and return loss S11 data for a low loss transmission line

The data plot in Figure 3.3 provides information regarding the transmission line’s insertion loss and return loss due to DUT intrinsic parameters over the frequency range from DC to 50GHz. Both insertion and return loss increase with increasing frequency. For a low loss-transmission line at 50GHz the insertion loss is only -0.8dB which corresponds to less than a 20% signal power loss through the transmission. The insertion loss dependence on frequency is relatively uniform and roughly 0.04dB/decade. The -3dB cutoff frequency is a figure of merit for signal transmission channel which denotes the point at which half of the signal power is attenuated[10]. For high-speed signal transmission or RF/analog signal transmission, it is desirable for the insertion loss to be as low as possible over the
operating frequency range to ensure integrity of the data pulse shape and retention of the information carried by the signal.

A return loss of -10dB at 50GHz denotes that 10% of the signal power is reflected at the port. From the data in Figure 3.3, it is clear that the return loss is increasing faster at lower frequency – from -60dB at DC to -30dB at 5GHz. In contrast, the slope of the return loss from 10GHz to 50GHz is about 0.3dB/decade.

3.2 Simulation and modeling methods

For high frequency and RF systems, finite element modeling (FEM) and lumped element circuit modeling can be used to accurately model and extract the electrical signal transmission parameters for arbitrary structures. Good correlation between simulation and experimental characterization validate the models used and help researchers understand the underlying physics dominating signal propagation and the impact of various transmission channel design elements. In this dissertation, we used FEM modeling and lumped circuit modeling to simulate the high frequency signal transmission property of 3D high-speed channels.

3.2.1 Full wave finite element method modeling

Finite element modeling is a numerical technique for determining approximate solutions to boundary value problems for partial differential equations[11]. The ANSYS High Frequency Structure Simulator (HFSS) was used for investigations presented in this dissertation. It is based on finite element modeling to calculate electromagnetic field solutions. In general, the geometric models of the test structure were built in the HFSS 3D modeler, and then proper boundary conditions and excitation ports were assigned[12]. An example of a 1S2G TSV array model geometry used for an HFSS simulation is shown in Figure 3.4. The excitation wave ports are denoted as circles on the top and bottom surfaces of the signal (center) TSV. It is necessary to understand how simulation works in order to enable useful analysis of the results. A detailed simulation working process is described in the following section.
In HFSS, before the simulation calculations start, the geometric model is automatically divided into a large number of tetrahedra. Figure 3.5 shows the field quantities at each tetrahedron that are calculated by the simulator. The value of a vector field quantity such as the E-field or H-field at points inside each tetrahedron is interpolated from the vertices of the tetrahedron. At each vertex, HFSS stores the components of the field that are tangential to the three intersecting edges of the tetrahedron. At the midpoint of each edge, the component of the field that is tangential to the face of an element and normal to an edge is explicitly stored[12]. By representing field quantities in this way, the system can transform Maxwell’s equations into matrix equations that are solved using traditional numerical methods.

This collection of tetrahedra is referred as the mesh for a given HFSS simulation geometry (e.g. a 3D high-frequency channel). To produce the optimal mesh, HFSS uses an iterative process to automatically generate refined meshes in critical regions. Starting from a solution based on a coarse initial mesh, the HFSS software refines the mesh in areas of high error density and generates a new solution to reduce the error for a given simulation.

To compute the field quantities, it is critical to include accurate boundary conditions for the model and excitation ports that indicate the input and output waves[13]. The boundary conditions should be set as
close as possible to a real system condition. In our analysis of full 3D channel test structures composed of CPW and TSVs, the boundary condition is set as radiation at the surface of the air box that covers the silicon wafer and test structures.

Figure 3.5 The representation of detailed field quantities at each tetrahedron during numerical calculation[12]

A port is a 2D surface at which the fields will be solved according to Maxwell’s equations to determine appropriate RF modal excitations into the 3D model volume. In general, the excitation port can be set as a wave port or lumped port depending on the model and the wave modes. Wave ports solve actual field distributions in cross-sections. Lumped ports excite simplified field distributions to permit S-parameter outputs where wave ports are not feasible. Because our model TSV and CPW lines are interfaced to a thin layer of dielectric silicon dioxide and connected to the semiconducting silicon substrate, this non-uniform interface determined the wave propagation speed difference in those materials. Thus the high frequency 3D channel signal is transmitted as a quasi-TEM mode wave[14]. Most non-TEM excitations require wave ports for a model field distribution solution. In addition, a wave port is usually preferred for HFSS simulation. Therefore, wave ports are used in our 3D high-speed channel HFSS simulation. Every port is excited separately to generate a solution and each mode on the port contains a time-averaged power of 1 watt. In a 2-port system as in this study, port 1 is excited with 1 watt of signal power and port 2 is set to 0. After the solution is generated, port 2 is excited with 1 watt of signal power and port 1 is set to 0[12].
To calculate S-parameter results for signals over a wide range of frequency, a frequency sweep needs to be set during HFSS solution processing. There are three types of HFSS frequency sweeps: fast frequency sweep; discrete frequency sweep; and interpolating frequency sweep. Fast frequency sweep costs the least amount of simulation time but may involve higher error, while discrete frequency sweeps yield the most accurate results because it calculates field information at each frequency point. However, the latter is very time consuming. Interpolating frequency sweeps yield lower error than fast frequency sweeps but with less time than discrete frequency sweeps. Therefore in this study, we used interpolating frequency sweeps for our HFSS simulation studies for optimum simulation performance.

After the HFSS field calculations reach convergence, the calculated S-parameters as well as the electromagnetic field value are stored. In some cases, detailed signal field information will provide more insights regarding the wave propagation properties of the model in the 3D channel and help users analyze simulation problems or artifacts. In addition, in HFSS, the magnetic field (H-field) is less accurate than the solution for the electric field (E-field) because the H field is computed form the E-field using the relationship as in Equation 3.16 [15].

\[ H = \frac{\nabla \times E}{-j\omega \mu} \]  

(3.16)

Thus in the detailed analysis with electromagnetic field, we mainly show the electric field distribution from the models.

### 3.2.2 Lumped element modeling with equivalent circuits

In addition to HFSS, lumped element modeling was used to simulate signal transmission in 3D channels. Lumped element modeling simplifies the physical structure into a topology consisting of discrete circuit elements such as resistances, capacitances, and inductances (RLC)[16]. There are many circuit simulation software packages available including Agilent ADS, ANSYS Ansoft Designer, and Cadence Spectre etc. In this study, we used Agilent ADS for lumped circuit model simulations for frequency domain
characterization of S-parameters, and used Cadence Spectre with corresponding IC fabrication process libraries for high speed signaling studies from the circuit perspective.

The lumped element model approach is valid whenever the circuit characteristic length is much shorter than the operating wavelength[9]. The 3D high-speed channel components in our study are geometrically short compared to the wavelength of the high frequency signal of interest. The highest frequency in this study is 65GHz, which corresponds to a wavelength of about 4.6mm. The rule of thumb for using lumped element circuit models is that the component dimension is at approximately 1/10 of the wavelength[7]. In our study, the TSV length is 50µm which is far shorter than 1/10 of the 65GHz wavelength.

Simulations using lumped element models have three main benefits: 1) Calculation speed is much faster compared with full wave finite element HFSS simulation; 2) It provides more insights of the impact of the detailed electrical properties of the 3D components (e.g. resistance, capacitance and inductance) on overall transmission properties; 3) Accurate models can be implemented directly in electronic design automation tools to facilitate performance evaluation of 3D channels prior to system design.

In our 3D high-speed channel study, the discrete circuit elements, RLC, are calculated from analytical equations from the component geometry and material properties. The full path included vertical TSVs and planar redistribution layer (RDL) interconnects for a single wafer, plus bonding pads for multiple-tier systems. The detailed analytical models for each of those components are presented in the following sections. Because the circuit elements are calculated with ideal geometry and material parameters (absent variations encountered in real fabricated devices), the results calculated from the analytical equations, while giving reasonable ranges, require proper fitting mechanisms to determine the most accurate electrical element values (RLC) compared to experimental results.

### 3.2.2.1 TSV model

A high-speed signal channel in a 2D or 3D IC requires a full circuit or ‘loop’ composed of a signal path and a return path to propagate high frequency EM waves[10]. A signal/ground TSV pair is the basic
construct of such a high speed TSV configuration. Other configurations such as 1SXG TSV array models (TSV arrays incorporating a single signal TSV and multiple ground TSVs) can be compressed and simplified to conform to the basic model of a S/G TSV pair but with proper parameter modifications respecting the ground TSV configurations. For example, additional ground TSVs will have higher oxide insulation capacitance as well as higher coupling capacitance between signal and ground TSV. Details related to these effects will be discussed in Chapter 4 and Chapter 5 for lumped element modeling sections. In this section, we provide the basic model details for a S/G TSV pair. Figure 3.6 shows the schematic of a signal/ground TSV pair with landing pads for vertical to horizontal path connection and their geometrical parameters. Figure 3.7 shows the proposed electrical model for the same structure (signal TSV with a ground TSV with landing pads).

Figure 3.6 Schematic of a signal ground TSV pair with landing pad for vertical to horizontal connection and their geometrical parameters
In essence, the TSV is a copper wire (aspect ratios typically ranging from 10:1 to 20:1) vertically traversing a thinned silicon wafer. To electrically isolate the TSV from the semiconducting silicon substrate, an insulation dielectric layer surrounding the TSV is needed. In our study, we used silicon dioxide for the dielectric material. Due to this insulation, there is an oxide capacitance, \( C_{ox} \). The oxide capacitance can be calculated using a coaxial cable capacitance model \[C_{ox} = 2\pi \varepsilon_0 \varepsilon_{r,ox} \frac{h_{TSV}}{d_{TSV}/2 + t_{ox}} \ln \left( \frac{d_{TSV}/2}{d_{TSV}/2 + t_{ox}} \right) \] (3.18)

The DC resistance of a TSV, \( R_{TSV} \), is modeled with structural parameters as shown in Equation 3.19.

For high frequency AC signals, we need to consider the ‘skin effect’, i.e. the current flows close to the surface of the via due to internal eddy currents. The conductor skin depth is defined by material properties and is frequency dependent as shown in Equation 3.21. Therefore, the AC resistance is frequency dependent as shown in Equation 3.20, which is inversely proportional to square root of frequency \[ R_{TSV} \].
resistance effect is negligible compared to the TSV’s high capacitance effect, we simplify the model with a fixed resistance within a reasonable range calculated from the DC and AC resistance. Simulation results presented in Chapter 5 validate this assumption and simplification.

\[ R_{dc,TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times \left( \frac{d_{TSV}}{2} \right)^2} \text{[\Omega]} \quad (3.19) \]

\[ R_{ac,TSV} = \rho_{TSV} \times \frac{h_{TSV}}{2 \pi \times \frac{d_{TSV}}{2} \times \delta_{TSV} - \pi \times \delta_{TSV}^2} \text{[\Omega]} \quad (3.20) \]

\[ \delta_{TSV} = \frac{1}{\sqrt{\pi f \mu_{TSV} \sigma_{TSV}}} \text{[m]} \quad (3.21) \]

The TSV inductance can be modeled as one half of a loop inductance between two parallel conducting wires[17]. As the operating frequency increases, the impedance of the inductance becomes more dominant than that of the resistance.

\[ L_{TSV} = \frac{1}{2} \left( \frac{\mu_0 \mu_{r,TSV}}{2\pi} \times h_{TSV} \times \ln \left( \frac{p_{TSV}}{d_{TSV}/2} \right) \right) \text{[H]} \quad (3.22) \]

The coupling capacitance between signal and ground TSV, \( C_{Si} \), can be obtained by applying a parallel-wire capacitance model[9].

\[ C_{Si} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,si} \text{cosh}^{-1} \left( \frac{p_{TSV}}{d_{TSV}} \right)}{\cos^{-1} \left( \frac{p_{TSV}}{d_{TSV}} \right)} \times h_{TSV} \text{[F]} \quad (3.23) \]

And the conductance between the signal and ground TSV can be derived from equations relating the dielectric loss and capacitance relation[18]. The physical origin of the conductance is the silicon conductivity, which is predominantly determined by the doping concentration of the silicon wafer.

\[ \frac{G_{Si}}{G_{st}} = \frac{\varepsilon_{Si}}{\sigma_{Si}} \quad (3.24) \]

\[ G_{Si} = \frac{\pi \times \sigma_{Si} \text{cosh}^{-1} \left( \frac{p_{TSV}}{d_{TSV}} \right)}{\cos^{-1} \left( \frac{p_{TSV}}{d_{TSV}} \right)} \times h_{TSV} \text{[S]} \quad (3.25) \]
In 3D ICs, to yield a better connection between TSVs and planar metal lines, a design rule for a square-landing pad to cover the TSV (with a width slightly bigger than TSV diameter) is included in the last metal layer. Due to the insulation layer between the metal landing pad and the conducting silicon substrate, there is a landing pad capacitance included in the TSV model. The calculation is based on a parallel plate capacitance model:

\[
C_{pad} = \varepsilon_0 \varepsilon_{r,ox} \frac{d_{pad} - \pi \left(\frac{d_{TSV}}{2}\right)^2}{t_{ox,IMD}} [F]
\]  

(3.27)

### 3.2.2.2 RDL model

The redistribution layer interconnect (RDL) is a metal interconnect that provides horizontal electric connections between the TSVs and distribution of signals and power over different stacked dies. Similar to TSV modeling, an equivalent circuit model for the RDL component is proposed to estimate the electrical characteristics and include its impact on the overall 3D channel signal transmission characteristics[18]. The RDL model is shown in Figure 3.8.

Because the RDL uses the first metal layer on a thinned Si tier, the corresponding RLC can be derived from the detailed library parasitic models obtainable from standard process design kits. Related analytical equations are:

\[
R_{dc,RDL} = \rho_{RDL} \times \frac{L_{RDL}}{w_{RDL} \times t_{RDL}} [\Omega]
\]  

(3.28)

\[
R_{ac,RDL} = \rho_{RDL} \times \frac{L_{RDL}}{w_{RDL} \times \delta_{RDL}} [\Omega]
\]  

(3.29)

\[
\delta_{RDL} = \frac{1}{\sqrt{\pi f \mu_{RDL} \sigma_{RDL}}} [m]
\]  

(3.30)
The inductance of the RDL is determined with a loop inductance model by approximation to a two-wire transmission line model[19].

$$L_{RDL} = \frac{1}{2} \left( L_{signal} + L_{GND} - 2M \right)$$

$$= \frac{1}{2} \left\{ \frac{\mu_0 \mu_r \cdot \text{RDL}}{2\pi} \cdot \left[ \ln \left( \frac{2 \times l_{RDL}}{t_{RDL}} \right) - \frac{3}{4} \right] + \frac{\mu_0 \mu_r \cdot \text{RDL}}{2\pi} \cdot \left[ \ln \left( \frac{2 \times l_{RDL}}{t_{RDL}} \right) - \frac{3}{4} \right] \right\} [H]$$

$$- 2 \times \frac{\mu_0 \mu_r \cdot \text{RDL}}{2\pi} \times \left[ \ln \left( \frac{2 \times l_{RDL}}{t_{RDL}} \right) - 1 \right] [H]$$

The detailed capacitance model includes detailed analysis of the electric field distribution between the RDL metal line and adjacent RDL line and to the silicon substrate. The fringe capacitance includes the capacitance from the air between the RDLs, the insulation dielectric between RDLs, and the dielectric layer underneath the RDLs. The model approximations can be obtained from parasitic RC models provided by the process design kit. Note that the values are highly dependent on the specific fabrication process and technology node.
3.2.2.3 Bonding pad model

For the 3D wafer stack bonding utilized for this dissertation, direct Cu-Cu bonding was used due to its facile integration with available FEOL and BEOL process flows. Also, it avoided introducing possible contamination sources compared to other wafer stack bonding methods such as solder bump bonding. In our 3D stack designs, there is a specific metal layer designated as a bonding metal (Cu) layer. This is different and distinct from the RDL metal layer that was discussed in the previous section. Between these two metal layers (RDL and bonding layer), an array of vias was used to form electrical connection. In order to lower the resistance from a single via, multiple via in parallel are preferred. However, those vias’ parasitic capacitance increases the overall capacitance. Thus the bond pad capacitance includes both via capacitance and the parallel plate capacitance from the dielectric layer between the bond pad metal and the RDL metal as well as the silicon substrate. The detailed via capacitance can be calculated and derived from detailed RC models from the process design kit. To simplify the model, we define the total capacitance as \( C_{\text{bondpad}} \).

![Equivalent circuit model for Cu-Cu bonding pad](image)

Figure 3.9 Equivalent circuit model for Cu-Cu bonding pad that including capacitance from both pad and via connecting pad to the last metal layer

The value can be tuned in the model. Details will be discussed in Chapter 5 in the modeling section. Because of the short length in the signal transmission direction, the resistance and inductance of the bond pad is very small and negligible compared with that of the TSV and RDL. Therefore we simplified the bonding pad model to be a capacitor as shown in Figure 3.9.
3.3 RF characterization techniques

3.3.1 Instrumentation

A Vector Network analyzer (VNA) is the instrument that is often used to characterize networks such as transmission lines, amplifiers, and filters in the frequency domain. VNAs commonly measure S-parameters since signal reflection and transmission in electrical networks are straightforward to measure at high frequencies compared to other network parameters as discussed in the previous section[20]. Figure 3.10 shows the diagram of a typical 2 port VNA[21]. The central DUT is the device under test. In our study, it is one of various 3D test structures. P1 and P2 are the two ports connected to the VNA. The test port connectors provided on the VNA itself are a high-precision type, which will normally have to be extended and connected to P1 and P2 using precision cables PC1 and PC2 and suitable connector adaptors A1 and A2.

In practice, a VNA utilizes a variable frequency carrier wave (CW) source that generates the test frequency and a variable attenuator that adjusts the power level. The position switch (SW1) sets the direction of the signal passing through the DUT. When the switch is at 1, the signal incident on port 1 and the VNA measures $S_{11}$ and $S_{21}$ and vice versa. The splitter 1 splits the signal to a reference channel connecting to RX REF1 and a test channel connecting to P1 via directional coupler (DC1), PC1, and A1. The configuration is similar for signals leaving P2. RX TEST and RX REF are known as coherent receivers as they share the same reference oscillator and they are capable of measuring the test signals’ amplitude and phase at the test frequency. All of the complex receiver output signals are fed to a processor, which carries out the mathematical processing and displays the chosen parameters and format on the phase and amplitude display. The VNA used in this study is with a slightly different configuration to measure required terms.
In this study, we used an Agilent N5277A VNA and a Cascade Microtech Summit 1200B semi-automatic probe station to conduct S-parameters measurements up to 65GHz, as shown in Figure 3.11(a). The VNA consists of a sweep oscillator - a test set that includes two ports, a control panel, an information display and RF cables to hook up to the DUT. Compared to Figure 3.10 (diagram of a VNA components) the two ports from VNA connect to the probes through coaxial cables. The probes that were used to contact the test structure probe pads are coplanar waveguide (CPW) probes. We used 150µm GSG pitch and 50µm GSG pitch for different test structure needs. The CPW probe tips are constructed from nickel alloy to prevent oxidation and ensure low contact resistance between the wafer copper pads[22]. The probe station is mounted to a passive vibration table to prevent probe damage during measurements. The microscope associated with the probe station is to aid in placing the fine probe tip on the DUT and inspecting the proper probe contacts. In addition, there is a computer associated with the VNA to operate calibration.
computations and store the measurement data. Figure 3.11(b) shows a zoomed picture of probes contacting to DUT under microscopic inspection during tests.

![Characterization setup with Agilent VNA and Cascade Semi auto RF probe station in (a); Zoomed picture of probing on DUT in (b)](image)

3.3.2 Calibration methods

VNAs provide high measurement accuracy by calibrating the test system using a mathematical technique called vector error correction (this is a user calibration distinct from manufacturer’s calibration to ensure the instrument retains proper functioning after extended use and with various probe sets). Vector error correction accounts for measurement errors in the network analyzer itself, as well as the test cables, adapters, fixtures, and probes that are between the VNA and the DUT. Calibrating a VNA based test system removes the largest contributor to measurement uncertainty, which are systematic errors. Systematic errors are repeatable, non-random errors that can be measured and removed mathematically[23]. A vector error corrected VNA system provides the best picture of true performance
of DUT. Therefore, a good calibration is very critical to the high frequency electrical measurement with VNA.

3.3.2.1 NIST Multi-line TRL Calibration

There are many on chip and off chip calibration techniques used in RF/microwave VNA measurements. These include the Short Open Load Thru (SOLT), SOL, Thru Reflect Line (TRL), Line Reflect Reflect Match (LRRM) etc.[23] SOLT calibration is simple to implement and locates the reference plane of the VNA measurement at the ends of the coaxial cables used during the calibration procedure. It is frequently used in coaxial measurement but only removes six of the error terms and can only provide accurate results for low-frequency measurements. In our study, the test structures are fabricated on-wafer and the reference plane cannot be defined at the end of the coaxial probe cables. Therefore it was necessary to use full, 12-error model calibration methods (shown in Figure 3.12) since our 3D test structures will be characterized with a broad frequency range up to 65GHz.

![Figure 3.12 Full two port, 12 term error model used for TRL calibration][24]

In one part of this work, we collaborated with the RF Laboratory at the National Institute of Science and Technology (NIST) in Boulder, CO, to accurately characterize the first part of our research of 1SXG TSV arrays fabricated on a single layer wafer (discussed in detail in Chapter 4). To make certain the VNA measurements are accurate and reliable, proper cleaning of the cable and SMA connectors of the VNA
and probe station were conducted before the measurements. Then, the off chip calibration with SOLT standard coaxial cable were performed in preparation for the on chip multi-line TRL calibration.

![Optical microscopic image of test structures. On wafer TRL calibration structures are located on the left and right columns.](image)

We used an on-wafer calibration method - the Multi-line TRL Calibration – developed by NIST[24]. The calibration structure set is composed of a Thru, Reflect by Open and Short, and multiple standard transmission lines with the same sets of test fixtures as test structures for DUT. The algorithm takes an optimal weighted average of all line measurements and renormalizes the S-parameters impedance to 50Ω. Using sets of two port measurements on various on-wafer transmission lines of multiple lengths, in addition to the base short transmission line thru and two reflection measurements, plus the switch term
measurement to calculate both forward and reverse directions, the full 12 term error model can be
determined[24]. The reference plane can be accurately moved to the DUT to remove all instrument as
well as test-fixture induced errors. To perform this on a wafer calibration structure, we included the
Multi-line TRL calibration structures in the circuit layout with our test structure design. An optical
microscope image of this structure is shown in Figure 3.13. The test structures are in middle column and
the calibration structures are in the left and right columns.

3.3.2.2 Two step calibration with LRRM and Open/Short De-embedding

We also used a two-step calibration method that utilized an LRRM calibration method with impedance
standard substrate (ISS) in association with an on-wafer, open/short de-embedding technique. The ISS
consists of calibration standards that have been laser-trimmed to precision tolerances within 0.3% of the
nominal values. A full set of calibration standards are provided by ISS including TRL, SOLT, and LRRM
techniques. The LRRM calibration algorithm is available in WinCal the software developed by Cascade
microtech Calibration research. In practice the LRRM will provide more consistent calibration since it
uses an auto-load inductance algorithm rendering it less sensitive to variations of probe placement, probes
and standards that may occur.

After the off wafer LRRM calibration, the reference plane is moved to the GSG RF probe tips. The
second step is removing effects from the test fixture components. These include the CPW probe pads and
the CPW lines connected to the TSV[25]. To conduct the second de-embedding step, we need to first
measure the S-parameters for the DUT, Open and Short structures. Figure 3.14 shows the process of
matrix manipulation for mathematical extrapolation to determine the DUT S-parameters[26].
Figure 3.14 Equivalent models of the test structures for Open/Short de-embedding technique

All three S-parameters matrices are first converted to Y parameters using an S to Y matrix conversion [27].

The open Y parameter represents the capacitance component of the test fixtures (including the capacitance of the pad and CPW lines and the crosstalk capacitance between two ports). Therefore, both DUT and Short results should subtract the Open Y parameter to remove the parasitic admittance:

\[
[Y'_{DUT}] = [Y_{DUT}] - [Y_{OPEN}]
\]  
\[ (3.33) \]

\[
[Y'_{SHORT}] = [Y_{SHORT}] - [Y_{OPEN}]
\]  
\[ (3.34) \]

The Short measurement provides the parasitic resistance component from the test fixtures that are easier manipulated in a Z parameter format. Therefore, \([Y'_{DUT}]\) and \([Y'_{SHORT}]\) are converted to Z parameters using
a Y to Z conversion approach[27]. The Short’ Z parameter is subtracted from the DUT’ Z parameter to remove the series parasitic resistance:

\[ [Z''_{\text{DUT}}] = [Z'_{\text{DUT}}] - [Z'_{\text{SHORT}}] \]  

(3.35)

Then the DUT’’ Z parameters are converted back to S-parameters for the final de-embedded S-parameters of the DUT[27].

References


CHAPTER 4 High Frequency Signal Transmission with 1SXG TSV Array Configurations in a 2-tier Stacked Wafer

4.1 Introduction

In 3D heterogeneous ICs, TSVs are used to transmit various types of signals including digital, analog, and RF signals between functional dies such as MEMS, sensor, RF antenna etc. in the 3D stack system[1]–[3]. Substantial research has been reported on electrical characterization and simulation of TSVs performance for DC and high frequency applications up to 20GHz[4]–[10]. Most of proposed analytical models for TSVs were verified through a comparison to ANSYS HFSS full wave simulations, which are based on a electromagnetic field calculation using a finite element model [11]–[15]. However, there is a lack of experimental validation of such modeling with high frequency electrical characterization of fabricated TSVs. Such comparisons are important because the TSVs are surrounded by a semiconducting silicon substrate, which can result in high frequency signal coupling and losses. Such losses are a primary concern for signal integrity of the overall 3D system[8], [16]–[18].

In traditional high frequency signal transmission circuits, a well shielded transmission line is usually used for a low-attenuation system such as coaxial cable for long distance terminal connections, and strip-lines/micro-strip lines in planar high speed interconnections[19]. However, for 3D IC interconnects in the 3rd dimension where the interconnection must pass through the silicon substrate, a large vertical ground plane is impractical. Likewise a true, coaxial type of TSV sacrifices affordable fabrication cost due to the complex process required to achieve sufficient EM field shielding. Therefore configurations of a signal TSV surrounded by multiple ground TSVs - a coaxial-like shape - were proposed to provide both easy manufacturing and sufficient EM field shielding[9], [20]. Yu et al. reported HFSS simulations, which predicted that more ground TSVs around a single signal TSV yielded better high frequency signal transmission efficiency. They reported that a 1S4G (1 signal TSV surrounded by 4 ground TSVs) TSV array had superior high speed signal transmission efficiency compared to a 1S2G TSV array from DC to
10GHz, due to better field shielding provided by the extra two ground TSVs surrounding the signal TSV[20]. It could serve as a critical design guideline for high-speed signal channel design in 3D systems. However, this conclusion was only based on isolated TSV simulations using HFSS but without experimental validation. Moreover, for a real system the 3D channel performance depends on not only vertical TSVs but also on the planar interconnects constituting the complete signal path. Therefore, a study focused on a complete 3D path including both TSVs and planar interconnects is needed. Consequently, for the work described in this chapter, we carried out careful design of 1SXG TSV test structures and undertook accurate experimental characterization (VNA with proper calibration techniques) of fabricated 1SXG TSV test structures to verify the prediction by Yu et al[21]. In addition, a thorough research and analyses with full wave simulation and equivalent circuit modeling were performed to understand the proposed 1SXG TSV 3D channel high-speed signal transmission properties.

4.2 Via chain test structures

To enable experimental characterization for 3D high speed channels, it is necessary to have test fixtures that are composed of planar interconnects for probing as well as comprising connections to TSVs. Coplanar wave guides (CPWs) were chosen for connecting the TSVs across the front-side and back-side of a thinned silicon wafer. This test geometry was chosen since it is relatively straightforward to fabricate this structure without the need for extra metal layers. Likewise, this type of test structure displayed good compatibility with RF probes for testing purposes. Test structures comprised of dual TSV chains with backside CPW connections were used to characterize high frequency signal transmission properties of 1SXG TSV array configurations.

4.2.1 Layout and schematics

For RF characterization of 1SXG TSV arrays, using identical test fixtures for every configuration ensures comparability of the test results. Figure 4.1 shows the test structure schematics and the layout for the 1SXG TSV arrays. Figure 4.1(a) is the cross-sectional view at the signal TSV that shows the dual TSV
dual chain test structures. For insulation from the conducting silicon substrate, a thin layer of silicon dioxide is needed between the TSV and substrate as well as between CPW metal lines and substrate and is shown in white in Figure 4.1(a). Because the thinned wafer is very fragile, a regular wafer is temporarily adhered to the backside of the TSV wafer for easy handling. As shown in Figure 4.1(b), front side CPWs provide connection to the probing pads for S-parameter measurements and backside CPWs connect two sets of 1SXG TSV arrays to form the dual chain. Figure 4.1(c) illustrates the 1S2G/4G/6G TSV configurations that were studied for this chapter with the center orange copper via comprising the signal TSV and surrounding blue vias comprising ground TSVs.

Figure 4.1 Test structure schematics in a 2-tier system. (a) is the cross-section view of dual chain test structure; (b) is the perspective view of TSV dual chain test structure (using 1S2G as an example); (c) is zoomed 1SXG TSV structures

The experimental characterization and simulation studies shown in this chapter were based on these sets of dual chain test structures.

4.2.2 SEM images

The dual TSV chain test structures were fabricated by a via-middle process technique, as discussed in Chapter 2. A top-view SEM image of an as-fabricated 1SXG TSV test structure is shown in Figure 4.2. Two sets of Ground-Signal-Ground RF probe pads were patterned and connected to 1SXG TSVs to facilitate the RF characterization described in later sections. The calibration structures are located on the
left and right sides of the TSV dual chain test structure (see Chapter 3). The GSG probe pads used in the RF measurements were 150 µm in pitch and the detailed structure geometries are shown in Figure 4.2.

![SEM image for top view of TSV dual chain test structure](image)

**Figure 4.2 SEM image for top view of TSV dual chain test structure**

![FIB cross-section SEM image of TSV dual chain test structure](image)

**Figure 4.3 FIB cross-section SEM image of TSV dual chain test structure**

To inspect the TSV chain structure with a cross sectional view, a focused ion beam (FIB) tool was used to mill the silicon substrate to reveal the detailed structure underneath the surface. Figure 4.3 shows the cross-section view of a dual chain TSV test structure from the dual beam SEM image. This cross section was taken at the signal TSV dual chain position. Some small voids are evident in the TSV cross-section.
profile shown in Figure 4.3, indicating the presence of primarily minor defects during the TSV copper electroplating process.

4.2.3 Electrical continuity measurement

As the high aspect ratio Cu via deposition process may introduce defects that form voids in a given TSV (Figure 4.3), it is critical to characterize the resistance of TSVs and confirm good connection between planar interconnects and vertical TSVs. In our study, we tested the IV response for a 60 via chain test structure resident on the front-side/backside processed (thinned) wafer. Figure 4.4 shows the aggregated (averaged) IV curves from 5 separate TSV test structure dies. Using a linear fitting, the total resistance of 60 via chain was determined to be 13.2Ω.

![Figure 4.4 IV measurement results for 60 via chains for electrical continuity confirmation](image)

Figure 4.4 IV measurement results for 60 via chains for electrical continuity confirmation

To subtract the probe and test pad contributions from the data in Figure 4.4, dual via chain structures were tested and compared. With respective calculations for the planar interconnects, the DC resistance of representative 5.5 μm diameter/50 μm high TSVs was extracted and found to be approximately 70 mΩ - very close to the analytical result expected for this TSV geometry. Thus, it was confirmed that the electrical continuity for Cu TSV via chains conformed to that expected for densely filled TSVs, which ensured the feasibility of further investigations for high frequency characterization.
4.3 Experimental results – compare with prior predictions

An Agilent vector network analyzer (VNA) was utilized for S-parameter characterization for the aforementioned TSV test structures for a frequency range from 100MHz to 50GHz. We measured the test structures with a probe station and the VNA to determine the signal transmission coefficient $S_{21}$ and reflection coefficient $S_{11}$, which represent insertion loss and return loss, respectively. For extracting the transmission and reflection characteristics of the TSV dual chain 1SXG test structure, the calibration of the probe pads employed the NIST multi-line through reflection line (TRL) calibration method[22]. Since all of the components in the structures are reciprocal, for all three configurations, the following S-parameters are related as follows: $S_{11}=S_{22}$ and $S_{21}=S_{12}$. Thus, we only analyze the transmission coefficient $S_{21}$ and reflection coefficient $S_{11}$ values for insertion loss and return loss in our study.

![Graph of S21 vs Frequency for 1S2G TSV array dual chain structure on different dies over the wafer](image)

Figure 4.5 Test reproducibility validation with 1S2G TSV array dual chain structure on different dies over the wafer

Following raw data correction utilizing the TRL calibration process, the frequency dependence of the transmission coefficient, $S_{21}$, of 1S2G test structures on 5 dies was determined and is shown in Figure 4.5. The repeatable results of the S-parameter data in the figure demonstrated the reliability of our measurements. The minor differences between dies were due to process variances across the wafer. The insertion loss, $S_{21}$, of all 1S2G structures exhibited a similar degradation rate of about -0.1dB/10GHz with frequencies above 1GHz. For the reflection coefficient, $S_{11}$, the high degree of similarity between curves
from 5 different dies indicates the reproducibility of the measurements. The small oscillations evident in both plots resulted from non-ideal probe contacts on possibly partially oxidized copper pads. Measuring environment noises and uncertainties likewise played a role. This can be limited by averaging all results from 5 dies, as shown in Figure 4.6.

![Graph showing S-parameters for 1SXG TSV array dual chain structures comparison](image)

Figure 4.6 Statistical averaged S-parameters for 1SXG TSV array dual chain structures comparison

The statistical average values (with standard deviation error bars) for all three structures are shown in Figure 4.6. All three TSV structures exhibited low insertion losses that were less than -1dB at 50GHz. These results show that the proposed 1SXG TSV with CPW configurations may be very attractive as 3D interconnect components for high-speed signal transmission. The 1S2G structure exhibited the lowest insertion loss with 0.2dB lower than that of 1S4G and 1S6G from 5GHz to 50GHz. The 1S4G and 1S6G structures have almost the same transmission performance. These results also exhibit a decreasing slope of insertion loss with frequency. This loss was steeper at low frequency (less than 1GHz).

The signal reflection of all three TSV structures increased with higher frequency. The 1S4G test structure exhibited slightly lower but very similar reflection with respect to the 1S6G TSV, which was -17dB at 50GHz. $S_{11}$ of 1S4G and 1S6G TSV channels was increasing faster than that of 1S2G. The 1S2G exhibited about 4-5dB lower return loss for frequencies exceeding 10GHz. All three configurations
exhibited low return loss up to 50GHz, which proves 1SXG structures are promising interconnect components for high-speed 3D IC signal transmission.

Interestingly, the experimental characterization results from our fabricated 1SXG TSV test structures showed the inverse trend compared with previous prediction by Yu et al. As Yu et al performed a simulation and predicted that more ground TSVs surrounding a signal TSV yields a better signal transmission and lower insertion and return loss over the whole frequency range up to 10GHz, as shown in Figure 4.7[20]. They predicted that, compared to a 1S2G TSV array, the 1S4G TSV array introduces lower loss because of the better EM field shielding from extra ground TSVs. This prediction was based on a full-wave simulation of isolated 1SXG TSV structures. It is important to note that Yu et al. did not include any connectivity structures (in-plane CPWs or planar connections to probe pads) in their full-wave analyses of 1SXG TSV structures.

![Figure 4.7 Isolated TSV full wave simulation results predicted by Yu et al: 1S4G TSV array has lower signal insertion loss and return loss compared to 1S2G TSV array.[20]](image)

To understand the disagreement between our experimental results and Yu’s full wave simulation prediction, further modeling and simulation investigation was needed. In the following sections, we present thorough analyses using both full wave simulation and lumped circuit element modeling to investigate and document the high frequency signal transmission characteristics of 3D channel
incorporating 1SXG TSV arrays for comparison with our experimental measurements and the simulation results of Yu and coworkers.

4.4 Modeling study

4.4.1 Full wave simulation for CPW+TSV test structure

ANSYS HFSS was used for full wave simulation of the aforementioned single-tier TSV test structure[23]. The geometric model for our single-tier TSV test structure was built in the HFSS 3D modeler with all geometry parameters identical to the fabricated test structure regarding the specific via-middle process used for fabrication. For the material parameter settings, the silicon substrate conductivity was set to 10S/m and dielectric loss tangent was set to 0.0015. These values were both consistent with the estimated values for Si wafers used for TSV test structure fabrication. For the dielectric insulation layer, we set the silicon dioxide’s relative permittivity at 4. Figure 4.8 shows an example of the 3D model for the 1S2G TSV array dual chain test vehicle at CNSE. The simulation was performed on the entire test structure including the two sets of GSG RF probe pads. To extract the TSV dual chain results for comparison to experimental data, we used the de-embedding post simulation function in HFSS to de-embed the reference planes to the TSV positions. This is very similar to the de-embedding step described in the experimental characterization section in Chapter 3.

Boundary conditions for the ‘air box’ that cover the test vehicle in the model were set as radiation, which corresponds to the real world condition when the test was performed. In the experiment, the signals were transmitted to the TSV test structures from the GSG probe pads. To mimic the same signal source for the simulations, two excitation CPW wave ports were set on the 2D vertical surfaces at the CPW pads as shown in Figure 4.9.
Figure 4.8 HFSS simulation model for TSV+CPW 3D test structure

Figure 4.9 Electric field distribution on CPW wave port at the GSG probe pad

Figure 4.9 shows the electric field distribution on the excitation CPW port for our simulation of the 1S2G test structure. The color grade represents the electric field intensity from 0 to 7.6E6 V/m. The highest electric field was located at the space between the CPW signal and ground traces. The fringing fields extended up to the ‘air box’ and down into the insulation layer and silicon substrate. The CPW wave ports were set up using HFSS wave port standards to generate the correct port-excitation EM field entering the 3D model to maximize the accuracy of the simulation[23].
The same simulation setup and CPW test fixtures used for the 1S2G TSV array test structure were applied to the 1S4G and 1S6G TSV array dual chains for a fair comparison on the electrical characteristics between 1SXG TSV configurations.

### 4.4.2 Simulation with Lumped element circuit model

Lumped element circuit modeling was also utilized for simulation of 1SXG TSV test structures. Using the lumped circuit models for TSV and RDL, as described in Chapter 3.2, we performed equivalent circuit simulation for the TSV dual chain structure as shown in Figure 4.10. The TSV model was based on an S/G TSV pair model with a proper modification of circuit element parameters such as capacitances $C_{ox}$, $C_{Si}$ due to the additional ground TSVs placed around the signal TSV. The model parameters were optimized by direct comparison of the calculated S-parameter values with the experimentally measured data using a least error function. This is discussed in detail in Chapter 5.

![Circuit model simulation diagram based on lumped circuit models in chapter 3.2](image)

Agilent Advanced Design Systems (ADS) from Keysight Technologies – an electronic design automation software suite for RF, microwave and high-speed digital applications – was used to simulate the electrical characteristics of the 3D channels over a wide frequency range. To simulate the S-parameters for the TSV dual chain model, two ports were connected to the via chain model for input and output of signal. Both ports were set to 50Ω impedance as standard. The S-parameter simulation module was set up and a
frequency sweep from 100MHz to 50GHz was assigned, in correspondence with experimental tests and full wave simulations. The circuit model simulation results are shown in later sections in comparison with experimental measurements and full wave simulation results.

### 4.4.3 Comparison between measurement and simulation

To compare the simulation versus experimental results, 1S2G TSV dual chain transmission and reflection coefficients, $S_{21}$ and $S_{11}$, are plotted over a frequency of 100MHz to 50GHz in Figure 4.11. The good overall agreement between the experimental results and the simulation results from the full wave simulator and lumped circuit models validated the models used and the simulation accuracy. For the insertion loss, $S_{21}$, the full wave model exhibited excellent consistency with the lumped circuit model. There was a small discrepancy between the experimental result and the simulation result (less than 0.1dB over the entail frequency range), which was attributed to the difference between the actual as-fabricated geometric parameters and material properties versus the ideal settings used in the simulations. For the return loss, $S_{11}$, the excellent agreement between the experimental data and the full wave simulation indicates the accuracy of the wave port settings utilized for the HFSS model.

![Graph Comparison between measurement and simulation with full wave and circuit model for 1S2G TSV dual chain signal transmission and reflection S-parameter characteristics](image)

Figure 4.11 Comparison between measurement and simulation with full wave and circuit model for 1S2G TSV dual chain signal transmission and reflection S-parameter characteristics
The difference between the lumped circuit model and the experimental results is less than 10dB for frequencies over 20GHz, which was a relatively small amount when converted to magnitude of power loss. The slight difference between the two is acceptable, but is indicative of some limitations of the lumped circuit models.

Figure 4.12 Results show good agreement between full wave simulation and measurement results for 1SXG TSV dual chains’ S-parameters.

For all three 1SXG TSV array configurations, the full wave simulation results displayed excellent agreement with experimental characterization results, as shown in Figure 4.12. Despite small discrepancies, the overall frequency dependent insertion loss and return loss trends and the relative order between the loss magnitudes (at a given frequency) between the three 1SXG TSV configurations were very compatible with the experimental results. The insertion loss, $S_{21}$, exhibited an increase of about 0.1dB per decade from 1GHz to 50GHz for all three 1SXG TSV array dual chains. At frequencies under 10GHz, the return loss of 1S4G TSV arrays was similar to that of 1S2G TSV arrays. And at higher frequencies (over 20GHz) the value of $S_{11}$ for 1S4G TSV arrays was closer to that determined for 1S6G TSV arrays. Both experiment and simulation results indicate that 1S2G TSV array configurations suffered less loss compared with 1S4G and 1S6G TSV array configurations for signals over the full frequency spectrum ranging from 100MHz to 50GHz.
These full wave simulation results were consistent with our single-tier TSV test structure measurement data. These data show, clearly, that adding more ground TSVs worsened signal transmission performance for a 3D-TSV channel. This DIRECTLY CONTRADICTS Yu’s simulation results and predictions. Our experimental results, validated by our full wave simulation setup, provides a reasonable level of confidence that HFSS can be used to explore the EM field inside the structure so that we may understand the physics behind our results to elucidate the origin of the discrepancy between our data and Yu’s predictions. This will be discussed in detail in the next sections.

4.4.4 Limitations of full wave simulation with isolated TSV

To explore the disagreement between our measurement and simulation results and Yu’s results, we first need to reproduce their results with their simulation settings. Using the same settings as reported, we reproduced Yu’s full wave simulation results with isolated TSV structures. This is shown in Figure 4.13(a). Similar to their work, we set wave ports on the top and bottom surfaces of the signal TSV, as shown in Figure 4.13(b). Given the geometry of their models, we obtained the same results that the 1S4G TSV array exhibits lower insertion loss compared to 1S2G TSV arrays. The magnitude is around -4dB at 10GHz, which was much larger than the magnitude measured for our test structures. We attribute this quantitative difference to the geometrical differences in TSV size (TSVs modeled in Yu’s work have a diameter of 150 µm and length of 300 µm compared to 5.5 µm diameter and 50 µm length of TSVs considered here). The larger TSV dimensions definitely induce higher signal attenuation and, hence, higher loss. With these port settings we come to the same conclusion as Yu and coworkers that additional ground TSVs placed around a signal TSV provides better high frequency signal transmission.

However, upon further investigation with isolated TSV simulations, we found that the port size severely affected the S-parameter results. With the same geometric model, we varied the port size to determine its impact on the S-parameter simulation results. Figure 4.14 shows the port size impact on insertion loss $S_{21}$. Setting the circular wave port to sizes of 1.05x, 1.2x, and 1.6x of the TSV diameter, the simulation results revealed large discrepancies over the full frequency range (see Figure 4.14).
Figure 4.13 Reproduce Yu’s simulation results: (a) is transmission insertion loss $S_{21}$ (b) is the simulation models for 1S2G and 1S4G.

Figure 4.14 Port size impact on S-parameter results for signals from DC to 10GHz

The impact of the HFSS port size parameter on Yu’s simulation approach was more obvious at higher frequencies. At 10GHz, we varied the port size from 151 $\mu$m to 240 $\mu$m. As shown in Figure 4.15, the simulated insertion loss varied by more than 110%. This observation indicated clearly that the isolated TSV simulation result is very sensitive to the port size setting.
Further sensitivity studies were performed utilizing these simulations. The sensitivity parameter analysis entails calculating the first and second derivative of the insertion loss, $S_{21}$, with respect to the port size, as shown in Equation 4.1-4.2. The first order sensitivity is $8.85e4$ and the second order sensitivity is $1.58e10$. Figure 4.16 shows the sensitivity trend from the calculation. The larger port size had a more dramatic impact on $S_{21}$.

$$s^r_{S_{21}} = \frac{\partial S_{21}}{\partial r} \quad (4.1)$$

$$s^r_{S_{21}} = \frac{\partial^2 S_{21}}{\partial r^2} \quad (4.1)$$
Because the TSVs used in our study possessed a smaller diameter of 5.5 µm and a shorter length of 50 µm compared with Yu’s study of 150 µm diameter and 300 µm length TSVs, it was necessary to confirm we could obtain the same trend for our scaled geometry while using their simulation setup approach. Therefore, we performed the isolated 1SXG TSV array simulation with our TSV geometry. As shown in Figure 4.17, the simulation results yield the same relative trends – the 1S2G TSV arrays introduced the highest loss to the signal transmission while the 1S6G TSV arrays introduced the lowest. These exhibit trends compatible to Yu’s results. It is worth noting that the magnitudes of the differences between the 1SXG TSV arrays are much smaller due to its scaled geometry.

![Figure 4.17 Isolated TSV simulation results for 1SXG TSV structures in this study that are consistent with Yu’s prior prediction](image)

In summary, the isolated 1SXG TSV array simulations presented by Yu et al. are not able to represent realistic signal transmission performance for a true 3D channel, because: 1) The true EM field distribution of input signal to the TSV cannot be set as an excitation wave port on top and bottom surface of the TSV, because the signals are not introduced from vertical sources but rather from horizontal interconnects connecting to transmitters and receivers; 2) The isolated TSV model simulated S-parameter result is extremely sensitive to the port size, which also indicates the ports’ substantial impact on simulation results. Therefore, a thorough analysis with a full 3D channel simulation is necessary to quantitatively evaluate the high-frequency signal transmission performance of the channel. In the next section, we
perform such analyses based on complete TSV dual chain simulation to better investigate the EM field and electrical parameters associated with the TSV test structure in order to understand our observed experimental results.

4.5 Discussion

4.5.1 Investigation of electric field and signal transmission efficiency

To better understand the impact of the number of ground TSV on signal transmission, HFSS simulations were employed to investigate the details of the EM field shielding (confinement) resulting from the presence of ground TSVs placed around the signal TSV. The good agreement between the simulation and measurement results shown in Figure 4.12 supports and provides confidence for the use of our simulation analyses to investigate the EM field distributions in the test structures.

4.5.1.1 Electric field distribution around 1SXG TSV array

HFSS can store the spatial EM field information at working frequencies when solving Maxwell equations inside the finite element mesh representing the TSV test structure geometry. The stored EM field data can be shown in the model results by using a post simulation process. Figure 4.18 shows the contour plots of electric field at a working frequency of 10GHz on the horizontal cross section at the middle surface of various 1SXG TSV array configurations. The electric field intensity is presented in color scale in the figure. Single signal TSV (1S) and 1S1G TSV configuration were added to our simulation investigation to extend and complement the electric field study on 1SXG TSV configurations. As illustrated in the figure, the 1S TSV configuration exhibited the highest intensity electric field penetration into the silicon substrate, i.e. poor shielding. With one ground TSV, the 1S1G TSV configuration possessed lower field penetration and should exhibit less energy dissipation associated with the substrate conductivity. This trend continued for 1S2G and 1S6G TSV configuration (i.e. less field penetration into the silicon substrate). The 1S6G configuration exhibited the best confinement (in terms of a given E-field contour line). On 1S6G plot, the black circles around the signal TSV are surfaces for EM power flow integration into the next section. These field contour plots qualitatively confirmed the field confinement associated
with the 1SXG TSV arrays, i.e. that additional ground TSVs placed around the signal TSV actually provide better signal TSV electric field confinement. A more detailed quantitative comparison will be discussed in the next section with EM power flow calculations.

Figure 4.18 Electric field contour plots for 1SXG TSV configurations at middle point of TSV. The circles on plot 1S6G TSV configuration are representing the integration surface for EM power calculation.

4.5.1.2 Comparison of EM power flow

Improved signal transmission in interconnects denotes a greater fraction of incident power transmitted from one port to another port through the channel (interconnect). From Poynting’s theorem, the energy in an EM field is conserved, as presented in Equation 4.3[24].

\[ P_s = P_o + P_i + 2j\omega(W_m - W_r) \]  

(4.3)

The complex power conservation equation states that the power delivered by the source (\( P_s \)) is equal to the sum of the power transmitted through the surface (\( P_o \)), the power lost to heat in the volume (\( P_i \)), and \( 2\omega \) times the net reactive energy stored in the volume. Since we use the same test structure and source for all TSV configurations studied, a power loss comparison can be obtained by comparing the transmitted power through integration of the real part of the Poynting vector for a given cross sectional area. The Poynting vector is the cross product of the electric field and magnetic field. For a quantitative comparison,
we integrate the real component of the Poynting vector normal to the surface, within a series of concentric circles around the signal TSV using Equation 4.4:

\[
P_{oi} = \frac{1}{2} \int E \times H^* \cdot ds = \frac{1}{2} \int S \cdot ds
\]  

(4.4)

Where \( P_{oi} \) is the transmitted power over circle ‘i’ and \( S_i \) is the area of circle ‘i’.

To integrate the power flow, HFSS post simulation processes were employed to investigate the details of the electric field shielding (confinement) resulting from the presence of ground TSVs. HFSS post simulation processing allowed us to calculate the EM field along a line, area or volume to understand the details inside the FEM calculation results over the TSV channel test structures[25]. While building a geometric structure in the HFSS simulation 3D modeler, several circle sheets at the middle surface of signal TSV were used for integration of EM fields. After meshing and calculation across the entire 3D geometry, the field solution data was saved at the working frequency (10GHz in this study). Selecting the HFSS Field calculator activated the parameter-selection panel shown in Figure 4.19.
To integrate Poynting vector over circles, the following steps were used:

Quantity -> Poynting (The integration value is Poynting vector.)

Complex -> Real (Real part is used and the unneeded imaginary component is discarded.)

Geometry -> Surface -> Circle I (The integration surfaces needs to be set up before the simulation.)

Normal (Dot product of the vector data with the normal to the circle surfaces.)

∫ (Integrate over the circle surface)

Eval (Final value will be calculated.)

Figure 4.20 Calculated transmitted EM power around signal TSV for various 1SXG TSV configurations

Figure 4.20 shows the calculated transmitted power $P_{\text{trans}}$ for various 1SXG configurations versus integration area radius. The steep increase of transmitted power at smaller radius with increased number of ground TSVs simply reflected the higher intensity electric field around the signal TSV as shown in Figure 4.18. The flat region of the power flow curves for radii > 12µm, at the edge of ground TSV, indicated effective shielding by ground TSVs. The results verified the prediction that a 1SXG TSV configuration with more ground TSVs provides better electromagnetic field shielding. However, this does
not necessarily imply that better EM field confinement provides better signal transmission for 3D path, as discussed below.

During the simulation study, we found that the electromagnetic field intensity over the volume was not only related to the ground TSV number and location, but was also related to the substrate material properties. In our study, the substrate material is conducting silicon. Therefore, detailed analyses on the substrate conductivity could also provide critical information for the high-speed interconnect design.

Circuits for high frequency applications are typically fabricated with high resistive silicon substrates, which are generally more expensive than low resistive silicon substrates. Thus, the investigation of substrate conductivity can provide guidance for cost effective design for 3D high bandwidth interconnects.

We investigated the EM confinement for 1S2G TSV configurations for silicon substrate conductivities of 0, 5, 10, and 20 S/m. For the HFSS simulation, we added integration circles of 15µm radius at three Z-axis positions, which were at +20 µm, middle point 0µm, and -20 µm, to trace the power flow through TSVs in the vertical direction.

Figure 4.21 Power flow calculation with vertical location for 1S2G TSV on different resistive substrate
The results shown in Figure 4.21 implied that signal power attenuated gradually following the signal propagation direction. The input power from the port is 1 Watt. With an insulator substrate, the power loss through the TSV was lowest, which varied from 93% at 20 µm near the top of TSV to 78% near the bottom of the TSV. With conductivity of 5S/m, 10S/m, 20S/m silicon, the signal power confined close to the signal TSV was lower with higher conductive substrate and attenuated even more throughout the TSV transmission. Therefore, as expected, a high resistive silicon substrate is preferred for high frequency signal transmission in a heterogeneous 3D stacked system.

4.5.2 Impedance match of 1SXG 3D channel

With the confirmation of EM field-shielding benefits from the extra number of ground TSVs in a 1SXG TSV structure, we further explored other factors that might impact the signal transmission performance and explain the seemingly contradictory experimental observations presented for our single-tier 1SXG TSV test structures. The transmitted power delivered to the load depends on the reflection coefficient $\Gamma$, which characterizes the impedance mismatch for the system[26].

$$P_{av} = \frac{1}{2} \left| \frac{V_{inc}}{Z_0} \right|^2 \left( 1 - |\Gamma|^2 \right) \quad (4.5)$$

$$\Gamma = \frac{Z_{1SXG} - Z_0}{Z_{1SXG} + Z_0} \quad (4.6)$$

Where $Z_{1SXG}$ is the impedance of the 1SXG TSV configurations and $Z_0$ is the characteristic impedance of the system, which is 50 Ω.

Since our 1SXG TSV test structures included not only TSVs but also CPWs, the impedance matching between the 2D planar CPW and the 3D TSV configurations in the system needs to be evaluated. The degree of impedance matching determines the performance of the circuit’s overall transmission properties, i.e., better matching between the TSVs and the planar CPW yields greater transmission. Using the HFSS time domain analysis simulator, we compared the time domain reflectometer (TDR) impedance of the 1SXG TSV array structures as shown in Figure 4.22. The TDR impedance plot over time scale was
derived from the time domain voltage response of a fast step wave with a rise time of 20ps. The relations between the curves in the plots agreed with the transmission and reflection S-parameter results shown in Section 3.4.3. The 1SXG structures presented the same trend in the degree of impedance mismatch, where the 1S2G TSV test structure, which exhibited the best signal transmission, possessed the closest impedance to the system impedance of 50 Ω.

![Graph showing time domain impedance for 1SXG TSV array configuration](image)

Figure 4.22 Time domain impedance for 1SXG TSV array configuration indicates adding ground TSVs reduces the impedance so as increases impedance mismatch to reference impedance.

Equation 4.7 shows the calculation expression for impedance in the transmission line model. Although, our 1SXG TSV model does not correspond precisely to a transmission line model it can be represented by similar equivalent circuit models as shown in Chapter 3. With proper approximation and simplification, the simple transmission line model provided the intrinsic physics and electrical insights of the whole structure as a model.

\[
Z_{\text{1SXG}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{4.7}
\]

Where R, L, C, G are the resistance, inductance, capacitance and conductance of the device. Capacitance is inversely proportional to impedance. Larger capacitance introduces lower impedance at high frequency. The negative dips of the impedance in Figure 22 indicate the capacitive behavior of the components. Data
for the 1S6G TSV test structure exhibited the lowest dip, which indicated it had the highest capacitance. Thus we extended our investigation to include 1SXG TSV array capacitance analyses to compare with the previous analysis of EM field confinement. These results are presented in the next section.

4.5.3 Capacitance analyses of 1SXG TSV configurations

4.5.3.1 Analytical analyses

Because of the silicon substrate’s semiconducting characteristics, the capacitance of each configuration is composed of the total TSV insulation oxide layer capacitance ($C_{ox}$) in series with the total coupling capacitance between signal and ground TSVs ($C_{Si}$), as presented in the following Equation 4.8:

$$\frac{1}{C_{[1SXG]}} = \sum_i \frac{1}{C_{ox,i}} + \sum_j \frac{1}{C_{si,j}}$$  (4.8)

The capacitance of the insulation oxide layer was modeled as a coaxial cable capacitance of inner radius of copper via and outer radius of oxide liner as shown in Equation 3.18 in Chapter 3.2.

Figure 4.23 Equivalent capacitance models for 1SXG TSV array configurations

For the coupling capacitance between the ground and signal TSVs, an analytical expression is unavailable because of the overlapping coupling between the signal TSV and the ground TSVs as well as the complex fringing electric field distribution at the top and bottom regions of TSVs. The sum operator in Equation 4.8 denotes the equivalent total capacitance contributed from the TSVs’ oxide layer and the ground to the signal TSV coupling. The equivalent circuit models for the 1SXG TSV arrays are shown in Figure 4.23.
Since an analytical method for this calculation is not available, detailed capacitance values can be obtained by numerical calculation using a finite element modeling method as discussed in the following subsections.

### 4.5.3.2 Finite element method simulation with COMSOL

In this section, we employed COMSOL Multiphysics to numerically calculate the capacitance of 1SXG TSV array capacitance. COMSOL Multiphysics is a finite element analysis simulation software suite for modeling and simulating various physics problems such as electrical, mechanical, fluid flow, chemical applications etc.[27]. AC/DC and electrostatic modules with were used in our study for calculating the total capacitance of the 1SXG TSV configurations.

![Generated finite element meshes for capacitance calculation in COMSOL](image)

Figure 4.24 Generated finite element meshes for capacitance calculation in COMSOL.

The simulation software used advanced numerical techniques to calculate the electric field of each individual mesh element to find approximate solutions to converge at the boundary conditions. For the COMSOL finite element analysis, the silicon substrate was modeled as a wide cylinder that was large enough to cover the fringe field around the TSV. Knowing that the electric field degrades rapidly as inversely proportional to square of the distance from the conductor, the electric field intensity at the boundary of the model geometry was omitted due to its low value. Figure 4.24 shows the automatically generated meshes for the 1S2G TSV array configuration. The critical calculation regions immediately adjacent to the TSVs were meshed to finer element size to increase the calculation accuracy.
For the COMSOL finite element modeling setup (upon building the geometrical model of 1SXG TSV configuration) a set of material selections, such as copper vias and oxide liners, were created to set the material information before assigning the physics principles. The silicon permittivity used was 11.9 and the conductivity used was 10S/m. The silicon dioxide permittivity was 4.0 while the conductance of the copper was 58M S/m. All material properties were the same as those for the full wave HFSS simulation and corresponded to values measured from the materials used for fabrication. Figure 4.25 shows the geometric models for the 1SXG TSV array capacitance simulations carried out in COMSOL.

![Image of 1SXG TSV array models used in COMSOL](image)

Figure 4.25 1SXG TSV array models used to calculate capacitance in COMSOL

For boundary conditions, the signal TSV surface was set to 1V for easier post simulation calculation and the ground TSV surfaces were set to 0V. After meshing and calculation, the surface charge densities on
every geometry surface were calculated. The total electric charge quantity, \( Q \), was calculated by integrating the surface charge on the signal TSV, as shown in Equation 4.9.

\[
Q = \int \sigma_q(r) dS
\]  

(4.9)

The capacitance is equal to the holding electric charge quantity per unit voltage difference between the two terminals, as shown in Equation 4.10.

\[
C = \frac{Q}{V}
\]  

(4.10)

Thus the calculated electric charge value is numerically the same as the capacitance of the TSV configuration. The calculated total capacitance results for the 1SxG comparison are shown in Figure 4.26. Results show that the 1S6G TSV array structure exhibited the highest capacitance of 18.2\( \text{fF} \), and the 1S2G TSV array structure exhibited the lowest capacitance of 14.6\( \text{fF} \). Since the two capacitances are in series, the total capacitance of the 1SxG TSV array is dominated by the smaller coupling capacitance. More ground TSVs introduce more coupling capacitance, therefore decreasing the impedance of the 1SxG TSV interconnect. Therefore, the higher capacitance induced by additional ground TSV in the 1S4G and 1S6G TSV arrays induced higher impedance mismatch resulted in a poor trade-off for the better EM field confinement obtained with additional ground TSVs. As a result, 1S2G TSV dual chain test structure showed superior high-speed signal transmission compared to 1S4G and 1S6G TSV configurations since it had the optimal trade off of capacitance versus EM field confinement. We conclude that accurately characterizing both the capacitive and EM-confinement aspects of the 1SxG test structures - as well as utilizing realistic port settings for full-wave simulations – is essential for accurate predictive modeling of the full 1SxG+CPW TSV test structure.
4.6 Conclusions

In this chapter – to experimentally verify previous literature predictions of the positive performance impacts of additional ground TSVs in providing better high frequency signal transmission performance in 3D system due to better EM shielding – 1SXG TSV array dual chain test structures were fabricated and experimentally characterized to evaluate the performance impact of ground TSV configuration on high frequency, 3D signal transmission. Multi-line TRL calibration and de-embedding techniques were utilized to ensure characterization accuracy. However, in contradiction with previous literature predictions of Yu and coworkers, the experimental results showed that TSV array configurations with fewer ground TSVs (i.e. 1S2G) suffered less signal loss while TSV array configurations with additional ground TSVs (i.e. 1S6G) showed the highest signal loss. Full wave EM simulations with HFSS and equivalent circuit model simulations were conducted on the 1SXG TSV structures of interest and exhibited good agreement with measurement results and enabled a better physical understanding of the observed results. To understand and explore the underlying reasons for the difference from our experimental 1SXG results and previously published predictions, an investigation using a full wave simulation was carried out. Firstly, realistic port settings were used – unlike the unrealistic port settings employed by Yu et al. set directly on top and bottom of TSVs. For our studies the wave ports were more accurately placed on the planar interconnect.
cross sections since the signal originated from on-chip transmitters in the 3D signal system. Secondly, we found that the isolated TSV simulation results were very sensitive to port settings, which were unfortunately neglected in Yu’s simulation-based research on TSV in 3D ICs. Our detailed, full-structure simulation investigation on the electromagnetic field confirmed the ground TSVs’ shielding benefits as predicted. However, the higher capacitance from extra ground TSVs induced an impedance mismatch trade off with the EM field shielding benefits. Therefore, adding ground TSVs around signal TSV doesn’t necessarily improve high-speed signal transmission in a 3D system. Proper interconnect design needs to considered to take account of this tradeoff between ground TSV capacitance induced impedance change and its EM shielding effect. Fewer ground TSVs are preferred considering that both 3D channel transmission efficiency and die area consumption are key design parameters for 3D ICs.

References


CHAPTER 5 High Frequency Signal Transmission in a Multi-layer Stacked 3D System

5.1 Introduction

In a 3D heterogeneous system, a multi-layer stacked wafer is used to improve and expand chip performance, extend miniaturization through footprint reduction, and reduce power consumption[1]–[3]. In a multi-layer stacked, heterogeneous system, various signals including digital, analog and RF etc. are transmitted through the stacked structures within 3D channels composed of TSVs, RDLs and die joints[4]–[6]. To connect stacked dies, many bonding approaches have been utilized, including wire bonding, micro-bump, and direct Cu-Cu bonding[7]–[9]. For the work presented here, a direct Cu-Cu thermo compression bonding technique was used to fabricate the 3D multi-layer stacked test structures. Most of high frequency signal transmission analyses for multi-layer stacked 3D systems have been directly extrapolated from single layer TSV performance by cascading various signal transmission models[10]–[12]. However, this simple cascading approach neglects the physical environment differences (and, thus, electrical parameter differences) induced by stacking more silicon dies. To the best of our knowledge, there is no systematic characterization and analysis on high-speed (RF) signal transmission in a multi-layer stacked 3D IC system using TSVs. This chapter addresses this gap by high-frequency signal characterization and accurate modeling of high-frequency signal transmission in TSV-based 3D IC channels for a more complete understanding of signal transmission in a multi-layer stacked system.

In the last chapter, the characteristics of 1SXG TSV channels with top and bottom CPW connections in a single layer stack were analyzed. Simulation and characterization results indicated that fewer ground TSVs surrounding a signal TSV was a preferred geometry for high frequency signal transmission due to the ground TSV’s capacitance tradeoff with the EM shielding effect. Therefore, in this chapter, the analyses for 3D channels in a multi-layer stack were based on a standard signal/ground TSV pair. With a fabricated 3-tier stacked wafer, we characterized S-parameters for various test structures on a 2-tier or 3-
tier stack to investigate the influences from substrate resistivity, RDL length, stacking and the presence of Cu bonding pads. The proposed 3D, 3-tier test structures were fabricated and characterized for S-parameters to investigate these critical impacts on high-speed signal transmission on multi-layer 3D channels. In addition, we formulated optimized equivalent circuit models for key 3D channel components using a least square error function algorithm and successfully validated them with multiple distinct 3D IC test structures. Comprehensive analyses with validated circuit models provided critical insights and guidance to key component design for a 3D channel in a stacked system.

5.2 Test structures in a multi-layer stacked system

5.2.1 Layout and schematics

To investigate high-speed signal transmission in 3D channels in a multi-stacked system, test structures must represent typical configurations of 3D channels in a real stacked wafer system wherein functional dies at different locations of different tiers are connected by various channel configurations with different horizontal and vertical routings. Therefore experimental characterization and elucidation of the impacts of various design parameters on the signal transmission of a channel is necessary for optimized 3D routing and design. In this study, several groups of controlled comparison test structures were designed to investigate the impact factors on signal transmission performance of a 3D channel in a multi-layer stacked system.

In a 3D channel through a multi-layer stacked system, there are three key components: TSV, RDL and bond pad. To systematically characterize and compare the impact of these components on a channel, we designed various TSV chain structures in a 2-tier stacked system and a 3-tier stacked system, as shown in Figure 5.1. All test structures were designed with the same set of test fixtures to utilize the two-step calibration and de-embedding techniques discussed in Chapter 3.3. Figure 5.1 presents the cross-sectional view of various test structures. For a clear view, we eliminated the test fixtures in the figure associated with the probe pads and CPWs that connect with the TSVs.
Figure 5.1 Cross-sectional schematic for various TSV chain test structures in 2-tier and 3-tier stacked wafer to investigate impacting factors for signal transmission property in a multi-layer stacked system

Because the stacked dies are likely to have different floor plans for various modules, the routing RDL line is an important component for a complete 3D channel for high-speed signal transmission. In both the 2-tier stack and the 3-tier stack, TSV ‘U’ chains are structures for which signal goes straight from the top layer to the bottom layer and then back to the top layer, with a bottom layer RDL connection. The RDL’s impact can be evaluated by comparing characterization results of test structures with different RDL lengths. Both middle layer RDLs and bottom layer RDLs were designed and fabricated to have various lengths for distinct test structures. In addition, the impact of stacking was investigated (e.g. the presence of additional conductive Si as well as the various processed layers as the tier interface). Identically shaped U chain structures in 2-tier and 3-tier systems were designed and fabricated to evaluate the direct stacking
impact. Another set of test structures was designed to evaluate the insertion of RDL layers between tiers and consisted of a series 4-TSV chains with a 2-tier W chain and a 3-tier V chain (Figure 5.1). The physical lengths of both 4-TSV channels are the same but the signals propagate through 2 tiers for the W chain and through 3 tiers for the V chain. The performance differences between these two structures with respect to signal transmission is expected to derive primarily from the stacking geometry. Moreover, to investigate the impact of bond pads inserted into the 3D channel of a multi-tiered structure, different bond pad sizes were inserted into 3D channels for testing and comparison.

5.2.2 SEM images

Using a Cu-Cu thermo compression bonding technique, a 3-tier stacked 3D wafer structure was fabricated in CNSE’s 3D integration process line (300mm silicon wafer fabrication flow). Figure 5.2 is a tilted angle SEM image of a 3-tier silicon stack. Tier 1 and tier 2 are thinned, 50 µm silicon wafers with TSVs fabricated with a via-middle process, while tier 0 is a regular 775 µm thick silicon wafer with back end of line (BEOL) processed layers for Cu-Cu bonding and interconnections.

Figure 5.2 Tilted angle SEM image for 3-tier stacked wafer system
Figure 5.3 is a cross-sectional SEM image of a 3-tier V chain test structure. As can be seen from the image, this test structure exhibited good die to die and die to wafer alignment and high-quality connections at the bonding pads.

Figure 5.3 Cross-section SEM image of a 3-tier V chain that shows good die to die and die to wafer alignment and connections between layers.

5.3 Experimental characterization for 3D channels in a multi-layer stacked system

RF measurements for on-chip devices are very sensitive. Accurate and reliable RF measurements rely on careful calibration and de-embedding. For the test structures discussed in this chapter, we implemented a 2-step calibration method to remove the parasitics of the connection cables and on-chip test fixtures, with details described in Chapter 3.3[13], [14]. An RF probe station and an Agilent VNA for S-parameter characterization were used to characterize RF signal transmission through various TSV chain test structures for frequencies ranging from 100MHz to 65GHz. The measurement error was under 0.1dB and is manifested as the small fluctuations in the S-parameter curves as a function of frequency.
5.3.1 Test reproducibility

Good reproducibility over different dies on the wafer was critical to establish of the accuracy of the signal transmission testing as well as validity of the resulting conclusions. The 3-tier TSV U chain structures on 5 different dies sampled from across the 3-tier stacked wafer were tested. The results are shown in Figure 5.4. The right panel of the figure also includes an inset of the test structure schematic. Insertion loss $S_{21}$ and return loss $S_{22}$ showed high repeatability for stacked dies across the 3-tier wafer stack. Sample-to-sample variation was very low (less than 0.2dB for $S_{21}$ over the entire frequency range for dies 1 to 4). A slightly larger discrepancy was observed for die 5 (green line in Figure 5.4). We attribute these differences to process and material variations. The highly repeatable frequency dependent signal loss with the 3-tier TSV U chain on different dies is a strong confirmation that these data exemplify the intrinsic signal transmission properties of this type of 3D channel structure.

![Figure 5.4 Test reproducibility validation on the same test structure on different dies over the stacked wafer](image)

Similar high repeatability was also observed on other 3-tier test structures – an important observation supporting the accuracy of analyses of the impact of the various 3D channel design elements on high-speed signal transmission. In sections presented below, to simplify the data presentation, only one set of data from repeatable die test results is plotted for each figure.
5.3.2 Substrate conductivity’s impact

Distinct from conventional high frequency transmission lines, which are surrounded by insulating materials in a package or a PCB board, 3D high-frequency signal communication channels are surrounded by the semiconducting silicon substrate. Due to this difference, the DC and RF signals are more likely to leak to the return path through the conductive substrate. Therefore, investigation of the impact of the silicon substrate conductivity on high frequency signal transmission in 3D ICs is critically necessary. Figure 5.5 shows the signal insertion loss $S_{21}$ and return loss $S_{22}$ of identical test structures - a TSV ‘U’ chain on a 2-tier stacked silicon wafer - with different substrate conductivities.

![Graph showing S-parameter characterization results for 2-tier U chain test structure fabricated on different resistive substrates](image)

Figure 5.5 S-parameter characterization results for 2-tier U chain test structure fabricated on different resistive substrates

The two sets of data represented identical test structures on high resistive silicon (HRS) and low resistive silicon (LRS) substrates with resistivity of 9~18Ω·cm and 1~2Ω·cm, respectively. There are no clear definitions for high resistive silicon and low resistive silicon for different application needs. As in this study, we used two types of substrate and the HRS/LRS denoted relative values. The U chain test structure in the HRS substrate exhibited lower signal loss of $S_{21}$ (less than -0.7dB at 65GHz) while the LRS substrate exhibited a higher signal loss of $S_{21}$ (more than -2.5dB at 65GHz). The $S_{11}$ results showed the same trends – higher reflection loss with LRS substrate. These results clearly and directly reveal the substrate conductivity’s substantial – and expected – impact on signal transmission of a 3D channel. A higher resistive silicon substrate is clearly preferred for high frequency signal transmission in a 3D
stacked system. For the data presented in later sections of this chapter HRS silicon substrates were utilized.

### 5.3.3 Stacking impact

3D channels in a multi-stacked system, depending on the connection and routing needs, can be random configurations composed of TSVs, in-plane RDLs and bond pads. Extended from 2-tier stack systems discussed in the last chapter, TSV chain structures in a 3-tier stacked system were characterized to evaluate the frequency-dependent S-parameters to investigate the impact of stacking on high-speed signal transmission. The U chain test structure in a 2-tier stack system and a 3-tier stack system were characterized and compared, as shown in Figure 5.6. For the S\textsubscript{21} parameter, the 2-tier U chain showed flatter behavior (reduced attenuation with increasing frequency) for frequencies from 10GHz to 65GHz, while the 3-tier U chain showed an approximately linear decrease at a rate of 0.27dB per decade. For both U chains, the S\textsubscript{21} phase increased linearly with frequency from 100MHz to 65GHz. The 3-tier U chain has 4 TSVs in the path while the 2-tier U chain has 2 TSVs in the path, which explains the main reason for the absolute difference of insertion loss between the two structures. However, the very large difference in the slopes of S\textsubscript{21} as a function of frequency and the more than 2x phase difference (30° for 2-tier U chain and 70° for 3-tier U chain at 65GHz) indicate that other factors associated with the stack impacted the signal transmission beyond the additional 2 TSVs.

In addition to the 2-tier/3-tier U chain comparison, a 2-tier W chain and 3-tier V chain with the same physical signal path length were designed to investigate the impact of stacking on high-frequency signal transmission in 3D channels. The 2-tier W chain can be seen as 3-tier V chain with bottom tier ‘U’ ‘flipped’ up to the top tier as illustrated in Figure 5.1 in section 5.2.1. The experimentally characterized signal transmission losses of these two configurations are shown in Figure 5.7 with the inset schematics for both structures. The signal insertion loss difference between these two structures appeared around 10GHz and increased with higher frequencies to about 0.5dB above 50GHz. And the S\textsubscript{21} phase change showed the same trend with about a 20-degree difference at 65GHz.
Figure 5.6 S-parameter characterization results for U chain structure in 2-tier and 3-tier stacked system that represent stacking impact on signal transmission property

The differences in the insertion loss and phase between these two configurations are directly related to the tier stacking. These data imply that the stack impacts are more pronounced for higher frequency signals. This experimental comparison is important for accurate modeling of the effects of stack-specific channel features, such as bond pads, and providing validated design guides for 3D high frequency signal transmission in multiple stacked wafers.

Figure 5.7 S-parameter characterization results for 2-tier W chain and 3-tier V chain that represent stacking impact on signal transmission property
5.3.4 In-plane RDL’s impact

Besides the TSVs for vertical connections, 3D channels also include in-plane components such as RDL lines forming electrical connection between different horizontal locations. To investigate the impact of the in-plane RDL components on a 3D channel in a multi-layer stack, test structures with various RDL lengths at the bottom tier and middle tier were characterized and compared.

To investigate the RDL as bottom connection, RDL connection lengths of 32µm and 64µm in TSV U chains in a 2-tier stack and a 3-tier stack were compared. Figure 5.8 shows a comparison of the $S_{21}$ magnitude and phase for various RDL lengths. The RDL length impact on a 2-tier U chain was larger than that for a 3-tier U chain. Because the total signal length of the 2-tier U chain was shorter than that of the 3-tier U chain, the impact from the same absolute length RDL was relatively higher in the 2-tier U chain. The same 10-degree difference of the $S_{21}$ phase change was due to the extra RDL line length for both cases. This confirmed a modest but significant impact of the bottom-length RDL on both 2-tier and 3-tier stack U chains.

Figure 5.8 S-parameter characterization results for 2-tier and 3-tier U chain test structures with different bottom RDL lengths for in-plane connection.

To investigate the RDL impact within a middle tier connection, 3-tier V chain test structures with middle RDL lengths of 32µm and 64µm were compared as shown in Figure 5.9 (inset schematics for respective
The magnitude of insertion loss $S_{21}$ for these two 3-tier V chain structures showed larger differences at higher frequencies, especially over 50GHz. The impact of the ‘middle’ RDL length was more substantial compared to the ‘bottom’ RDL connection length for 3-tier U chain structures. The $S_{21}$ phase change of both structures increased linearly with frequency. The phase change difference between the two structures was about 20° at 65GHz, which agreed well with the difference between the U chain structures shown in Figure 5.8. It is worth noting that the RDL length difference of the V chain structures is 64µm in total (32µm for each wing), which was twice of that of the U chains.

![Figure 5.9 S-parameter characterization results for 3-tier V chain test structures with different middle tier RDL lengths for in-plane connection.](image)

From the characterization results of various sets of test structures with different RDL lengths at the bottom and middle layers, the RDL component has a limited but measurable impact on 3D channel signal transmission. This comparison helps validate accurate modeling discussed below in Section 5.4.

### 5.3.5 Bonding pad impact

Besides RDL connections, bonding pads between adjacent tiers represent another type of in-plane connection in 3D channels. However, different from the RDL metal interconnects, the bond pads can be seen as wide and short interconnects due to the vertical signal transmission through the pads. Therefore, the resistance and inductance of the bond pad is negligible. As described in Chapter 3.2, the bond pad...
impacts are mainly capacitive in nature. Varying the bond pad size is the most effective method to investigate the bond pad impacts on signal transmission. Figure 5.10 shows the measured S-parameters for 3-tier U chain structures with various bond pad sizes. It is clear from the data in the plot that the smaller bond pad test structures suffered lower insertion loss and return loss. At frequencies lower than 5GHz, there was no obvious difference between the three test structures. The $S_{11}$ and $S_{21}$ differences induced by bond pad size increased with higher frequencies.

Figure 5.10 S-parameters characterization results for 3-tier U chain test structures with various bond pad sizes

These results are compatible with fundamental principle that the capacitive impacts on impedance and S-parameter increase with higher frequency. This implies that bond pad size should be minimized in 3D channel design. However, smaller bond pads require higher accuracy on the alignment and bonding process. Therefore, choosing a proper bond pad size needs to be considered as the tradeoff between the bond pads induced capacitance and bonding process yields in 3D high-speed channel design.

5.4 Equivalent element model simulation for 3D channels in multi-layer stacked system

5.4.1 Test structures with channel model representation

In a true 3D system, there are many more channel configurations than fabricated test structures as discussed in earlier sections. However, accurate models for general components in 3D channels can be.
extracted from test structures in this study to facilitate customized designs for 3D high-speed signal transmission channels. There are three key components in a real 3D channel: vertical connections by TSVs, horizontal interconnects by RDLs, and direct connection for adjacent dies through bond pads. As described in Chapter 3.2, each component was modeled with geometrical and physical parameters by analytical general models such as parallel plates, two wire configurations etc. Using the three models, the test structures in Figure 5.1 were represented by connected model chains shown in Figure 5.11. The TSV model is represented as a red block; the RDL line segment is represented as a green block; the bond pad is represented as a yellow block. These 3D channel models were used in circuit simulations detailed in later sections in this chapter.

Figure 5.11 3D component model representations for various TSV chain test structures in multi-layer stacked system

The models for TSV and RDL components were formulated and discussed in Chapter 3.2, as shown in Figure 5.12. The bond pad model is simply a parallel capacitance. The model-based analyses in the following sections are all based on these models.
5.4.2 Model optimization with least square error function

The equations for 3D component model parameters described in chapter 3.2 are all based on ideal physical models such as infinite length twin pair wires and coaxial cables, parallel plate capacitors etc. However, in a real 3D channel, all components are not ideal and can only be approximated through analytical equations. Therefore, the calculated results from analytical equations can only be expected to yield a reasonable range for each parameter.

For model simulations, Keysight’s Advanced Design System (ADS) was used to simulate S-parameters for over the frequency range of interest so as to be directly comparable with VNA measured results[15]. The ADS simulation package has an optimization module with different algorithms allowing designers to reach their design goals. Accurate models are critical for a reliable design and minimum cost for a design cycle. In this study, a test bench was set up to determine the optimized parameters for 3D component models. To get the most accurate circuit models for 3D components, reasonable tuning ranges were set up for model parameters (within 20% of analytical calculated values) and the simulation goal for the test
bench was set to have the minimum difference between the model simulation results and measurement results over the frequency range from 100MHz to 65GHz.

A least squares error function with a gradient search engine was applied in ADS for the optimization algorithm. The method of least squares is a standard approach in regression analysis to get the approximate solution for an over-determined system. The differences between the simulated results and the measurement results are called residuals, which are used for calculating the error and iterating simulations to reach the goal. For a least squares error function, each residual is squared and all terms are then summed. Shown in Equation 5.1, \( r_i \) is the residual and \( S \) is the sum of squared residuals.

\[
S = \sum_{i=1}^{n} r_i^2 
\]

The sum of squares is averaged over frequency. Simulations continue until the maximum number of iterations is reached or the error function (summation of the residuals) reaches a minimum (closest to the measured value). The difference between the simulated and measured test bench values vanishes or reaches a minimum when optimized[15].

For model simulations, each test structure was modeled as a cascade of 3D components as shown in Figure 5.11. Two terminals with 50Ω were connected to the 3D chain model for S-parameter simulations. In order to determine the optimized model parameters based on the least square error function algorithm, the simplest U chain structures were simulated and compared with measurement results. The 2-tier U chain was modeled as [TSV+ RDL+ TSV] and the 3-tier U chain was modeled as [TSV+ bond pad+ TSV+ bond pad+ RDL+ bond pad+ TSV+ bond pad+ TSV]. The 2-tier U chain model simulation yields optimized TSV and RDL models, which would be used in the 3-tier U chain model simulation to extract the model for the third component-bond pad. The optimized model parameters from this approach are presented in Table 5.1.
Table 5.1 Least square error function optimized model parameters

<table>
<thead>
<tr>
<th>Electric element</th>
<th>Value</th>
<th>Electric element</th>
<th>Value</th>
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<tbody>
<tr>
<td>$R_{TSV}$</td>
<td>190mΩ</td>
<td>$R_{RDL}$</td>
<td>500Ω</td>
</tr>
<tr>
<td>$L_{TSV}$</td>
<td>17.57pH</td>
<td>$L_{RDL}$</td>
<td>8pH</td>
</tr>
<tr>
<td>$C_{OX}$</td>
<td>66fF</td>
<td>$C_{RDL2Sub}$</td>
<td>10fF</td>
</tr>
<tr>
<td>$C_{Si}$</td>
<td>10fF</td>
<td>$C_{Sub}$</td>
<td>3fF</td>
</tr>
<tr>
<td>$R(G_{Si})$</td>
<td>1250Ω</td>
<td>$R(G_{Sub})$</td>
<td>2000Ω</td>
</tr>
<tr>
<td>$C_{pad}$</td>
<td>3fF</td>
<td>$C_{RDL}$</td>
<td>5fF</td>
</tr>
</tbody>
</table>

Figure 5.13 shows the comparison between the experimental measurement results and the optimized model simulation results for 2-tier and 3-tier U chain test structures. The simulation agreed very well with measurement results over the entire frequency range from 100MHz to 65GHz for both $S_{21}$ magnitude and phase. The small discrepancy for the 3-tier U chain is acceptable since the signal path and EM field is more complex through multi-layer stack system, thus making it difficult to perfectly represent the true behavior by simple circuit models. This broad agreement over multiple test structures validates the correctness of the proposed 3D component model.

In order to provide helpful guidance for future designs, these model values need to be further validated through application to other test structures. In the following section, systematic model validations were performed.
5.4.3 Systematic model validation with various test structures

TSV and RDL models were validated by applying models from the last section to other 2-tier test structures. The longer 2-tier U Chain and 2-tier W Chain test structures were simulated in ADS. The longer 2-tier U chain has 2x RDL length compared to the 2-tier U chain discussed in the last section – thus it can be modeled as [TSV+ RDL+ RDL+ TSV]. The 2-tier W chain had 4 TSVs in the chain and was modeled as [TSV+ RDL+ TSV+ RDL+ TSV+ RDL+ TSV] as shown in Figure 5.11. Figure 5.14 displays the simulated results for 2-tier longer U chain (denoted as ‘2-tier UchainL’ in the legend) showed excellent agreement with measurement results for both insertion loss magnitude and phase. Less than -0.9dB loss and phase change of about -40° at 65GHz were observed from both simulation and measurement results. The small discrepancy between simulated and measured 2-tier W chain was possibly due to RDL approximation during modeling. There were three RDL connections between 4 TSVs in the W chain: the first and third were at bottom of the silicon wafer, while the second was on the top of silicon wafer. It is clearly shown in Figure 5.1 that the surrounding dielectric material for the second top RDL line was substantially different from that of the other two bottom RDL lines. Therefore the discrepancies in magnitude and phase are acceptable considering the usage of the same RDL model for both the top and bottom of the silicon RDL connections. However, the overall good agreement...
between the measurement and simulation results on these distinct 2-tier test structures validated the TSV and RDL model accuracy.

Figure 5.14 S21 Magnitude and phase comparison between measurement and model simulation results for 2-tier long U chain with 64µm RDL connection and 2-tier W chain test structures to validate 3D component models.

In a multi-layer stacked system, another component – the bond pads – required validation with additional 3-tier test structures. Consequently the longer 3-tier U Chain and 3-tier V Chain test structures were simulated in ADS. The longer 3-tier U chain has 2x RDL length compared to the 3-tier U chain discussed in the last section. Thus, it was modeled as [TSV + bond pad + TSV + bond pad + RDL + RDL + + bond pad + TSV+ bond pad + TSV]. The 3-tier V chain is a 4 TSV chain and was modeled as [TSV + bond pad + RDL + TSV+ bond pad + RDL + bond pad + TSV + RDL + bond pad + TSV] as shown in Figure 5.11. The simulated results for these two 3-tier test structures showed excellent agreement with measurement results for both insertion loss magnitude and phase as shown in Figure 5.15. Because of its longer RDL connections, the 3-tier V chain signal loss magnitude and phase change were slightly higher than those of 3-tier longer U chain (denoted as 2-tier UchainL in the legend of Figure 5.15). Again, the excellent agreement between simulated and measured S-parameters for these structures is indicative of the 3D model accuracy. These results validated 3D component models so as to confidently provide design guidance for more complex 3D high-speed channels.
Figure 5.15 Magnitude and phase of transmission coefficient comparison between measurement and model simulation results for 3-tier long U chain with 64µm RDL bottom connection and 3-tier V chain test structures to validate 3D component models

5.5 Analyses of electrical characteristics of a high speed 3D channel

Using the proposed – and substantially accurate – model methodologies for the key 3D components, the 3D model library was established for future applicable and practical 3D system designs and circuit analyses. With the validated 3D model library, high-speed signal transmission properties of a specific signal path in any application can be analyzed. Systematical analyses on the impact of model parameters on 3D channel signal transmission integrity is then able to provide critical insights and valuable guidance to high-speed channel design for 3D ICs. Furthermore, the models and parameter impacts can be extended to and applied to evaluate other aspects of electrical performance such as signal delay and power consumption along the 3D channels. Generally, by proper floor planning for each tier’s functional modules, minimizing the horizontal connections and maximizing the vertical connections is the most beneficial way to apply 3D integration for high-speed communication (shortest interconnect length compared to 2D routing). Therefore in this section, these analyses were performed based on a 4-tier stack 3D channel (4 TSVs) with short horizontal connections.
5.5.1 TSV design

As a key component in 3D ICs, a TSV model was constructed which considered the resistance, inductance and capacitance from various contributing physical parts as shown in Figure 5.12. The equivalent elements were analyzed to provide insights and understanding of their impacts on the signal transmission over the broad frequency range.

The silicon dioxide layer between the silicon substrate and the copper via provides the critical insulation against current leakage, but also adds significant capacitance to the system. By varying the oxide capacitance in the TSV model, the simulated S-parameter results provide the oxide capacitance impact on the channel signal transmission characteristics. Shown in Figure 5.16, the insulation oxide liner capacitance mainly affects signal transmission for frequencies from 700MHz to 8GHz. A capacitance of 66fF was determined from the optimized model. In addition, a lower capacitance 46fF and a higher capacitance 86fF were also applied for simulations. The grey shaded area in Figure 5.16 indicates the frequency region with the most significant impact on the channel transmission from the oxide capacitance (the grey region is arbitrarily defined as that frequency region over which $S_{21}$ varies by 0.25dB across the range of modeled oxide capacitance parameters). The results indicated higher oxide capacitance introduced more than 0.25dB signal transmission loss from 1.1GHz to 3GHz. However, there was no noticeable impact on frequencies lower than 300MHz or frequencies higher than 20GHz. The dielectric oxide capacitance is related to the TSV diameter, the dielectric layer thickness, and the dielectric material permittivity. If the interested signal frequency is in the 1.1GHz-3GHz regions, increasing the oxide thickness or using a material with a higher permittivity constant can be applied to the TSV fabrication processes to reduce the oxide capacitance and therefore suppress the overall transmission loss. In addition, if the oxide thickness and dielectric material remain constant, scaling down the TSV diameter can reduce the dielectric oxide capacitance as well. However, generally TSV scale and oxide materials are not simple to change in a given TSV process. Thus, increasing oxide liner thickness is an applicable method to reduce oxide capacitance of the TSV.
Figure 5.16 Channel’s signal transmission $S_{21}$ with variation with TSV’s insulation layer oxide capacitance.

Another capacitance contribution is from coupling capacitance between the ground and signal TSVs ($C_{gs}$). Because the coupling capacitance is in series with the oxide capacitance, the much smaller coupling capacitance dominates the total capacitance of the TSV model. By varying the coupling capacitance value around the optimized value of 10fF, the coupling capacitance impact on the channel signal transmission is shown in Figure 5.17. The coupling capacitance exhibited a limited impact for frequencies below 3GHz, but exhibited a larger impact on signals with frequencies above 3GHz. And the impact is more significant than that of the oxide capacitance. (Similar to Figure 5.16, the grey region in Figure 5.17 is arbitrarily defined as that frequency region over which $S_{21}$ varies by 0.25dB across the range of modeled coupling capacitance parameters.) For frequencies higher than 8GHz, the $S_{21}$ magnitude difference due to different coupling capacitance remained constant at 0.25dB per 5fF. The coupling capacitance is primarily determined by the pitch between the signal and ground TSVs. The values of 7.5fF, 10fF, and 12.5fF were based on ground and signal TSV pitches of 25µm, 15µm, and 10µm. When the transmission signal is at
frequencies of 8GHz and higher, the TSV pitch is an important design parameter to consider. The signal transmission though TSV configurations with larger signal/ground pitches suffer significantly less loss.

![Figure 5.17 Channel’s signal transmission $S_{21}$ with variation with TSV’s coupling capacitance](image)

Besides capacitance, inductance is another parameter affecting high frequency signal transmission in the 3D channels. For modeling purposes the TSV inductance was varied about the nominal optimized value of 17.5pH. As shown in Figure 5.18, the insertion loss $S_{21}$ is affected by inductance at frequencies higher than 28GHz and the impact was more significant with increasing frequency. In Figure 5.18 the frequency region over which the TSV inductance parameter variation (12.5pH to 22.5pH) negatively impacted $S_{21}$, by more than 0.25dB is shown as the grey shaded area. These results showed that TSVs with higher inductance suffered less loss. The inductance is related to the magnetic flux over the current loop. For G/S TSV configurations, the loop area was proportional to the pitch of the ground and signal TSVs. Larger pitch is preferred for a larger inductance. This preference is also in accordance with the impact of the coupling capacitance. Interestingly, it is also contrary to intuition that closer ground TSVs and signal TSVs provide better EM field confinement so as to lower signal loss.
Figure 5.18 Channel’s signal transmission $S_{21}$ with variation with TSV’s inductance

Due to the conducting properties of silicon, the substrate conductance between the signal and ground TSV is another important parameter to study. The conductance is closely related to the coupling capacitance between signal and ground TSVs. As described in Chapter 3.2, the derivation for conductance also stems from the coupling capacitance. Shown in Figure 5.19, the most dramatic impact of the conductance on the signal loss occurs at frequencies higher than 3GHz (the frequency range over which conductance induced variations in $S_{21}$ exceeding 0.25dB are shown as a grey shaded area in Figure 5.19). The simulations were performed with $R_{GSi}$ of 625, 1250 and 2500Ω. The $R_{GSi}$ is directly related to substrate resistivity. 3D ICs fabricated with higher substrate resistivity suffer less signal loss. This observed conductance impact is also compatible with the measurement results shown in Figure 5.5. Another way to increase $R_{GSi}$ is by increasing the signal/ground TSV pitch. Higher pitch is preferred from this $R_{GSi}$ parameter analyses.
Figure 5.19 Channel’s signal transmission $S_{21}$ with variation of silicon substrate conductance between G/S TSVs

TSV resistance ($R_{TSV}$) is another important electrical element for the TSV model. By varying the resistance value from the calculated DC resistance (50Ω) to the AC resistance considering skin effects at 70GHz (290Ω), it is clear that there is a modest impact on the channel’s signal transmission. As shown in Figure 5.20, $R_{TSV}$’s impact is relatively uniform over the entire frequency range from DC to 65GHz. But, compared with capacitance and inductance impacts, the resistance impact is negligible. If one considers the TSV as a fat short copper wire, it is easy to understand that the electrical characteristics are dominated by the relatively large capacitance compared to the small resistance. This result also confirms that we can use a fixed resistance value for approximated setup in the lumped circuit model simulation without considering frequency dependent resistance due to the skin effect.
Figure 5.20 Channel’s signal transmission $S_{21}$ with variation with TSV’s resistance

In this TSV model, another important parameter is related to the landing pad. The landing pad is included into the TSV model because it is always attached to TSVs for electrical connection to planar interconnects. Landing pad capacitance mainly depends on the size of metal pad and the inter layer dielectric (ILD) oxide thickness. As shown in Figure 5.21, the impact from landing pad capacitance is substantial, primarily, for signals with frequencies above 20GHz (the frequency range over which the landing pad capacitance variation from 1fF to 5fF induced variations in $S_{21}$ exceeding 0.25dB are shown as a grey shaded area in Figure 5.21). At 65GHz, a difference in the landing pad capacitance of 2fF will result in a 0.3dB difference in insertion loss. Lower capacitance is preferred for lower signal loss from 3D channels. Therefore, while maintaining good electrical connections, designers should shrink the landing pad size for better signal transmission efficiency.
Figure 5.21 Channel’s signal transmission $S_{21}$ with variation with landing pad capacitance

In summary, from analyses on TSV models, critical guidance for 3D channel design in a multi-layer stacked system was provided. The high speed signal will suffer less loss if the TSV is fabricated with thicker oxide insulation layer, designed to have larger ground/signal pitch, and utilizes higher resistive substrates and smaller sized landing pads.

5.5.2 RDL design

In a 3D heterogeneous integration system, the high-speed channels connect and communicate wide band signals in both horizontal and vertical directions between functional modules distributed over the stacked system. The heterogeneous dies at each tier probably have different floor plans and layouts such as I/O pin locations. Thus, horizontal connections by RDL lines are necessary to insure proper communication paths. Therefore, for a complete signal communication path in a 3D system, besides the novel vertical connection TSV component discussed in last section, the horizontal RDL interconnect is another important component. It is necessary to investigate the impact from RDLs on the 3D channels.

Distinct from TSVs, which are surrounded by a semiconductor silicon substrate, RDL interconnects are surrounded by insulating dielectric layers; the same as traditional metal interconnects in 2D ICs. Because
of their small cross section areas for current flow, the resistance of RDLs is much larger than TSVs with the same length. By varying the resistance of RDLs from 100mΩ to 900mΩ, there was not significant difference on the transmission loss of the channel. Shown in Figure 5.22 – and very similar to the impact of TSV’s resistance – the impact of RDL resistance on transmission loss is uniform but very limited over the entire frequency range from DC to 65GHz. Theoretically, the RDL interconnect resistance would show a skin effect at high frequencies, but due to the small thickness of the interconnect (less than 1µm) relative to the skin depth for relevant frequencies, a constant resistance in the model is acceptable.

Figure 5.22 Channel’s signal transmission $S_{21}$ with variation with RDL resistance

Other than the resistance, it is important to consider the impact of other RDL’s electrical parameters on 3D channel transmission such as inductance $L_{RDL}$, conductance $R_{\text{sub}}$, and capacitance $C_{\text{rdl2sub}}$ and $C_{\text{sub}}$. As evident in Figure 5.23, there was no significant overall impact on the insertion loss $S_{21}$ when RDL parameters were varied in the model. With a relatively large variation of +/- 5pH from the nominal 8pH for $L_{RDL}$ (which was used in the optimized RDL model in previous sections) the insertion loss $S_{21}$ showed small variations at high frequencies above 30GHz but almost no difference at lower frequencies, as shown in Fig. 5.23(a). In addition, as the RDLs are surrounded by inter-layer dielectric materials with very high
resistivity, the high resistance ($R_{sub}$) induced by the substrate conductance doesn’t affect the channel’s insertion loss $S_{21}$ as shown in Fig. 5.23(b).

For metal wires fabricated by BEOL CMOS processes, inter layer dielectrics (ILDs) are used to isolate the copper wires from the conductive silicon substrate. This thin layer of dielectric material introduces capacitance between the RDL metal and the silicon substrate (denoted as $C_{rdl2sub}$ in the RDL model). No significant changes were exhibited by $S_{21}$ when varying the $C_{rdl2sub}$ from a nominal value of 20fF to 5fF and 40fF, as shown in Fig. 5.23(c). Another capacitance, $C_{sub}$, also showed no impact on the channel’s transmission loss $S_{21}$ as shown in Fig. 5.23(d).

In summary, from analyses in this section, the RDL electrical parameters had no significant impact on the 3D channel’s signal transmission efficiency. This conclusion was drawn from relatively short RDL
connections in 3D channels. Proper floor planning and routing are needed for every die in the 3D stack to limit the horizontal connection length so as to maximize the benefits from 3D integration for the high-speed signal transmission. However, if the actual 3D channel is composed of long horizontal RDL routing, detailed, specific analysis is needed and can be easily performed using the proposed equivalent models as presented in this section.

5.5.3 Bond pad design

For a multi-layer stacked 3D IC system, the bond pad is an important component that provides electrical connection between stacked dies. As described in Chapter 2, an extra layer of metal was added on top of the last layer metal of interconnects for the bond pads. Therefore, the via arrays connecting these two metal layers and the bond pad metal layer were both included in the bond pad model as shown in Figure 5.10 in Section 5.4.1. As described in Chapter 3.2, the bond pad model was simplified to a total capacitance $C_{\text{bondpad}}$. The nominal optimized total capacitance was 15fF, which had been validated by various test structures as discussed in Section 5.4.3. To investigate the bond pad capacitance impact on the channel’s signal transmission performance, the capacitance $C_{\text{bondpad}}$ was varied from 5fF to 25fF. As shown in Figure 5.24, the bond pad capacitance had a significant impact – more than 0.25dB difference in $S_{21}$ for bond pad capacitance ranging from 5fF to 25fF, for signals with frequencies over 15GHz. The impact was more substantial with increasing frequency. For a signal of 65GHz, increasing the bond pad capacitance by 10fF resulted in about 1dB higher channel signal loss. This result was compatible with the experimental results shown in Figure 5.9 in Section 5.3.5, a comparison of test structures with various bond pad sizes.
Figure 5.24 Channel’s signal transmission insertion loss $S_{21}$ with variation with bond pad capacitance

The bond pad capacitance in the model is directly related to the bond pad size and the number of vias used to connect the metal layers. Therefore, smaller pad size and a lower number of vias is favorable for less loss for signals with frequencies above 15GHz. However, larger sized bond pads can ease the alignment and bonding requirements and improve the fabrication yield. In addition, more vias can enhance the electrical connection and also reduce the resistance. Therefore, the optimized pad size and number of vias should be carefully determined by evaluating and balancing the tradeoff between the impact on high frequency signal transmission loss and manufacture yield.

### 5.5.4 Summary of 3D channel design

Figure 5.25 summarizes the major impacting elements of 3D components that have significant effects on signal transmission loss $S_{21}$. The grey shaded areas in each sub-plot indicate frequency regions over which variations in $S_{21}$ exceeded 0.25dB due as the design parameters ranged from low to high values (shown in the legends). In addition, with detailed analyses in this chapter, the impacts of the key channel elements on signal transmission performance were summarized as the impacting frequency range in Figure 5.26. For a complete 3D channel with modest horizontal distance, bond pad and TSV equivalent
element parameters have distinct impacts on different frequency ranges, while the RDL has negligible effects on the channel signal transmission performance over the entire frequency range.

Figure 5.25 Major impacting elements and respective impacting frequency range from: (a) oxide layer capacitance; (b) G/S TSV coupling capacitance; (c) TSV inductance; (d) substrate resistance; (e) landing pad capacitance; (f) bond pad capacitance.
Figure 5.26 Summary of electrical element influence region on S-parameter of 3D channel

Using the variations of $S_{21}$ exceeding 0.25dB over a given frequency range as an indication of significant impact from design element parameters, the detailed impacts from key design elements are listed below:

- Bond pad capacitance has substantial impact on signals with frequencies above 15GHz and the impact is more significant with increasing frequency. To reduce signal loss of the 3D channel, smaller bond pads are preferred but with a tradeoff of more demanding requirements on alignment and bonding processes.

- Within the TSV model, the coupling capacitance ($C_{Si}$), inductance ($L_{TSV}$), and resistance of silicon substrate between the signal and ground TSVs ($R_{GSI}$) impact $S_{21}$ primarily for signals with frequencies over 8GHz, 28GHz and 3GHz, respectively. The signal/ground TSV pitch directly affects these three parameters. Larger signal/ground TSV pitch is preferred since it yields lower coupling capacitance, lower inductance and higher substrate resistance, which therefore yield lower signal loss.
• Oxide insulation layer capacitance ($C_{OX}$) mainly affects $S_{21}$ for signals with frequencies from 1.1GHz to 3GHz. Within the fabrication process requirement, a thicker oxide layer is preferred for less transmission loss for signals with frequencies of 1.1GHz-3GHz.

• Smaller landing pads with less capacitance contribution to the TSV model induces less loss for signals with frequencies of 15GHz and higher.

References


CHAPTER 6 High Speed Signaling in a Stacked 3D System:
Circuit Perspective

6.1 Introduction

In previous chapters, we experimentally characterized and proposed/validated equivalent lumped element models for high frequency signal transmission analyses of 3D channels in a single or a multi-stacked system. The work and research described and discussed in those chapters was primarily focused on passive elements in a 3D channel for transmitting signals[1]–[6]. In a real system, active transmitter and receiver circuits play a key role in high-speed transmission of signals. To further understand the overall performance of a complete 3D high-speed channel, active driver circuits were also included in the analyses in this chapter from a circuit perspective.

In this chapter, we present comparative, simulation-based studies of two high-speed, active signaling schemes: single-ended signaling and differential signaling. Single-ended signaling was based on a signal-ground pair as modeled and discussed in Chapter 5. The signal information in such a system is carried by the voltage signal on one wire referenced to another wire (i.e. the ground wire). Differential signaling is based on a differential pair that transmits two signals 180° out of phase with one another. When detected in a receiver circuit differential signaling can provide significantly higher bit rates. For high-speed I/O channels utilized for on-chip, on-package and on-board applications, differential signaling is widely used because of its high noise suppression for common-mode noise and EMI reduction[7][8]. In contrast with traditional differential signaling on planar interconnects (chip, package or board), a 3D differential signaling system utilized TSVs, which are surrounded by a conducting silicon substrate. Thus, it is necessary to investigate the impact of the substrate and other variables on the performance of differential signaling in a 3D system. Many research groups have undertaken differential TSV analyses with lumped element models and experimental characterization[1], [9], [10]. However, to the best of the author’s
knowledge, have been no systematic circuit analyses of 3D differential channels with on-chip transmitter and receiver circuits.

For a complete channel analysis, active single-ended and differential transmitter and receiver circuits were designed and implemented using IBM 65nm technology[11]. The passive channel component models were simplified from the proposed equivalent circuit models that were previously validated by various test structure experiments in Chapter 5. Comparison between single-ended signaling and differential signaling will be presented with respect to signal integrity, timing analysis and power consumption. The complete 3D high speed signaling test system has been successfully designed. The designs for the active circuitry and the corresponding active, high-speed 3D channels have been validated and masks fabricated for IC processing and chip stacking, but final fabrication and assembly is ongoing at the time this dissertation was drafted and submitted. Testing of the final fabricated/assembled active, high-speed signaling circuits will be reported separately.

6.2 Transmitter and Receiver circuitry

To implement high speed signaling schemes with active circuits, various types of transmitter and receiver circuits were considered and applied to the 3D system in this study. The signal integrity, timing parameters and power consumption analyses were performed with both single-ended and differential signaling approaches. The details for the single-ended and differential signaling transmitter and receiver circuitries are presented in this section.

6.2.1 Single ended signal transmitter and receiver

For single-ended signaling, we used simple inverter buffers as drivers. As shown in Figure 6.1, the signal to be transmitted through the channel is input into ‘Tx’ from ‘In’ and the buffered signal from the transmitter will carried on the 3D interconnects as ‘sigl’. After transmission through the 3D interconnects (composed of TSVs, RDL lines and bond pads) the signal denoted by ‘sigO’ is transmitted into receiver ‘Rx’. The final output signal ‘Out’ is output at the receiver. Two sizes of transmitter and receiver circuits
were used in this study - 4X and 16X. The 4X inverter PMOS was 3.12 µm (4X780nm) wide and 60nm long and the NMOS was 1.56µm (4X390nm) wide and 60nm long. Because of the large size, both PMOS and NMOS were separated into 4 sections (fingers) and arranged in a square in the layout.

![Figure 6.1 Schematics of single-ended signal transmitter and receiver](image)

### 6.2.2 Differential signal full swing transmitter

A differential signal transmitter was used to convert and transmit the full swing single-ended signal to a waveform suitable for differential transmission. Thus, distinct from the single-ended transmitter’s single-port output, the differential transmitter has a two-port output. The simplest approach for which to apply differential signaling was to use an inverter based full swing transmitter as shown in Figure 6.2. Although not shown in the figure, the original signal will go through a pair of balanced transmission gates and inverter gates to generate a pair of inversed signals ‘in0i’ and ‘in0b’. To ensure a fair comparison between the single-ended and differential circuits, the same inverter-based transmitters and receivers for single-ended signaling (as described in previous section) were used in the full swing differential transmitter. The outputs of the full swing differential transmitter were denoted ‘sigl’ and ‘siglb’ with the same full voltage swing and 180° phase difference.
6.2.3 Differential signal reduced swing transmitter

Compared to the full swing differential signaling mode discussed in the previous subsection, the reduced swing differential signaling has benefits with respect to lower power consumption and higher speeds due to a faster transition time. The reduced swing differential transmitter was based on current-mode logic circuits (shown in Figure 6.3)[12], [13]. The bottom part of the transmitter with R0/T0/T1 elements,
functions as a current mirror circuit to provide stable current to both wings of differential input. R1 and R2 were used to provide a balanced voltage drop for both wings. Full swing signals – ‘in0i’ and ‘in0b’ – were driven from matched transmission circuit and invertor circuits to have the 180° phase difference. The transmitter output signals (‘sigl’ and ‘siglb’) will have reduced swing magnitude and 180° phase difference.

To implement the reduced swing differential transmitter circuit, multi-fingered transistors and cross positioning was used to ensure a balanced process variation on both differential wings. The detailed circuit element parameters and transistor sizes are shown in Table 6.1. L is gate length and W is gate width. N is the number of separate sections and M is the number of fingers in each section.

Table 6.1 Layout information for reduced swing differential transmitter

<table>
<thead>
<tr>
<th>Circuit element</th>
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<th>Layout multi-finger</th>
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</thead>
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<tr>
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<td>800Ω</td>
<td>--</td>
</tr>
<tr>
<td>R1</td>
<td>800Ω</td>
<td>--</td>
</tr>
<tr>
<td>R2</td>
<td>800Ω</td>
<td>--</td>
</tr>
<tr>
<td>T0/T1</td>
<td>L: 7.68µm; W: 60nm</td>
<td>N=4, M=4</td>
</tr>
<tr>
<td>T2/T3</td>
<td>L: 3.84µm; W: 60nm</td>
<td>N=2, M=2</td>
</tr>
</tbody>
</table>

6.2.4 Differential signal receiver

Both full swing and reduced swing differential circuitries use the same differential signal receiver as shown in Figure 6.4. The output receiver for differential signaling operates via current-steering techniques. The current mirror circuitry T0/T1 acts as a current source whose current flow was controlled by R0. The transistors, confirmed in their saturation modes, act as a current source. The current mirror circuitry T4/T5 ensures that the current flow was balanced for the differential wings for received signals. For full-swing differential drivers, the receiver circuit receives the differential signals from ‘vsing’ and ‘vsingb’ and then the inverter buffer T6/T7 outputs the signal at ‘Out’. Similarly for reduced swing differential
drivers, the receiver circuit receives the reduced swing signals from ‘vsing’ and ‘vsingb’ and then the inverter buffer T6/T7 recovers full swing signal at ‘Out’.

![Schematics of a differential signaling receiver](image)

**Figure 6.4 Schematics of a differential signaling receiver**

**Table 6.2 Layout information for differential receiver circuit**

<table>
<thead>
<tr>
<th>Circuit element</th>
<th>Value</th>
<th>Layout multi-finger</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>800Ω</td>
<td>--</td>
</tr>
<tr>
<td>T0/T1</td>
<td>L: 960nm; W: 60nm</td>
<td>N=2, M=2</td>
</tr>
<tr>
<td>T2/T3</td>
<td>L: 960nm; W: 60nm</td>
<td>N=2, M=2</td>
</tr>
<tr>
<td>T4/T5</td>
<td>L: 3.84μm; W: 60nm</td>
<td>N=4, M=2</td>
</tr>
<tr>
<td>T6</td>
<td>L: 480nm; W: 60nm</td>
<td>--</td>
</tr>
<tr>
<td>T7</td>
<td>L: 960nm; W: 60nm</td>
<td>--</td>
</tr>
</tbody>
</table>

To implement the circuit with proper transistor configurations to function as differential receivers for the 3D system, and ensure saturation stage for analog circuitry operation, proper sizing and strengths for each transistor were determined by iterative simulations and tuning. Similar to transmitters, multi-fingered
transistor and cross-positioning techniques were used to ensure balanced process variation on both differential wings. The detailed circuit element parameters and transistor sizes are shown in Table 6.2.

### 6.3 Reduced circuit models for 3D channels

For accurate simulation of the single-ended and differential signaling channels, detailed modeling of the passive interconnects are presented in this section. The equivalent lumped element models from Chapter 5 were validated by experimental characterization for wide band frequency up to 65GHz. In this chapter, we simulated the channel’s performance at 10Gbps – a typical high-speed digital interface. At this speed, the inductance effects can be neglected and the models can be simplified for faster simulation times without sacrificing accuracy. In this section, we use reduced RC circuit models based on proposed equivalent models and process design kit information for each component and the complete channel models.

The via-Middle 3D process integrated with the IBM 65nm 10lpe process was used to fabricate the test vehicle to perform the complete 3D channel characterization. TSVs were 50µm long and 5.5µm wide in diameter, same as the passive test structures that were investigated in previous chapters. The TSV models were based on validated models illustrated in Chapter 5.

For on-chip metal interconnects, 5 layers of 1X metal and 2 layers of 2X metal were used for connecting the TSVs, transmitters and receivers. The RDL line segments for planar connection use the first 2X metal. Figure 6.5 shows the detailed model configuration for the metal stack connection between the TSVs on adjacent dies. The resistance is derived from the metal layer structures and vias between metal layers. The capacitance originates from the interlayer dielectric capacitance and via capacitance etc. The detailed values were directly cited from the IBM 65nm 10lpe design kit[11]. The total 7 layer metal stacks were cascaded to form the connection between stacked TSVs, thus we modeled them into one metal stack model which can be instantiated in channel models, as shown in Figure 6.7. Basically, the 1X metal layer and 2X metal layer were with same model configuration but different electrical parasitic values based on design kit.
Figure 6.5 Metal stack model: 5 layer of 1X and 2 layer of 2X

To connect the transmitters and receivers to the TSV, RDL metal line segments were used. Figure 6.6 shows the model for the differential RDL line segment. All electric parasitic values were based on the geometry and process information in the design kit. The line segment was instantiated for use in the 3D channel models as shown in Figure 6.7.
With the designed component model library, a complete 3D channel with any configuration and any number of dies in the stack can be modeled by cascading the input to the output of each component. Figure 6.7 shows an example of a 3D passive channel in a 3-die stack. The metal stack first connects with the first layer of TSVs; and is then bonded to another metal stack from the adjacent die, and connects with consecutive TSVs, and line segments. The signal input and output are thereby connected to specific transmitters and receivers to form the complete high-speed signal transmission channel. The circuit simulations discussed in later sections were performed on such complete channels.
6.4 Circuit simulation results

For the various types of proposed high-speed signal channels, we use Cadence Spectre – a SPICE class of circuit simulators to analyze circuit performance metrics, such as signal integrity with eye diagram, timing parameters for delay information and total dynamic power consumption. We compared the simulation results of the proposed 3D systems with the various sets of single ended and differential signal transmitters and receivers.

6.4.1 Eye diagram results

Eye diagram analysis is an effective and straightforward way to evaluate signal integrity of a high-speed signal channel. It is a time domain characterization with hundreds to thousands of overlapped unit time intervals presenting signals received at receiver. Usually the input signal is a pseudo-random set of bit signals with a specific data rate. The vertical eye height represents the difference in voltage levels for 1s and 0s, while the horizontal eye width provides critical timing information such as jitter and setup/hold time specifications. A clear and open ‘eye’ is always preferred for high-speed signaling with different applications requiring specific eye heights and widths for reliable signal transmission.

For a complete comparison, we simulated multiple stacked 3D interconnects with different sized single-ended and differential transmitters and receivers. With smaller sized 4X transmitters and receivers, for a 2-die stack, differential signaling showed a more opened eye with wider width (60%) and height than single ended signaling, as shown in Figure 6.8. The eye for single ended signaling was closed with various distorted signals and higher jitter. This closed eye indicates higher bit error rate for the single-ended signaling system. However, for increasing number of dies, both differential and single-ended signaling eyes were closed for a 4X transmitter, due to higher RC load from stacked 3D interconnects. Stronger transmitters and receivers were hence needed to drive the higher load.
Figure 6.8 Eye diagrams for differential and single-ended signaling in 2-stack system with 4X Tx/Rx

With stronger 16X transmitters and receivers, both differential and single-ended signaling showed open eyes, which illustrated their ability to transmit the high-speed 10Gpbs signals. With the inverter recovering the voltage level, the eye height was almost 100% for both cases. The eye width was compared as shown in Figure 6.9. For fewer tiers in the stack such as 2-die and 3-die, the eye of the single-ended system was wider than that of the differential system. For a 2-die system, single-ended system has 95ps eye width while differential system has 87ps eye width. The difference was about 8ps for 2-die system and was decreased to 5ps for 3-die system. The difference was shrinking with more stacked
dies. The eye widths were almost same for the 4-die system at around 67ps. Differential signaling starts showing greater eye width and benefits over the single-ended system for 5 and more dies in the 3D stack system. These results indicate that for greater number of tiers and longer interconnect lengths, differential signaling showed better signal integrity than single-ended signaling. However, single-ended signaling shows more promise for smaller 3D stacks.

6.4.2 Timing parameters

The most important timing parameter in the test structures presented in this chapter that must be considered is the signal delay introduced by the passive and active paths. The delay was measured by the time difference between the input signal and output signal – measured at 50% of the transition point of the signals (i.e. at 500mV for 1V signal)[14]. The signal delay parameter was compared between single-ended and differential channels for 16X transmitters and receivers. As shown in Figure 6.10, for 2, 3 and 4-die stacks, differential channel introduces slightly higher delay than single-ended channel. However, with increasing number of stacks, the single ended signal delay increases faster than differential signal delay. More tiers imply greater resistance and capacitance load; thus the delay is increasing with more dies, as shown in Figure 6.10. For a 5-tier system, the delay of about 105ps was same for single ended signal and differential signal channel. Because the eyes were closed for systems with more than 5-tiers, we only showed the delay comparison for up to 5-tiers. However, with proper optimization with transmitter and receiver circuits and interconnect configurations, from this trend, it is reasonable to predict that differential signaling introduces less delay for many tiered 3D stacks. It is worth noting that greater sizes of transmitters can be utilized for providing high-speed signal transmission for die stacks with greater than 5 tiers.
6.4.3 Power consumption

Besides signal integrity and delay timing analyses, power consumption is another important metric for high-speed circuit performance[15]. For our various proposed differential and single-ended channels, we analyzed dynamic power consumption of each channel configuration. As shown in Figure 6.11, power consumption from differential signal channels was about 3 times that of single-ended signal channels for each multi-stacked system.

The reason for the huge difference was due to the fact that the transmitter and receiver circuitries for differential signaling were more complex than single-ended signaling drivers, requiring analog circuitry. The active transistors consume more power to realize the differential signal transmission scheme. However, if the transmission was through long interconnects and many tiers, the power consumption needs to be re-evaluated for specific cases since single-ended signaling would need repeater drivers for valid signal transmission. Thus, for short interconnections with limited number of tiers, if the power consumption is the main concern for the design, single-ended signal is preferred.
Figure 6.11 Power consumption of differential and single-ended channel for multiple stack systems

### 6.5 Conclusions

In this chapter, active driver circuits were added to 3D passive channel components to further understand the overall performance of a complete 3D high-speed channel. Differential and single-ended signaling schemes were investigated with various types of transmitters, receivers, and experimentally verified equivalent circuit models for 3D interconnects. Important circuit metrics were analyzed such as signal integrity (via eye diagrams), signal delay and power consumption of the complete channel path. Major conclusions are:

- With 4X transmitter and receiver for eye diagram analyses, differential signaling is able to transmit 10Gbps high-speed signal with a 60% eye opening for 2-die stack, while single-ended signaling cannot provide reliable signal transition due to a closed eye. For more than a 2-die stack, stronger Tx/Rx with larger sizes are needed for higher RC loads for both differential and single-ended signaling.
• With 16X Tx/Rx for eye diagram analyses, 3D stack systems with less than a 4-die stack performed better with single-ended signaling, while 3D stack systems with more than a 4-die stack system performed better with differential singling.

• Channel delay increases as the stacked die number increases. Single-ended signal channels suffer a slightly lower delay compared with the delay suffered by differential signal channels but with a higher rate. For 3D stack systems with more than a 5-die stack, a differential signal channel is expected to have a lower delay than single-ended signal channel.

• Due to the more complex Tx/Rx requirements for analog circuits, differential channels consumed about 3X power than single-ended signal channels in the cases studied. However, the power consumption needs to be evaluated for specific cases for long channels considering repeaters for single-ended channels.

Therefore, the design constraints and budget need to be carefully considered when choosing the desired high-speed signaling scheme for signal transmission in a 3D stack. Design metrics to be considered include number of tiers, bit rate, delay, power consumption, energy-delay product (EDP), real-estate considerations, etc. Based on the aforementioned metrics the final 3D design would be tailored to meet the specified constraints.

References


CHAPTER 7 Conclusions and Future Directions

7.1 Conclusions

3D integration using TSV technology has emerged as a promising solution to extend Moore’s Law by providing shorter interconnects lengths, smaller footprints and reduced power consumption compared to their 2D counterparts. Heterogeneous 3D ICs with stacked functional dies facilitate chip and package minimization. Characterization, modeling and simulation of various 3D channel configurations in a 2-tier die stack and a multi-tier die stack were performed to investigate key attributes and trade-offs for high-speed signal channel design in TSV based 3D systems. Circuit-level studies with validated performance models associated with active transmitters and receivers were also analyzed for investigation of complete high-speed links for 3D multi-layer stacked systems.

In a 2-tier stacked die system, experimental VNA characterization on fabricated 1SXG TSV dual chain test structures was performed to validate the prediction reported in the literature that additional ground TSVs provided better high frequency signal transmission owing to better EM shielding. With care to ensure measurement accuracy by carrying out proper calibration and de-embedding processes, our experimental results exhibited an inverse trend showing, rather, that the fewer ground TSV configuration (1S2G) had a lower signal loss than a 1S6G TSV configuration. Both full wave EM simulation with HFSS and equivalent circuit model simulations showed good agreement with our measured S_{21} and S_{11}. This confirmed the physical insights of the observed results and provided confidence to investigate the phenomenon with in-depth simulation approach. It was found that specific signal port settings in finite element modeling of 1SXG TSVs had a critical impact on results for simulations with isolated TSV structures, which most of the published research was based on. Therefore, isolated TSV simulation results without experimental validation were not reliable for design guidance or model validation standards for a 3D channel. Moreover, the true high-speed signal path in 3D IC applications originates from on-chip transceivers. Thus it is more reasonable to investigate 3D IC channel structures by setting ports at planar
interconnects such as the CPWs in the test structures, as shown in this work. Further investigation with validated full test structure simulations were also conducted and showed that the higher capacitance from extra ground TSVs induced higher impedance mismatch, thus cancelling out the EM field shielding benefits. Therefore, adding more ground TSVs around a signal TSV doesn’t necessarily improve high-speed signal transmission in 3D systems. A ‘few-ground’ TSV configuration provides higher transmission efficiency and consumes less die area.

In a multi-layer stacked die system, experimental characterization was performed on fabricated structures to investigate the impacts of substrate conductivity, redistribution layer (RDL) interconnects, and multi-layer stacking on high-speed signal transmission in 3D channels. Higher resistivity substrates are preferred for high-speed signal transmission. Also the bond pad has a substantial impact on 3D channel signal transmission. A large bond pad degrades signal transmission and decreases trace density. Optimized equivalent circuit models for key components in the 3D channel were designed using least square error function algorithm. Further analyses by varying electrical parameters in each model helped determine the expected performance impact on the 3D channel signal transmission. For TSV design, the ground/signal TSV pitch effects various electrical parameters such as coupling capacitance, inductance etc. Our analyses indicated that wider G/S TSV pitch provides better high frequency (above 2GHz) signal transmission. Following fabrication process requirements to ensure the manufacturing yield, a thicker oxide layer would be preferred for lower signal loss for frequencies ranging from 300MHz to 20GHz. Lastly, the analyses on RDL model parameters shows that RDL electrical parameters have limited impact on a 3D channel (for relatively short horizontal travel).

Circuit perspective analyses were also performed for complete 3D channels including active transmitters and receivers for high-speed single-ended and differential signaling schemes. Various versions of transmitter and receiver designs were utilized to facilitate high-speed signal transmission in 3D systems. For a 2-tier stack with a 4X transmitter and receiver, a differential signaling scheme is able to transmit 10Gbps high-speed signal with a 60% eye opening, while single-ended signaling cannot provide reliable
signal transition due to a closed eye. For 3D stacks with more than 2-tiers, stronger Tx/Rx with larger sizes are needed for the higher RC load for both differential and single-ended signaling. A 16X Tx/Rx single-ended signaling is superior for 3D stacks with more than 2 dies but fewer than 4 dies – with differential signaling performing better for taller stacks. Timing analyses shows that channel delay increases with increasing number of stacked dies. A single-ended signal channel suffers a slightly lower delay compared with differential signals for a stack with less than 5-dies. For more than 5-dies in the stack, a differential signal channel is expected to be faster than a single-ended signal channel. Due to the more complex Tx/Rx requiring analog circuits, the differential channel consumes about 3X the power compared with single-ended signal channels, in the studied cases. However, the power consumption needs to be evaluated for specific cases for long channels, including repeaters for single-ended channels.

The 3D channel design guidelines from this work will help semiconductor companies better develop 3D products with high speed links, leading to enhanced performance, reduced cost and faster time-to-market.

### 7.2 Future directions

The high-speed signal transmission analyses with fabricated 3D stacked wafer system were completed in this work. As an extension, a list of future work is proposed as follows:

- Experimental characterization on fabricated 3D channels including Tx/Rx to validate and correlate to the simulation results as discussed in Chapter 6.
- Investigation of other signal integrity issues including crosstalk and ground bounce in 3D systems.
- Applying the results and models detailed in this work to predict performance of other 3D systems for signal and power network analyses.
APPENDIX A: Fabrication Process Flow for Multi-layer Stack 3D IC

The multi-layer stack 3D IC fabrication processes include thinned wafer fabrication and stacking/bonding thinned dies to build multi-layer stack.

As shown in Figure A.1, the processes for the thinning and dicing wafers are as follows:

1. Device wafer with TSV’s and Cu bond pads
2. Device wafer attached to handle wafer using temporary bonding
3. Backside grinding and final reveal to expose TSV’s
4. Further backside processing to create metal layers and Cu bonding pads
5. Thin device wafer is mounted onto dicing tape and the handle wafer debonded
6. Temporary adhesive is cleaned
7. Wafer dicing to separate thin dies
Figure A.1 Process for the thinning and dicing wafers

With individual thin dies, stacking and bonding processes (using Cu-Cu thermo compression bonding techniques) are as follows:

1. 300mm base wafer with Cu bonding pads

2. A blanket layer of thermo-decomposable adhesive (blue) is coated on top of base wafer.

3. Multiple dies are tacked onto the base wafer one-at-a-time using short, low-temperature cycles in a high-accuracy die bonder

4. Collective bonding – heat and force applied across all die in parallel. During bonding, the adhesive thermally decomposes and the Cu-to-Cu bond is formed

5. Another adhesive layer is applied and dies are tacked on top of previous die

6. Repeat collective bonding to complete bonded die stack
Figure A.2 Stacking and bonding processes

Note: Courtesy of Robert Carrol and CNSE 3D integration group
APPENDIX B: Layout for passive 3-tier stack test vehicle

Figure B.1 presented the final superimposed layout for passive 3-tier stack test vehicle used for high speed signal transmission analyses in Chapter 5. The middle section is the RF test structures used in the comprehensive analyses.

Figure B.1 Superimposed layout of both sides of all dies in passive 3-tier stack test vehicle
APPENDIX C: Layout for circuits’ perspective high-speed signaling test vehicle

Figure C.1 presented the superimposed layouts of 3-tier stack multiple purpose wafer (MPW) with the circuits’ perspective high-speed signaling test vehicle (detailed analyses in Chapter 6) at the bottom section.

Figure C.1 Superimposed layouts of all 3 tiers of the MPW, with Circuit perspective high-speed signaling test vehicle at the bottom section.

Shown in Figure C.2 is the zoomed layout of active circuits-differential and single-ended transmitters and receivers multiplexed to the I/O.
Figure C.2 Different transmitter and receiver circuits multiplexed to the IO