Development of novel technologies to enhance performance and reliability of III-Nitride avalanche photodiodes

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Development of novel technologies to enhance performance and reliability of III-Nitride avalanche photodiodes

by

Puneet Harischandra Suvarna

A Dissertation
Submitted to the University at Albany, State University of New York in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

College of Nanoscale Science and Engineering

2014
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Dedicated to the beauty of nature
and the ones who try to understand her
Acknowledgements

First and foremost I would like to thank my advisor Prof. Fatemeh (Shadi) Shahedipour-Sandvik for the guidance that has made this dissertation possible. The encouragement I received to think new ideas and her nothing-is-impossible attitude has been instrumental in molding my personality. I would also like to thank my committee members Dr. L. Douglas Bell, Dr. Alexey Vert, Dr. Natalya Tokranova and Dr. Alain Diebold for their inputs towards the successful completion of this thesis.

This work would not have been possible without the teamwork, useful discussions and key contributions of our collaborators, Dr. Shouleh Nikzad, Dr. L. Douglas Bell and Dr. John Hennessy from the Jet Propulsion Laboratory at Caltech.

I am indebted to my senior team members Neeraj and Mihir for teaching me the skills and discipline of scientific research. I would like to thank them and our other lab alumni for setting high standards of excellence that served as a guiding light during my journey through graduate school.

Jeff with whom I had the greatest time overlap of 4+ years has a special place in my 'thank-you' list for being an excellent team player, for being able to catch details that I have overlooked and for wielding many complementary skills that I am short on. I would like to thank the other members of the lab as well, namely Jon, Isra, Jack and Neil for their inputs towards my research and for their energy and positive attitude that made labwork a pleasure.
I would also like to acknowledge the help of the CNSE engineering team especially Brian Taylor and John Winchell for their assistance in lab equipment maintenance. Finally I extend thanks to my non-technical advisors: my parents, my brother and my close friends in Albany namely Dhiraj, Abhishek, Anurag and Vijay for their endless support.
Abstract

Solar-blind ultraviolet avalanche photodiodes are an enabling technology for applications in the fields of astronomy, communication, missile warning systems, biological agent detection and particle physics research. Avalanche photodiodes (APDs) are capable of detecting low-intensity light with high quantum efficiency and signal-to-noise ratio without the need for external amplification. The properties of III-N materials (GaN and AlGaN) are promising for UV photodetectors that are highly efficient, radiation-hard and capable of visible-blind or solar-blind operation without the need for external filters. However, the realization of reliable and high performance III-N APDs and imaging arrays has several technological challenges. The high price and lack of availability of bulk III-N substrates necessitates the growth of III-Ns on lattice mismatched substrates leading to a high density of dislocations in the material that can cause high leakage currents, noise and premature breakdown in APDs. The etched sidewalls of III-N APDs and high electric fields at contact edges are also detrimental to APD performance and reliability. In this work, novel technologies have been developed and implemented that address the issues of performance and reliability in III-Nitride based APDs.

To address the issue of extended defects in the bulk of the material, a novel pulsed MOCVD process was developed for the growth of AlGaN. This process enables growth of high crystal quality Al$_x$Ga$_{1-x}$N with excellent control over composition, doping and thickness. The process has also been adapted for the growth of high quality III-N materials on silicon
substrate for devices such as high electron mobility transistors (HEMTs). A novel post-growth
defect isolation technique is also discussed that can isolate the impact of conductive defects
from devices.

A new sidewall passivation technique using atomic layer deposition (ALD) of dielectric
materials was developed for III-N APDs that is effective in reducing the dark-current and trap
states at sidewalls by close to an order of magnitude, leading to improved APD performance.
Development and implementation of an ion implantation based contact edge termination
technique for III-N APDs that helps prevent premature breakdown from the contact edge of
the devices, has further lead to improved reliability. Finally novel improved III-N APD device
designs are proposed using preliminary experiments and numerical simulations for future
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Chapter 1

Introduction

1.1 Motivation for UV detection

The ultraviolet (UV) region of the electromagnetic spectrum with wavelengths below 400nm, has attracted considerable scientific interest for many decades. The UV spectrum is generally classified into four regimes namely: near-ultraviolet (400 to 300nm), mid-ultraviolet (300 to 200nm), far ultraviolet (200 to 100nm) and extreme ultraviolet (100nm to 1nm). Alternatively they are also classified as UV-A (400-320nm), UV-B (320-280nm) and UV-C(280-100nm)[1]2 as shown in figure 1.0 [3].

The sun and the stars are powerful sources of UV and contain a wealth of information about the state and composition of our universe; however data in these regimes is scarce due to the lack of reliable and efficient detectors. Detection in the UV regime is also important for understanding and monitoring the biological effects of UV radiation on plant, animal and human health [2][4].
There are a number of other applications as well that stand to benefit from the development of UV detectors namely: flame detection, missile plume detection, covert communication, biological agent detection, transmission line monitoring etc.

Shown in figure 1.2 is the spectrum of solar radiation received on the earth’s surface [5]. Due to the absorption of ultraviolet radiation by oxygen and ozone in the upper layers of the atmosphere, the solar spectrum received on the earth’s surface is depleted of UV with radiation less than 400nm amounting to less than 10% of the total solar irradiance. Furthermore
radiation below 280nm is almost completely absorbed in the atmosphere making it very attractive for sensors and communication systems that operate in this spectral regime. Detectors which operate in this regime (<280nm) are called solar blind detectors since they can be operated on earth in broad daylight without any background signal from the sun. Similarly detectors that only respond to wavelengths below the human eye spectral limit (400nm) are termed as visible blind detectors.

Figure 1.3: Applications of solar blind UV detectors a) NLOS UV communication setup [8] and b) Detection of corona emission from high voltage power lines [11].
Short range communication in the solar-blind ultraviolet has a lot of advantages; it can be made secure, low power, anti-jamming and can also benefit from the completely unused communication bandwidth. For these reasons it has been under study and research since the 1960's [6]. A few groups have achieved such non line of sight (NLOS) UV communication by using UV transmitters employing an array of UV LEDs and receivers using photomultiplier tubes and solar blind filters [7][8].

Solar blind UV detectors are also useful in the detection of corona discharges in transmission lines and high voltage equipment [9]. The corona discharges lead to power loss, noise, electromagnetic interference, damage to transmission line insulators and produce ions and ozone [10]. The corona emission spectrum has been recorded to be in the range of 230 to 405nm, making it invisible to the naked eye; moreover it is hard to detect coronas in day time using conventional detectors due to the high background from sunlight. Corona monitoring is essential for the maintenance of high voltage transmission lines and serves as an early warning of equipment degradation. Shown in figure 1.3b [11] is an image of a 500kV overhead transmission line showing corona emission on the insulator string.

For the detection of stellar radiation below 280nm the detectors need to operate outside the earth’s atmosphere on rockets or satellites. The joint ESA-NASA spacecraft known as the Solar and Heliospheric Observatory (SOHO) was launched in 1995 equipped with extreme ultraviolet (EUV) imaging capabilities [12]. Another NASA space mission in 2006 launched a pair of spacecraft known as the STEREO to image the sun, that were equipped with multiple cameras including an EUV imager [13]. Shown in figure 1.4 are some of the images captured by these spacecraft. The data from these spacecraft has been extremely important in monitoring and studying solar wind, coronal mass ejections and space weather forecasting.
Unlike the sun, the imaging of the faint emission from distant galaxies and the intergalactic medium (IGM) would require photon counting detectors with high quantum efficiency. The intergalactic medium is composed of gases that connect and feed the galaxies throughout the universe. The mapping of the composition, density and other properties of the IGM are of high scientific interest [14][15]. III-N photodetectors are capable of very low noise, however their detection capabilities could be limited by the noise from the readout circuitry. By the use of avalanche multiplication, the signal can be amplified before it reaches the readout circuit resulting in a higher sensitivity. Further by operating the avalanche detectors in geiger mode, noise is no longer an issue and single photon detection can be achieved with a simplified digital readout circuitry [16].

Figure 1.4: a) Image of the sun captured using the extreme ultraviolet imaging telescope aboard the SOHO with 17.1nm in shown in blue, 19.5nm in yellow and 28.4nm in red [12]. b) EUV image of the sun taken by the STEREO spacecraft used to study and predict solar storms [13].
1.2 Photodetector parameters

Some of the important parameters for photodetectors are defined below.

**Dark current $I_d$**: The current through the detector in the absence of illumination.

**Photocurrent $I_{ph}$**: The current through the detector as a consequence of illumination.

**Responsivity $R$**: The ratio of the photocurrent to the incident optical power $P_{inc}$

$$R = \frac{I_{ph}}{P_{inc}} \quad \text{(1.1)}$$

**Quantum efficiency $\eta$**: The number of carriers collected per incident photon

$$\eta = \left(\frac{I_{ph}}{e}\right)\left(\frac{hv}{P_{inc}}\right) \quad \text{(1.2)}$$

Where $v$ is the frequency of the incoming photon and $e$ is the electron charge.

**Gain $M$**: The number of carriers collected per photogenerated carrier

$$M = \frac{I_{ph}}{I_{phUG}} \quad \text{(1.3)}$$

Where $I_{ph}$ is the photocurrent under a given voltage bias and incident optical power and $I_{phUG}$ is the photocurrent for the same incoming power but at a low bias voltage where the device shows unity gain (UG).

**Noise Equivalent Power $NEP$**: The smallest input signal that can detected by the device and is given by the lowest incident optical power that generates a photocurrent equal to the RMS noise current.
Specific Detectivity $D^*$: The specific detectivity is a measure of the sensitivity of a detector and is given by

$$D^* = \frac{\sqrt{A} \sqrt{B_w}}{NEP}$$  \hspace{1cm} 1.4

Where $A$ is the area of the device and $B_w$ is the bandwidth.

Spectral Bandwidth and Cutoff: The range of wavelengths of the incident radiation over which the photodetector shows measurable photoresponse.

1.3 Ultraviolet detectors

Ultraviolet photodetectors may be broadly classified into photon based and thermal based detectors. In thermal detectors the absorbed radiation causes a change in temperature which can then be detected by a change in resistance or electrical polarization. Thermal based detectors have limited applications due to their low sensitivity and lack of radiation wavelength dependence. Early photon based detectors used emulsion films, however they have been supplanted by photoelectric detectors [17]. Photoelectric detector technology can be further classified into photovoltaic, photoconductive and photoemissive technologies [17].

1.3.1 Photoemissive detectors

Photoemissive detectors make use of a photocathode to absorb the incident photons and eject electrons into vacuum. These electrons may then be multiplied by collision and secondary emission from high voltage plates known as dynodes. Shown in figure 1.5 is a schematic of a photomultiplier tube [18].
The development of the continuous channel electron multiplier (CEM) in the 1960’s using hydrogen annealed lead based glass fibers, spurred the development of the microchannel plate detector. Shown in figure 1.6 is the operating principle of the CEM photomultiplier. Radiation incident on the photocathode leads to the emission of electrons into the tube. These electrons are accelerated by the high electric field in vacuum, which causes them to strike the walls of the tube leading to the generation of secondary electrons which multiply in number from successive collisions as they drift across the tube to the anode [19].

A large number of these continuous channel multiplier glass fibers are fused and diced to create microchannel plate (MCP) ‘wafers’ which can then combined with readout circuitry to
create a UV imager. Shown in figure 1.7 is the MCP based UV detector used in the GALEX space mission [20][21].

![Figure 1.7: MCP based UV sensor used in the GALEX space mission [20].](image)

Photocathode technology for ultraviolet photo-emissive detectors is based around the use of highly reactive alkali metal based materials to achieve negative or very low electron affinities. Cs$_2$Te and CsI are the most commonly used photocathode materials for UV detectors [22][23]. Both of these materials require vacuum processing to avoid exposure to atmosphere that can severely degrade the photocathode. GaN and AlGaN are upcoming candidates for UV photocathodes and have several desirable properties like tunable direct bandgap, long term stability and radiation hardness. Cesiated p-type GaN based photocathodes have been explored[24] and found to have high quantum efficiencies[25], however the use of reactive cesium brings with it many of the drawbacks of the Cs$_2$Te and CsI based devices. Our group is involved in the development of novel device structures for III-N based photocathode without the use of surface cesiation that would lead to the realization of robust and highly efficient UV photocathodes [26].
The bulkiness, high operating voltages, fabrication challenges, vacuum enclosure requirements and photocathode and scintillator degradation make the use of photoemissive detectors extremely complicated for a wide variety of applications and hence the motivation to develop solid state detectors.

1.3.2 Photoconductive and photovoltaic detectors

Advances in semiconductor technology have enabled the realization of solid state photoconductive and photovoltaic detectors using a wide variety of semiconductors. Traditional semiconductor based photodetectors are not very suitable for UV detection due to high surface absorption and radiation induced damage of the semiconductor material. Silicon microelectronics being a extremely mature technology has been used in UV photodetection and does offer many advantages compared to photoemissive detector technology. However the indirect bandgap of silicon leads to poor quantum efficiency and the
low bandgap leads to very low penetration depth of the radiation and also necessitates the use of bulky filters to stop the visible and infrared light spectrum. Prolonged exposure to high energy radiation leads to accelerated aging of the devices leading to reliability and drift issues. For these reasons it would be extremely beneficial to realize a wide direct bandgap semiconductor based UV detector and hence the motivation for exploring the III-Ns [17]. To be capable of filter-free visible-blind detection a semiconductor with bandgap of greater than 3.1eV is needed and for solar-blind operation a bandgap of greater than 4.4 is needed, this makes GaN (bandgap 3.4eV) and Al$_{0.45}$Ga$_{0.55}$N (bandgap 4.4eV) suitable candidates for these applications. There are very few direct bandgap semiconductors in this bandgap range as shown in figure 1.9 [27].

Figure 1.9: Room temperature bandgap of various semiconductors with the indirect bandgap semiconductors in italics [27].
1.4 Photodetector device design

A number of device topologies have been explored for III-N based photodetectors, the prominent designs are photoconductive, metal-semiconductor (Schottky) diodes, metal-semiconductor-metal (MSM) and p-i-n diodes [28].

![Diagram of device structures](image)

Figure 1.10: Commonly used device structures for III-N photodetectors [28].

1.4.1 Photoconductors

A photoconductor is the simplest form of solid state photodetector. When photons with energy greater than the bandgap of the material are incident on the semiconductor, electron hole pairs are created that increase the conductivity of the semiconductor leading to an increase in current. In its simplest form an undoped semiconductor film with two ohmic contacts is used as shown in figure 1.10. The photocurrent is given by equation 1.5.
\[ I_{ph} = q \eta A \phi x G \]  \hspace{1cm} 1.5

Where

- \( q \) is the electronic charge,
- \( \eta \) is the quantum efficiency,
- \( A \) is the area of the device on which the light is incident,
- \( \Phi \) is the incident flux,
- \( G \) is the photoconductive gain and is given by

\[ G = \frac{t}{t_t} \]  \hspace{1cm} 1.6

Where

- \( t \) is the carrier lifetime
- \( t_t \) is transit time between the electrodes of the higher mobility carrier (electrons) and is given by

\[ t_t = \frac{L^2}{m_e V} \]  \hspace{1cm} 1.7

Where

- \( L \) is the distance between the contacts,
- \( m_e \) is the mobility of electrons and
- \( V \) is the applied voltage

The electrons due to their higher mobility get swept out of the material, this leaves the semiconductor positively charged due to the presence of photogenerated holes, which causes it to attract electrons from the contact; multiple electrons flow between the contacts for each hole before the hole is lost to recombination or is swept out. At very high electric fields the holes too are swept out faster than the recombination lifetime causing the gain to drop and approach unity [29]. Photoconductors with large carrier lifetimes show high gain but this limits
the response time of the detector making it suitable only for low bandwidth applications. These detectors also have high dark current due to the ohmic nature of both the contacts.

Diode based photodetectors are operated in reverse bias (or no bias) and have lower dark current than photodonuctors and the depletion region serves as the absorption region. The high field in the depletion region causes photogenerated carriers to separate and drift towards the opposite electrodes. The quantum efficiency of the device can be increased by increasing the size of the depletion region, but this comes at the cost of higher transit time and hence there is a tradeoff between quantum efficiency and bandwidth. Direct bandgap semiconductors like the III-Ns have an advantage here, since their high absorption coefficients enable thinner depletion regions with high quantum efficiency and speed.

1.4.2 Schottky photodiode

Schottky photodiodes in its simplest form is a semiconductor film with one ohmic contact and the other being a Schottky barrier contact. III-N Schottky photodiodes typically consist of a vertical structure with a n⁺ ohmic contact layer at the bottom and an undoped or n’ drift layer followed by a semi-transparent Schottky metal contact on top. Shown in figure 1.11 is the band diagram of a metal semiconductor photodiode. For energy greater than the bandgap of the semiconductor band to band excitation takes place, creating electron hole pairs that drift to the opposite electrodes registering a photo current. The Schottky photodiode can also show sub-bandgap photoresponse due to the internal photoemission effect for photons with energy greater than the barrier height energy $q\phi_b$ that are absorbed in the metal. Those hot carriers with energy sufficient to cross the barrier potential and momentum in the direction of the semiconductor make it into the semiconductor and contribute to the photocurrent. This
phenomenon has been exploited by Tripathi et al. [30] from our group in the design of tunable III-N hyperspectral detectors.

Figure 1.11: Band diagram of a Schottky device showing a) generation within the semiconductor and b) internal photoemission from the Schottky metal contact. c) Quantum efficiency as a function of incident photon energy [29].

1.4.3 MSM photodiode

MSM diodes are semiconductor devices in which both the contacts are the Schottky type. The fabrication of this type of device is extremely simple, since both the Schottky metal contacts can be deposited in the same lithography step and the absence of ohmic contact obviates the need for a conductive ohmic contact layer. However these devices typically require higher bias voltages to operate.
1.4.4 p-i-n photodiode

p-i-n based diodes are one of the most commonly used designs for photodetection. They consist of an i-type (intrinsic or undoped) semiconductor layer sandwiched between a p-type and n-type doped layer. The thickness of the i-layer can be chosen to get high quantum efficiency (thicker layer) or high speed (thinner layer). Under normal device operation, the i-layer is depleted and develops a uniform electric field across it. When excited with photons of energy greater than the bandgap, electron hole pair generation takes place. The electric field in the depletion region sweeps the photogenerated carriers to the n and p regions resulting in a photocurrent.

1.4.5 Avalanche photodiode (APD)

Photodiodes can be made to achieve gain internally in the diode at high bias voltages by secondary carrier generation through impact ionization. As the reverse bias voltage across the diode is increased, the electric field in the depletion increases, which accelerates the photogenerated carriers causing them to reach high velocities. When these accelerated carriers with high energy collide against the atoms of the lattice, they create secondary electron hole pairs.

The force acting on a electron in an electric field $E$ is given by

$$F = eE$$

The accelerated electron will acquire energy equal to the threshold energy for impact ionization ($U_{th}$), after traversing a distance $d$ in the electric field given by

$$d = U_{th}/F$$
However this assumes that it does not scatter and lose its energy before reaching the threshold energy; the probability of which, is related to the mean free path $\lambda$ of the electron

$$ p \approx \exp(-d/\lambda) \quad 1.10 $$

Substituting for $d$ in equation 1.6, we get

$$ p \approx \exp\left(-\frac{U_{th}}{e\lambda E}\right) \quad 1.11 $$

This leads us to the form of the impact ionization coefficient $\alpha$, which is the number of secondary electron-hole pairs generated per unit distance travelled by the primary photogenerated electron.

$$ \alpha = \alpha_0 \exp\left(-\frac{U_{th}}{E}\right) \quad 1.12 $$

Similarly the ionization coefficient of holes ($\beta$) may be derived.

For the case when $\alpha > \beta$, and assuming that the electrons are injected into the depletion region from the edge of the region, the multiplication gain due to electrons can be derived[29][31][32] and is given by

$$ M_n = \frac{1}{1 - \int_0^W \alpha \exp[-\int_0^x (\alpha - \beta) dy] dx} \quad 1.13 $$

A simplified expression may be derived by assuming $\alpha = \beta$ in which case the expression for the multiplication gain simplifies to

$$ M = \frac{1}{1 - \int_0^W \alpha \, dx} \quad 1.14 $$

Assuming constant ionization coefficient in the depletion region, the integral in equation 1.14 can be simplified to $\alpha W$
When $\alpha W = 1$ as per equation 1.15 the gain goes to infinity and breakdown occurs, this regime is known as the Geiger mode regime and can be used for extreme low light detection applications like photon counting. Shown in figure 1.12 is a typical reverse bias current voltage characteristic of an APD showing the no-gain, linear mode and Geiger mode regions [33].

![Figure 1.12: Reverse bias characteristics of an APD [33].](image)

### 1.5 APD device design

The design of III-N avalanche photodiodes requires careful choice of device structure, substrates, buffer layers, doping and thickness of the various layers. The most commonly used device designs are the Schottky, p-i-n and the p-i-n-i-n separate absorption and multiplication (SAM) based diodes. The basic structure of these devices and the simulated electric field
profile in the structure is shown in figure 1.13. The simulations were done in Synopsys Sentaurus TCAD with material parameters for GaN.

1.5.1 Schottky APD

III-N Schottky APDs typically consist of an undoped or low doped (n-) drift layer grown on top of an n\(^+\) doped conductive layer. Ohmic contact is made to the n\(^+\) layer and a semi-transparent Schottky contact is made to the undoped layer. The electric field profile is shown in figure 1.13 assuming typical values for the doping of the n\(^+\) layer (2 x 10\(^{18}\) cm\(^{-3}\)) and the drift layer (2 x 10\(^{16}\) cm\(^{-3}\)). Al\(_{0.4}\)Ga\(_{0.6}\)N based Schottky APDs with a gain of 1000 at 70V have been demonstrated by Ozbay et al. [34]. MSM GaN based devices with interdigitated dual Schottky electrodes on bulk GaN substrate have also been demonstrated with a gain of 1200 at 140V [35].

1.5.2 p-i-n APD

The p-i-n based APD design has an intrinsic (undoped) drift layer sandwiched between a p-doped and n-doped layer and ohmic contacts made to both the layers. Due to the higher quality, higher conductivity and lower contact resistivity that can be achieved in n-type GaN, it is usually made the bottom layer as opposed to the p-type. The i and p-layers are grown on top of the n-layer to complete the device. Devices illuminated from the top lose some of the quantum efficiency to absorption in the top metal and p-GaN, while devices illuminated from the bottom suffer from absorption in the substrate, buffer layers and the n-layer. Bulk GaN and conventionally grown GaN on sapphire templates have many microns of GaN below the device and preclude the option of back illumination.
<table>
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<th>Simulated Electric Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schottky APD</td>
<td>![Schottky APD Structure]</td>
<td>![Schottky APD Electric Field]</td>
</tr>
<tr>
<td>p-i-n APD</td>
<td>![p-i-n APD Structure]</td>
<td>![p-i-n APD Electric Field]</td>
</tr>
<tr>
<td>p-i-n-i-n APD</td>
<td>![p-i-n-i-n APD Structure]</td>
<td>![p-i-n-i-n APD Electric Field]</td>
</tr>
</tbody>
</table>

Figure 1.13: Structure and simulated electric field profile of the commonly used device designs for III-N avalanche photodiodes.
However back illuminated devices can be made possible by the growth of GaN APDs on double side polished sapphire with an optimized thin and transparent buffer layer. p-i-n GaN based APDs grown on bulk substrate[36] and sapphire[16] have been demonstrated with typical gains in the $10^4$ range and breakdown voltages in the 80-100V range. p-i-n devices on sapphire have also been demonstrated in back illumination mode by Dr. Razeghi’s group[37]. The back illuminated design makes it possible to design imaging arrays with the flip-chip configuration, simplifying device processing and integration with readout circuitry[38].

1.5.3 Separate Absorption and Multiplication (SAM) APD

The i-layer in a p-i-n APD serves as both the absorption region and the multiplication region. The i-layer maybe increased in thickness to increase the quantum efficiency but this also increases the breakdown voltage of the device. Higher breakdown voltages lead to higher circuit complexity and also higher leakage current and lower reliability due to the impact of the high voltage on defects, dislocations and the sidewall of the device. The separate absorption and multiplication device design make use of two i-layers, one of which is thicker and serves as the absorption region, while the other is thinner and serves as the multiplication region, allowing for designs with high quantum efficiency and high multiplication gains at lower voltages. Shown in figure 1.13 is the structure of a typical p-i-n-i-n GaN APD designed for back illumination. The thinner i-layer is sandwiched between the top p-layer and the intermediate n-layer and serves as the multiplication region. While the thicker i-layer towards the bottom serves as the absorption layer. Under UV illumination and reverse bias, photogenerated holes in the absorption region drift into the multiplication region, where the higher electric field causes gain due to impact ionization. GaN SAM APDs have been
demonstrated with gains in the $10^4$ range and have been shown to have higher gain and lower noise in back illumination mode [39].

1.6 Experimental work

Experimental work on the III-N APDs was begun with the optimization of GaN on sapphire templates to serve as low defect and high quality starting surfaces for device epitaxy.

1.6.1 GaN template growth

The templates were grown using the well known two step GaN epitaxy technique where a low temperature (LT ~525°C) GaN buffer layer is grown on annealed sapphire followed by high temperature (HT ~1030°C) GaN growth [40][41]. The V/III ratio and reactor pressure during the high temperature growth is adjusted in multiple steps to delay the coalescence and achieve low defect density [42].

The growth conditions of the template were optimized to achieve high quality, 4μm thick undoped GaN films on sapphire. Rocking curve measurements made using a Bruker high resolution X-ray diffraction (HRXRD) tool showed a FWHM of 249 arcsecs for the (0002) and 380 arcsecs for the (10\overline{1}2) reflection which compare very well with other works. Shown in figure 1.14 are the small area and large area atomic force microscopy (AFM) scans of the optimized GaN surface, showing a low defect smooth surface as evident from the sub 1nm RMS surface roughness of the 20μm x 20μm scan. The carrier concentration and mobility of the undoped GaN template were measured using the Hall technique and found to be
2x10^{16} \text{cm}^{-3} \text{ and } 550 \text{cm}^2/\text{Vs} \text{ respectively and compare well with values reported in literature by other groups.}

Figure 1.14: AFM images of the GaN on sapphire a) 2 \mu \text{m} \times 2 \mu \text{m} \text{ area and b) 20} \mu \text{m} \times 20 \mu \text{m}

The top two microns of the GaN template were doped with Silane during the growth to create a n-type template which is used as the starting surface for device epitaxy. The carrier concentration and mobility of the n-layer were also measured using Hall technique and found to be 2x10^{18} \text{cm}^{-3} \text{ and } 250 \text{cm}^2/\text{Vs} \text{ respectively. The high conductivity of the n-layer allows for low resistance contacts and low series resistance in the n-side of the device.}

Shown in figure 1.15 are scanning electron microscope (SEM) images of the surface captured by imaging samples interrupted at different stages in the template growth process. The use of a lower growth temperature (1000°\text{C}) during the initial stages of the high temperature (HT) growth (3D layer) leads to a larger density of islands (figure 1.15d) that coalesce to form a poor quality film (XRD (0002) FWHM \approx 400\text{arcsecs}), compared to films with the 3D layer grown
at the optimized temperature (1030°C) (figure 1.15b) that coalesce to form smoother films with higher crystal quality (XRD (0002) FWHM ≈ 250arcsecs).

Figure 1.15: SEM images of the sample surface after a) LT GaN buffer layer and HT anneal, b) optimized HT GaN grown in 3D growth mode on the buffer layer, c) start of coalescence of the HT GaN on optimized 3D layer and d) growth of unoptimized 3D layer.

*Scale bar in the images is 2μm.*
1.6.2 p-type GaN growth

p-type doping of GaN requires careful optimization of the growth process because of the difficulty in obtaining high hole concentration with good material quality. This is also one of the reasons why the p-type layer is typically the last grown (topmost) layer in most III-N structures, such that the crystal quality of the rest of the structure is unaffected. GaN can be doped p-type by the addition of group II elements namely Zn, Mg, Be or Cd to substitute for the Ga atoms in the lattice. However the activation energies of these dopants is very high, the lowest being Mg, which has an activation energy of 150meV, which is still much higher than the thermal energy available at room temperature [43]. Due to the high activation energy, only a small percentage (1 – 5%) of the dopant atoms are ionized, which makes it necessary to dope the material with two orders of magnitude higher magnesium atoms to achieve a given hole concentration.

p-GaN grown by MOCVD is highly resistive and shows very low hole concentration due to the formation of Mg-H complex that neutralizes the acceptor. One of the biggest breakthroughs in GaN in (1989-1992) was the discovery that high p-type conductivity can be achieved by post growth exposure to electron beam irradiation[44] or thermal anneal in nitrogen atmosphere to dissociate the Mg-H complexes[45].

The introduction of Mg into GaN also leads to the formation of defect levels that can be seen as peaks in the photoluminescence spectrum of p-GaN[46][47].p-GaN grown under non-optimized growth conditions can lead to the formation of defects and inversion domains[48][49] in the crystal and adversely impact device performance. An overdose of Mg can also lead to phase separation and other defects in the material[50][51].
<table>
<thead>
<tr>
<th>Growth Condition</th>
<th>AFM</th>
<th>Results</th>
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<tr>
<td><strong>a)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pressure = 100torr</td>
<td></td>
<td>RMS roughness = 2.8nm</td>
</tr>
<tr>
<td>Substrate = u-GaN template</td>
<td></td>
<td>hole conc. = resistive</td>
</tr>
<tr>
<td>(Cp_2Mg) = 120sccm</td>
<td></td>
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</tr>
</tbody>
</table>

| **b)** | | |
| Pressure = 300torr | | RMS roughness = 2.5nm |
| Substrate = u-GaN template | | hole conc. = \(3 \times 10^{17}\) cm\(^{-3}\) |
| \(Cp_2Mg\) = 120sccm | | mobility = \(8\) cm\(^2\)/Vs |

| **c)** | | |
| Pressure = 500torr | | RMS roughness = 1nm |
| Substrate = u-GaN template | | hole conc. = \(5.5 \times 10^{17}\) cm\(^{-3}\) |
| \(Cp_2Mg\) = 120sccm | | mobility = \(5\) cm\(^2\)/Vs |

| **d)** | | |
| Pressure = 500torr | | micro cracks on surface |
| Substrate = n-GaN template | | |
| \(Cp_2Mg\) = 120sccm | | |

| **e)** | | |
| Pressure = 300torr | | RMS roughness = 3.2nm |
| Substrate = u-GaN template | | hole conc. = \(5 \times 10^{16}\) cm\(^{-3}\) |
| \(Cp_2Mg\) = 200sccm | | mobility = \(3\) cm\(^2\)/Vs |

Figure 1.16: Growth conditions, AFM micrographs and results of the p-GaN optimization.
For the optimization of the p-GaN growth process; 400nm thick p-GaN was grown on undoped GaN templates under various growth conditions. A 700C, 15minute in-situ anneal in Nitrogen was done post-growth to activate the dopants, before characterization using AFM and Hall. Several growth parameters were studied, and reactor pressure was found to have significant impact on the properties of the p-GaN film.

Shown in figure 1.16 are the growth conditions and results of the Mg-doped p-GaN grown under the different conditions. An increase in growth pressure from 100torr to 300 torr was found to be helpful in increasing the hole concentration in the material from a resistive film (hole concentration below the measuring limit of the hall system) at 100torr to a film with a hole concentration of 3x10^17 cm^-3 with a mobility of 8 cm^2/Vs at 300torr. Increasing the pressure to 500 torr increased the hole concentration to 5x10^17 cm^-3 with a reduction in mobility to 5 cm^2/Vs and also resulted in a smoother p-GaN surface with an RMS roughness of <1nm for a 20μm x 20μm scan (figure 1.16c). However the p-GaN at 500 torr when grown on n-templates (as required for the APD structure) resulted in cracks in the surface (figure 1.16d) due to stress relaxation and hence was not pursued further. An increase in magnesium flow in the 300 torr growth recipe resulted in a very rough surface with lower conductivity (figure 1.16e), hence the growth condition at 300 torr with 120sccm of Cp2Mg (figure 1.16b) was chosen as the growth condition for the APD p-GaN layer.

The use of rapid thermal anneal (RTA) as the post growth annealing condition in place of the in-situ anneal was found to be helpful in increasing the hole conductivity. An RTA of 2mins at 800C in nitrogen resulted in p-GaN with a hole concentration of 4x10^17 cm^-3 and a mobility of 8 cm^2/Vs.
1.6.3 p-i-n APD fabrication process

The fabrication process for GaN p-i-n APDs begins with the MOCVD growth of n-type, u-type (undoped) and p-type GaN on a GaN-on-sapphire template. A thickness of 250nm for the undoped drift region and a p-GaN thickness of 250nm was used for these structures. Shown in figure 1.17 are the process steps for device fabrication.

After device growth and p-layer activation anneal (Step 1), the samples are diced using a diamond tipped blade into 1cm² pieces and are cleaned in acetone, iso-propyl alcohol and deionized water. The samples are blow dried with a nitrogen air-jet, a dehydration bake is done at 120°C for 5 minutes after which they are cooled to room temperature.

For the mesa etch process (Step 2), the samples are coated with an HMDS based adhesion promoter and then coated with Shipley 1813 positive photoresist using a spin coater. The samples are then exposed using a chrome mask and a UV contact aligner, after which they are developed in AZ300MIF developer. The samples are then inspected in a microscope and profilometer to check for wafer cleanliness, resist height and completion of development. A short bake at 120°C for 1 minute is done to harden the resist prior to etching. The resist masked samples are etched in an inductively coupled plasma (ICP) etcher using BCl₃/Cl₂ chemistry to create the device mesas. The etch rate is calibrated on a dummy sample prior to etching the APD structures. The etched samples are then cleaned in a photoresist remover solution (R1165) and organic solvents to remove photoresist residue from the surface.

For the p-Contact process (Step 3) the samples are patterned with AZ5214 based image reversal lithography to create an undercut profile.
Step 1: Device structure growth
MOCVD growth of n-i-p structure on GaN/Sapphire template and nitrogen annealing for p-GaN activation.

Step 2: Mesa etch
Positive photolithography using S1813 photoresist, ICP etching to create mesa and photoresist strip off in R1165.

Step 3: p-contact
Image reversal photolithography using AZ5214 photoresist, HCl+H₂O dip, 3nm Ni/3nm Au evaporation, liftoff in acetone, and Annealing in tube furnace @ 500C for 5mins in air.

Figure 1.17a: Growth and process steps for the fabrication of GaN pin APDs (steps 1 to 3)
Step 4: n-contact
Image reversal
photolithography using AZ5214
photoresist, HCl+H₂O dip, 50nm
Ti/150nm Au evaporation,
liftoff in acetone, and RTA
anneal @ 750C, 30s in nitrogen.

Step 5: Passivation
Blanket deposition of 250nm
silicon dioxide using PECVD.

Step 6: SiO2 RIE Etch
Photolithography using
AZ5214, RIE etch and
photoresist strip in acetone.

Figure 1.17b: Process steps for the fabrication of GaN pin APDs (steps 4 to 6)

Figure 1.18: Optical image of a fabricated APD wafer with devices of different dimensions.
The samples are dipped in HCl:H₂O = 1:1 for 60s prior to contact metal evaporation to clean the surface of any contaminants and oxide. The samples are loaded into an electron-beam evaporator and pumped down to the 10⁻⁷ torr range. 3nm Ni /3nm Au is evaporated to serve as a semi-transparent ohmic contact to the p-layer. The residual metal and photoresist is lifted off in acetone (or R1165) and the sample is inspected for shorts and photoresist residue. The cleaned samples are then loaded in a quartz tube furnace and heated in air for 5mins at 500°C to anneal the p-Contact metal stack.

For the n-contact process (step 4) a lithography step similar to the p-contact process is used to create resist openings with undercut over the n-GaN layer. The fragile nature of the thin (6nm) p-contact does not lend itself to easy probe contact or wire bonding so openings are created over the center of the p-contacts as well, such that the deposited metal can create a thicker contact pad. A stack of 50nm Ti/ 150nm Au is evaporated and RTA annealed for 30s @ 750°C in nitrogen, to improve ohmic contact resistivity.

Next (step 5), 250nm of silicon dioxide is deposited using silane and nitrous oxide based chemistry in a plasma enhanced chemical vapor deposition (PECVD) tool at 300°C. This is a blanket deposition over the entire sample.

The sample is then lithographically patterned (step 6) with photoresist openings over the p-contact probe pad and over the n-contact. The resist masked sample is etched in reactive ion etching (RIE) tool using CF4 plasma to etch the SiO₂ in the resist openings. Finally the samples are cleaned in acetone and ready for probing. Shown in figure 1.18 is an optical image of the processed APD wafer with devices of different dimensions.
1.6.4 Ohmic Contacts to n-GaN and p-GaN

Ohmic contact resistivity of contacts on n-GaN and p-GaN depend on a number of factors, namely conductivity of the surface, surface treatment, choice of metal stack and annealing conditions. Ohmic contacts to n-type GaN using Ti/Al and Ti/Al/Ni/Au metal stacks have been explored extensively for use in LEDs and HEMTs and specific contact resistances in the range of $10^6 \ \Omega \text{cm}^2$ to $10^8 \ \Omega \text{cm}^2$ have been demonstrated [52][53]. However achieving low resistance ohmic contacts on p-GaN is difficult with typical specific contact resistances in the $10^3 \ \Omega \text{cm}^2$ to $10^4 \ \Omega \text{cm}^2$ range [54][55]. The annealing condition for the contact metal stack has been found to be critical to achieving low contact resistivity and has been attributed to the formation of Ni-O and Ni-Ga-O at the interface [56].

To optimize the p-contact resistivity, circular transmission line model structures [57][58][56] were lithographically patterned on a p-GaN/undoped GaN template with the center pad of radius 50$\mu$m and the spacing between the pad and the outer region increased in steps of 5$\mu$m from 5$\mu$m to 35$\mu$m (figure 1.19a). The resistance between the circular pad and the outer region is given by

$$R_t = \frac{R_{sh}}{2\pi} \left[ \ln \left( \frac{R}{r} \right) + L_t \left( \frac{1}{r} + \frac{1}{R} \right) \right]$$  \hspace{1cm} 1.11

Where

- $R_t$ is the total resistance,
- $R_{sh}$ is the sheet resistance of the p-GaN,
- $r$ is the radius of the inner contact,
- $R$ is the radius of the outer contact, and
- $L_t$ is the transfer length
The resistance $R_t$ between the inner contact and the outer region is measured for the various spacings and plotted vs $\ln(R/r)$ (figure 1.19c). The slope of the line gives the sheet resistance $R_{sh}$ and the Y-intercept can be used to calculate the transfer length $L_t$. Then the specific contact resistivity $\rho_c$ is given by

$$\rho_c = L_t^2 R_{sh}$$  \hspace{1cm} (1.12)
A range of annealing temperatures and times were explored and 500°C for 5 minutes was found to result in the lowest contact resistivity. The gas ambient was also explored and a specific contact resistivity of $7.8 \times 10^{-3} \ \Omega \text{cm}^2$ was achieved by annealing in oxygen ambient, while a lower resistivity value of $4.4 \times 10^{-3} \ \Omega \text{cm}^2$ was achieved in air ambient and was thus used as the annealing condition for the APD samples. The IV curve after the optimized annealing treatment shows a linear characteristic compared to the high resistance non-linear behavior seen before annealing (figure 1.19b).

### 1.6.5 Device characterization

The current voltage (I-V) characteristics of the fabricated p-i-n APD devices were measured using a Keithley 6430 sourcemeter with a set current limit. For the photoresponse measurements, devices were illuminated from the top side (p-side) using a broadband xenon-lamp, a monochromator and UV fiber optic setup.

Shown in figure 1.20 is the current voltage characteristic of the p-i-n GaN/Sapphire APDs under dark (in blue) and under 360nm UV illumination (in red). The devices show a sharp breakdown at ~85V at which point the current rises sharply by more than five orders of magnitude and is limited by the current limit setting of the sourcemeter. The APD devices showed avalanche gains as high as $2.5 \times 10^5$ which is among the best reported gain for GaN APDs [59][60].
Figure 1.2: Temperature dependent breakdown characteristic of the GaN APD.

Figure 1.20: Reverse bias characteristic of GaN APD under dark (in blue) and 360nm illumination (in red) and the multiplication gain (in green).

Figure 1.21: Temperature dependent breakdown characteristic of the GaN APD.
To verify the avalanche nature of the breakdown, we measured the devices under different temperatures. The breakdown voltage showed a shift to higher values at higher temperatures that is characteristic of the avalanche breakdown mechanism. The positive temperature coefficient of the breakdown voltage is due to the reduction of mean free path of the carriers at higher temperature that leads to higher scattering, requiring them to be accelerated through a higher electric field to attain the critical energy necessary for impact ionization [61].

The spectral response of the devices were measured by changing the wavelength of the incident light on the sample, in the range of 200nm to 400nm, shown in figure 1.22 is the normalized responsivity which shows a peak responsivity at 363nm and a higher wavelength cutoff at 378nm well within the visible blind region (<400nm), making these devices suitable for visible blind UV detector applications.

![Normalized spectral responsivity of the GaN p-i-n APD.](image)

Figure 1.22: Normalized spectral responsivity of the GaN p-i-n APD.
1.7 Problems in III-N APDs

Measurement of a large number of devices on the APD wafer brought to light many problems with III-N APDs. A large number of devices showed premature breakdown at lower voltages leading to a shorted device but from the devices that showed repeatable breakdown characteristics important trends could be seen. It was found that devices with diameter greater than 40\(\mu\)m did not show a sharp breakdown characteristic, they instead show steadily increasing leakage current (figure 1.23) with a small jump at the breakdown voltage leading to a lower avalanche gain.

![Figure 1.23: Reverse bias IV characteristics of GaN/Sapphire p-i-n APDs with different mesa diameters: 40\(\mu\)m, 80\(\mu\)m and 120\(\mu\)m.](image)
Large diameter devices showed large fluctuations in current when biased at high reverse voltages. Shown in figure 1.24 is a plot of the current vs time for devices biased at 75V, the larger device (80\(\mu\)m diameter) show rapid fluctuations in the dark current compared to the smaller device (40 \(\mu\)m) which shows a gradually increasing current. The yield of devices with repeatable stable characteristics was found to be higher at lower devices diameters pointing towards the role of defects in the material.

![Figure 1.24: Dark current vs time for GaN/Sapphire APD with different diameter mesas: 80\(\mu\)m and 40\(\mu\)m.](image)

Measurement of a the dark IV characteristic from a large number of devices showed large variations in dark current even for devices of the same diameter in the same region of the wafer (figure 1.25). A variation in dark current of more than five orders of magnitude is seen at 60V, excluding devices that showed a short or low voltage premature breakdown.

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Figure 1.25: Dark current variation in 25μm diameter GaN/Sapphire p-i-n APDs. Measurement performed on 32 devices from the same region of the wafer.

Figure 1.26: Voltage cycling of APD a) before breakdown and b) after breakdown.
Shown in figure 1.26 are the results of voltage cycling of an APD before and after breakdown. The IV characteristic of the APD before breakdown in repeatable and retraces itself during the ramp down with negligible hysteresis (figure 1.26a), however once the device is taken to the breakdown voltage a permanent change in the IV characteristic is seen and the device shows hysteresis, indicative of traps in the device.

The development of filter free III-N solar blind APDs is only possible with devices made of AlGaN with Al>40%. However at the start of this work the quality of Al$_{0.4}$Ga$_{0.6}$N on sapphire that could be grown in the lab was extremely poor for APD development (figure 1.27).

Figure 1.27: AFM of the Al$_{0.4}$Ga$_{0.6}$N on sapphire, grown using conventional MOCVD.
1.8 Thesis organization

The rest of this thesis is focused on the development of technologies to improve III-N APD yield, reliability and performance.

The focus of chapter 2 is the development of growth techniques to improve III-N material quality and reduce defects.

Chapter 3 deals with the development of a novel sidewall passivation technique to reduce leakage current and hysteresis in the III-N APDs.

Chapter 4 deals with the development of a novel contact edge termination technique for III-N APDs to improve yield and reduce noise, leakage current and premature breakdown.

Chapter 5 introduces new device designs for III-N APDs using TCAD simulations and discusses future directions to this work.

1.9 Chapter references


Chapter 2

Techniques to reduce extended defects and their impact on APD performance

2.1 Impact of extended defects on device performance

Crystal defects in semiconductors can be detrimental to device performance. This is especially a problem with III-N materials, where native substrate technology is still not fully developed and require devices to be grown on foreign substrates like sapphire, silicon(111) or silicon-carbide leading to a large number of defects due to lattice and thermal mismatch with the substrate. The complexity of III-N devices requires growth of layers with precise composition, thickness and doping that cannot be achieved with bulk growth methods, necessitating the use of MOCVD or MBE for device structure growth. Shown in figure 2.1 is a Transmission Electron Microscope(TEM) micrograph of GaN grown on Sapphire [1]. As
can be seen in the image, dislocations starting from the substrate-buffer layer interface frequently thread all the way up to the surface. These extended dislocations act as leakage pathways and can lead to premature breakdown of the device, before the critical field is reached in the bulk of the material.

Figure 2.1: Transmission Electron Microscope image of GaN on Sapphire [1].

Figure 2.2: CL image [2] of the surface of a) GaN on Sapphire and b) HVPE bulk GaN.
The density of these dislocations is a function of the substrate, buffer layer scheme and the growth process. Cathodoluminescence (CL) imaging of the GaN surface reveals dislocations as dark spots due to their higher non-radiative recombination efficiency. The lower dislocation density in bulk GaN substrates can clearly be seen from the CL images of the GaN surface shown in figure 2.2 [2].

The periodicity of the crystal lattice leads to the formation of energy bands in semiconductors. However dislocations break the periodicity of the lattice due to broken bonds, leading to the formation of states within the bandgap [3][4]. Strain fields due to dislocations cause changes in atomic spacing and can lead to the formation of shallow levels [5] in the bandgap that can act as traps [6]. Furthermore dislocations may be charged and act as dopants, developing localized space charge regions and cause scattering of carriers and affect the mobility of devices [7].

Shown in figure 2.3 is the temperature dependent mobility of AlGaN/GaN heterostructures with different threading dislocation densities (TDD); the devices grown on bulk GaN substrate that have the lowest TDD of 5x10^7 show the highest mobility in the 2D electron gas [8]. The impact on mobility is highest at low temperatures where dislocation scattering is the dominant scattering mechanism. High mobility of electrons in the 2D electron gas (2DEG) of AlGaN/GaN heterostructures is of particular importance for III-N high power, high electron mobility transistors (HEMT) and has been seen to depend on the TDD in the material [7][8].

Defects at the metal semiconductor interface in diodes can cause increased leakage current due to defect assisted tunneling [9]. Dislocations can contribute to leakage current in devices by conduction through carrier hopping and trap assisted tunneling from one defect site to the
other [10][11][12]. Threading dislocations that have a continuous network of defects can be extremely detrimental to the performance of vertical devices [13][14].

Figure 2.3: Temperature dependence of the mobility of 2DEG in AlGaN/GaN heterostructures of different substrates [8].

Figure 2.4: Mechanisms of leakage current through defects [13].
Shown in figure 2.4 are the mechanisms of hopping conduction leading to reverse bias leakage current [13]. High electric field in reverse biased devices can lower the barrier for carrier emission from traps and enhance the hopping conduction by the Frenkel-Poole effect leading to increased leakage current [14][15].

The lateral epitaxial overgrowth technique which can be used to reduce the threading dislocation density in selected regions of the wafer, shows lower leakage current for devices fabricated on the laterally overgrown areas. Shown in figure 2.5 is the leakage current from devices on the same wafer that were fabricated on the laterally grown regions (lower TDD) and on the window regions (higher TDD)[16].

![Figure 2.5: a) Devices fabricated on the window and wing regions of a LEO GaN wafer and b) Reverse leakage currents in the devices from the two regions[16].](image)

Dislocations have also been known to act as recombination centers and have been shown to affect the optical output and lifetime of InGaN LEDs. It has been seen that for reverse biased LEDs and HEMTs at high electric fields, accelerated carriers can interact with the lattice and defects causing degradation at pre-existing defect sites leading to loss in optical performance and lifetime of the devices [17]. Localized avalanche breakdown at dislocation sites can lead to increased leakage current, noise, micro-plasmas and the formation of defect states that cause device shorting [18][19]. Hot carriers in high electric fields can also lead to further defect formation at existing defect sites [20]. Shown in figure 2.6 is the visible luminescence from reverse biased InGaN/GaN LEDs (40V), due to microplasma formation at defects [19].

Figure 2.6: Luminescent microplasmas on the surface of InGaN/GaN LEDs under high reverse bias (40V) [19].
Dislocations in the material can also serve as migration pathways for metal and other impurity atoms and can lead to increased leakage and device shorting [21][22][23]. The local electric field around spherical impurity particles in a semiconductor depletion region was studied by Shockley [24]. An enhancement of the electric field by 3 times and 1.5 times is possible around metallic and dielectric impurity particles respectively (figure 2.7). This enhanced electric field can lead to microplasmas at impurity sites and premature breakdown in devices [24][25].

Figure 2.7: Electric Field enhancement around foreign particles in a material with conductivity $\sigma_0$ and permittivity $\varepsilon_0$. a) Particle with $\sigma \gg \sigma_0$ (metallic particle) and b) Particle with $\sigma = 0, \varepsilon \ll \varepsilon_0$ (dielectric particle) [24] [25].

The threading dislocation density in III-N devices is a function of the substrate, buffer layers and the growth process. Discussed in the next section are the various III-N growth techniques.
2.2 III-Nitride bulk crystal growth

The group III-Nitrides are members of the III-V compound semiconductor group that include the III-As and III-Ps. But unlike them the technology for growing low defect bulk III-N crystals has lagged behind the device technology, which has conventionally resorted to the use of heteroepitaxial growth on non-native substrates. Melt growth which is the most commonly used technique for substrate manufacturing cannot be easily applied to the III-Nitrides; This is due to the fact that the melting point of III-Nitrides for example GaN is very high (>2000°C), and at these high temperatures, the vapor pressure of Nitrogen required to keep the GaN from decomposing is greater than 10,000 atm [26].

However in the past few years, bulk crystal growth technology of GaN and AlN has seen rapid growth using a number of different technologies, with manufacturers reporting 2-4” diameter GaN[27] and 1-2” diameter AlN bulk substrates with epi-ready surfaces [28]. There are a number of different technologies used for III-N bulk crystal growth, a few of relevance are described here.

2.2.1 Hydride Vapor Phase Epitaxy

Hydride Vapor Phase Epitaxy (HVPE) is a quasi-bulk crystal growth technique[29][27], but is considered to be the most practical solution for growing free standing GaN bulk substrates. The process is fairly simple and well understood [30]; First a chloride gas of the group III metal (Example: Ga) is formed by reacting HCl with Ga, this gas then flows downstream and reacts with ammonia to deposit GaN on the substrate surface. A Sapphire, GaAs or SiC substrate is commonly used and is later removed by mechanical methods or laser liftoff. The basic reaction mechanism is as follows.
\[ Ga + HCl \rightarrow GaCl + \frac{1}{2}H_2 \]

\[ GaCl + NH_3 \rightarrow GaN + H_2 + HCl \]

The high surface migration of the Chloride species results in very high growth rates of greater than 100μm/hour. This process is also extremely cost effective due to its relatively low temperature and pressure requirements. Intentional n-type doped wafers can also be achieved by HVPE[31] by the use of a silicon based gas (silane, disilane, dichlorosilane) or by the use of solid silicon exposed to HCl. Semi-insulating[32] and p-type doped GaN[33] can also be achieved by doping with various metals during HVPE.

![Figure 2.8: Schematic of a GaN, HVPE reactor[27].](image)

2.2.2 Ammonothermal Growth

A high pressure solution growth of GaN was attempted in the 1970s with pressures of greater than 10000 atm to grow GaN single crystals[34]. This method was later adapted into a solvothermal process that uses supercritical ammonia and a mineralizer, where by using
temperatures in the range of 400°C to 500°C and pressures of about 2500 atm, GaN crystals with excellent quality can be grown[35]. The process employing Alkali mineralizers uses polycrystalline GaN feedstock material at the low temperature region of the furnace and GaN seed crystals in the high temperature region of the furnace. The solubility of GaN when using an Alkali mineralizer has been found to decrease with increase in temperature, hence this process is able to utilize the convection currents in the reactor for mass transport[36][35].

Figure 2.9: Schematic of setup used for Ammonothermal growth[35]
2.2.3 Physical Vapor Transport

Physical Vapor Transport (PVT) is the commonly used technique for bulk AlN crystal growth[28]. The process can achieve growth rates as high as 100μm/hour. It involves the sublimation of Al and Nitrogen from a feedstock material, mass transport in gaseous phase and condensation over a seed crystal. Wafers are then sawed off the crystal and diameters upto 2” have been demonstrated with very low dislocation densities. Even though AlN has a bandgap of 6.2eV, bulk AlN wafers are not completely transparent due to impurities and defects and have a characteristic brown color (figure 2.11) [37][38].

Figure 2.10: Schematic setup for PVT of AlN[37].

Figure 2.11: Bulk aluminum nitride of 33mm diameter from Hexatech Inc [38].
2.3 Growth on non-native substrates

Due to the high cost and lack of easy availability of bulk substrates, researchers and manufacturers of III-N devices have resorted to the heteroepitaxial growth of GaN on non-native substrates like sapphire, silicon(111) or silicon-carbide. There are a number of growth techniques that can be used, however only a couple of these can provide the high degree of control in thickness, uniformity, doping and alloy composition necessary to fabricate III-N devices.

2.3.1 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) of GaN is typically performed in a high vacuum chamber with a Ga vapor beam from an effusion cell and an activated nitrogen beam from a plasma source directed towards a heated substrate (600-800°C). MBE can provide atomically sharp interfaces in a very high purity growth environment[39]. MBE uses lower temperature compared to MOCVD due to the high dissociation rate of GaN in high vacuum used in the MBE process. The process is expensive and has low growth rates and throughput compared to MOCVD.

![GaN MBE Growth setup](image)

Figure 2.12: GaN MBE Growth setup [68][41].
2.3.2 Metal Organic Chemical Vapor Deposition

Metal Organic Chemical Vapor Deposition (MOCVD) is the most popular method[40] for growing GaN based devices and has been the mainstay of the GaN optical and power devices industry. In this process volatile metalorganic sources carried by a carrier gas, typically N\textsubscript{2} and/or H\textsubscript{2} react with the nitrogen source typically ammonia, and deposit the III-N material on a hot substrate surface [41].

\[ R_2M + NH_3(g) \rightarrow MN(s) + 3RH(g) \]

R is the organic radical typically CH\textsubscript{3} or C\textsubscript{2}H\textsubscript{5} and M is the group III Metal (Al, Ga or In).

The process typically uses high growth temperatures (~1000°C) and high ammonia overpressure to prevent the dissociation of the III-N material. n-type doping is achieved by introducing a source of silicon typically using silane gas and p-type is achieved by magnesium doping using a metalorganic source typically (C\textsubscript{3}H\textsubscript{5})\textsubscript{2}Mg. The devices described in this thesis are grown using MOCVD in a VEECO D180 reactor at the Wide BandGap Optronix lab of the SUNY College of Nanoscale Science and Engineering.

Figure 2.13: D180 MOCVD showing the Growth chamber and Load lock.
2.4 Experimental work: APDs on bulk GaN

GaN p-i-n APDs were grown on HVPE bulk substrate using MOCVD. The high quality of the grown material on bulk substrate is evident from the smooth AFM of the GaN surface showing uniform parallel step edges, in comparison to the surface on sapphire that shows step terminations and defects (Figure 2.14 a and b).

![AFM images](image)

Figure 2.14: Comparison of the AFM of MOCVD GaN grown on a) HVPE GaN and b) GaN template on sapphire

![Structure diagram](image)

Figure 2.15: Structure of the p-i-n APD on bulk GaN.
The structure of the APDs grown on the bulk substrate was similar to those grown on sapphire as discussed in Section 1.6, except that the u-GaN layer thickness is 280nm instead of the 250nm that was used for the APDs on sapphire. The APDs were fabricated in a fashion similar to the process used for APDs on sapphire as detailed in Section 1.6.

Figure 2.16: APDs on HVPE-bulk GaN substrate a) reverse bias IV characteristics of APDs with different mesa diameters: 40μm, 80μm and 120μm, and b) dark current and UV-photoresponse in 120μm diameter device.
Shown in figure 2.16a is the IV characteristic of the APD on bulk GaN substrate. The devices on bulk substrate show sharp breakdown for devices of diameter from 40μm to 120μm unlike the devices on sapphire that show a soft breakdown (figure 1.23). This can be attributed to the higher material quality of the devices on bulk substrate that allow for a low enough number of defects even in large device diameters to enable a sharp breakdown.

The devices on the HVPE substrate also showed lower noise and more stable dark current. Figure 2.17 shows the plot of dark current vs time for APDs on bulk and sapphire substrate biased 10V below the breakdown voltage. The 80μm diameter device on the HVPE substrate showed less than 4% of drift in dark current compared to greater than 80% in the 80μm APD on sapphire and 32% in the 40μm GaN/sapphire APD.

![Graph showing dark current vs time for APDs on sapphire and HVPE GaN substrate.]

Figure 2.17: Dark current vs time for APDs on sapphire (80μm diameter and 40μm diameter) and HVPE GaN substrate (80μm diameter).
HVPE GaN is not completely defect free and has a dislocation density in the $10^7 \text{cm}^{-2}$ range compared to GaN on sapphire that has $\sim 2 \times 10^8 \text{cm}^{-2}$. Also, imperfections in polishing of the HVPE substrate leaves scratches on the surface that leads to roughness and defects, as shown in the large area AFM in figure 2.18b.

Even though the devices showed a very sharp breakdown voltage across device diameter, the yield of devices larger than 40$\mu\text{m}$ was very low, possibly as a result of the imperfections of the GaN surface due to scratches in the substrate.

![Figure 2.18: Defects in GaN grown on HVPE substrate a) small area AFM and b) large area AFM showing non-uniformity due to overgrowth on substrate scratches.](image)

To achieve solar blind operation, AlGaN APDs with Al $> 40\%$ need to be developed. The development of AlGaN APDs brings with it many more challenges in addition to the problems already discussed for GaN APDs.
2.5 Challenges in AlGaN Growth

Technology for the growth of GaN bulk substrates and GaN heteroepitaxy on non-native substrates has matured to the point that high quality GaN substrates and templates are easily available. However the numerous challenges remain for the growth of high quality AlGaN materials/layers with high Al percentage. This is even more important given that no bulk growth technique is available for the growth of free standing AlGaN substrates. This section describes some of the associated challenges.

2.5.1 Cracking

The easy availability of GaN substrates and heteroepitaxial templates prompted inquiry into the use of these substrates for AlGaN growth. However the lower lattice constant of AlGaN compared to GaN, causes the film to be tensile strained; once a critical thickness is reached this strain is relieved leading to cracks. A critical thickness of less than 100nm has been observed for high Al composition films on GaN[42][43]. This makes the use of GaN templates impractical for AlGaN based device since they typically require thicknesses upwards of 1μm.

2.5.2 Parasitic reactions

Trimethylaluminum (TMAI) is the most commonly used organometallic for Al Source in III-N MOCVD. TMAI is highly reactive and has been observed to form a white crystalline solid when it reacts with ammonia even below room temperature[44]. This high reactivity of TMAI and ammonia leads to parasitic gas phase reactions before the reactants can reach the substrate surface. This leads to poor aluminum incorporation efficiency, low growth rates and particulate content that can lead to defects and impurities in the AlGaN material. The parasitic
reactions also make the relation between the gas phase Al composition and solid phase non-linear and difficult to control. Several methods have been looked into to reduce parasitic reactions[45], including reduced reactor pressures, higher gas velocity and modified reactor design.

2.5.3 Low adatom mobility

Even though the problem of gas phase parasitic reactions can be mitigated to some extent by using low pressures, low ammonia flow, moderate growth temperature and intelligent reactor design[45], one of the fundamental problems affecting AlGaN film quality still remains, namely the low adatom mobility of aluminum. From our previously reported work on density functional theory based calculation of adatom diffusion barriers, we see a very high diffusion barrier of 1.1eV and 2.28eV for an Al adatom on Al terminated and N terminated AlN (0001) surfaces respectively[46]. In comparison Ga adatoms face a diffusion barrier of only 0.32eV and 1.79eV on Ga terminated and N terminated GaN (0001) surfaces respectively[47]. This explains why AlGaN films show a lack of coalescence compared to GaN grown under the same growth conditions.

2.5.4 Doping

In order to design AlGaN based devices it is important to be able to grow n-type and p-type AlGaN. n-type AlGaN is absolutely essential since it is commonly the first layer in the device structure stack and is required to form a conductive contact layer whereas the requirement of p-type AlGaN is frequently circumvented by the use of pGaN, since usually this is the topmost layer for the majority of device structures and its function is not to support the subsequent growth of thick AlGaN layers. Achieving low resistivity n-type doped AlGaN is challenging
in high aluminum alloy compositions, due to the increase in activation energy of Si dopant atoms with increasing Al composition, (from 17meV for GaN to 95meV for AlN at room temperature with $n \sim 5 \times 10^{17}$ cm$^{-3}$ [48]) and the decrease in mobility from greater than 200 cm$^2$/Vs for $n$-GaN to about 20 cm$^2$/Vs in $n$-AlN. Moreover non-optimized doping conditions can lead to point defects in the films that will in turn reduce both carrier concentration and mobility [49].
2.6 Metal adatom diffusion length enhancement: Novel Pulsed MOCVD process for AlGaN Epitaxy

A novel MOCVD growth process was designed to address the AlGaN growth challenges explained in the previous section. For the optimization of this process, first the binary semiconductor AlN was targeted. Our process for AlN separates the introduction of the nitrogen source namely ammonia and the aluminum source namely TMAl by pulsing them alternatively. To achieve this, pneumatic valves on the respective lines are switched from run to vent mode and vice versa. This results in a TMAl pulse in the reactor for a set period after which TMAl is shut off and vented and the ammonia source is switched on for a set period, this sequence is repeated until the desired thickness is grown. This method reduces parasitic gas phase reactions since at any point of time only one of the reactants is being injected into the growth chamber. It also addresses the issue of low adatom mobility of the Al species since during the TMAl pulse, in the absence of ammonia, the Al species have sufficient amount of time to migrate on the growth surface to suitable (i.e. the most energetically favorable) lattice site thereby resulting in high quality growths at a lower temperature compared to conventional MOCVD. For the AlGaN growths a different pulse sequence was employed and will be explained later in the section. The gas flows and pulse durations were optimized experimentally by characterizing the quality of the films by XRD, AFM and EPD (etch pit density).

As discussed previously, AlGaN grown on GaN leads to cracking and strain relaxation through defects. To avoid this, the AlGaN layers would need to be grown pseudomorphically on bulk aluminum nitride or sapphire substrate. The high cost and lack of easy availability of bulk aluminum nitride wafers makes the growth on sapphire a very attractive option if material
quality can be improved. This approach also has the advantage of being able to facilitate back illumination for detectors and back emission for LEDs, since double side polished sapphire is transparent to UV as compared to bulk AlN wafers that show significant absorption in the UV region. The effect of substrate miscut was also explored and will be explained later in the section.

The films grown using pulsed MOCVD were characterized using High Resolution X-Ray Diffraction (HRXRD) to measure the lattice constant of the films and determine the alloy composition of the AlGaN films. These were also correlated with UV-Vis absorption spectroscopy for layers grown on double-side polished sapphire. Atomic force microscopy (AFM) of the surface and rocking curve XRD measurements were used to determine the surface and crystal quality respectively. Etch pit density of AlGaN/AlN structures was done to measure the macro-defect density. Electrical measurements for samples grown on sapphire substrate were done in a Hall measurement tool with Van der Pauw geometry to determine carrier concentration and mobility of the films.

2.6.1 Pulsed AlN development

All the growths here employ an AlN buffer layer. We have previously reported on the growth parameters for AlN buffer layer optimization [50]. Sapphire wafers with 25nm thick AlN buffer layers were loaded into the reactor and heated up to a growth temperature of 1050°C, no explicit annealing step was used. For the optimized growth process, a reactor pressure of 40torr, ammonia flow rate of 3.4 slm and TMAI flow rate of 43μmol/min were used. For the pulsed MOCVD growth the flow of TMAI and NH₃ was alternated every 6 seconds (figure 2.19b). The time duration of 6s was based on the growth rate calculations of thicker AlN layer to give a growth rate of approximately one monolayer per cycle. Given the low
desorption rate of Al at these temperatures from an AlN surface, a very small fraction of the adsorbed Al atoms leave the surface during the 6s of TMAI flow in the absence of ammonia. As can be seen from the AFM micrographs shown in Figure 2.19, the pulsed MOCVD grown AlN has a very smooth surface with clear atomic terraces and a surface roughness of 0.47nm for a 20μm x 20μm area compared to the conventionally grown AlN which shows a pitted surface (Figure 2.19a).

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Figure 2.19: Pulse sequences and AFM micrographs of a) Continuous flow AlN and b) Pulsed MOCVD grown AlN.
High resolution XRD measurements of the (0002) reflection show a FWHM of the 47 arcsecs for the pulsed films in comparison to greater than 1500 arcsecs for the continuous AlN as reported previous by J. Grandusky et. al. [50]. The FWHM of the (0002) reflection measured for the pulsed films compares very well with the best reported values of both homoepitaxial and heteroepitaxial AlN [51][52]. It is also notable that films as thin as 50nm showed similar surface and crystalline properties. This is in contrast to other works where larger thicknesses of AlN are employed as templates for AlGaN growth[53][54].

2.6.2 Pulsed AlGaN development

High aluminum percentage AlGaN shares much of the same problems as AlN growth. Given the success of pulsed growth for AlN, the pulsing scheme was explored for the growth of AlGaN. For development of pulsed AlGaN, growth was carried out on 50nm thick pulsed AlN buffers on sapphire. The flow rates of 43μmol/min and 72μmol/min were used for TMAl and TMGa respectively. The flow rate of ammonia was 3.4 slm for all the experiments.

A number of pulse sequences were tried as shown in Figure 2.20. From these growths, AlGaN growth using sequence #b shows no gallium incorporation in the film, this is not unexpected due to high desorption rate of Ga at these high temperatures[55] in the absence of ammonia. AlGaN grown using pulse sequence #c shows a measurable gallium incorporation but the film shows a rough surface with non uniform composition and poor crystal quality, this is possibly due to the fact that during the $\text{TMGa} + \text{NH}_3$ pulse, the GaN nucleates on the lattice mismatched surface in the form of islands.
Figure 2.20: MOCVD Pulse sequences and corresponding AFM micrographs of AlGaN.
AlGaN grown using sequence #d shows uniform composition and atomically smooth surface in comparison to the conventionally grown AlGaN which shows dislocations, pits and high roughness as evident in the AFM micrographs shown in figures 2.20 a) and d).

The flow rate of ammonia did not have any significant influence on the AlGaN properties for sequences #b and #c, however for sequence #d, an increase in Ga incorporation was observed with increasing ammonia flow and a flow of 8slm of $NH_3$ with a flow rate of 72μmol/min and 43μmol/min for $TMGa$ and $TMAl$ flow, respectively was found to result in a film of Al$_{x}$Ga$_{1-x}$N as evidenced by the XRD 2θ-ω scan (figure 2.21 a), this was also confirmed by the

Figure 2.21: a) HRXRD spectrum showing the AlGaN and AlN peaks, and b) UV-Visible spectrum of AlGaN showing a sharp absorption cutoff and interference fringes from the thickness of the film.

The flow rate of ammonia did not have any significant influence on the AlGaN properties for sequences #b and #c, however for sequence #d, an increase in Ga incorporation was observed with increasing ammonia flow and a flow of 8slm of $NH_3$ with a flow rate of 72μmol/min and 43μmol/min for $TMGa$ and $TMAl$ flow, respectively was found to result in a film of Al$_{x}$Ga$_{1-x}$N as evidenced by the XRD 2θ-ω scan (figure 2.21 a), this was also confirmed by the
UV-Visible transmission spectrum (figure 2.21 b) through the DSP sapphire substrate which shows a sharp absorption cutoff at 250nm.

For the growth optimization of pulsed AlGaN, two different sapphire substrate miscuts were explored $1^\circ$ and $0.2^\circ$. Figure 2.22 shows the difference in AlGaN morphology between them. AlGaN grown on the $1^\circ$ substrate shows step bunching to form alternating (0001) and high Miller index facets (Figure 2.22 a) due to the misorientation of the substrate. AlGaN on the $0.2^\circ$ miscut wafer showed better XRD FWHM and lower AFM roughness and hence was used for the remainder of the experiments.

![Figure 2.22: a) Pulsed AlGaN grown on sapphire with miscut a) $1^\circ$ and b) $0.2^\circ$](image)

### 2.6.3 n-type doping of pulsed AlGaN

The next step in the development and utilization of pulsed AlGaN is n-doping. Silane doped pulsed AlGaN films were grown and evaluated based on their crystal quality and electrical characteristics namely carrier concentration and mobility as measured by Hall technique. With optimal flow of silane during the pulsed Al$_{x}$Ga$_{1-x}$N growth, an electron
concentration of $1.7 \times 10^{18}$ cm$^{-3}$ with a mobility of 91 cm$^2$/Vs was achieved without any degradation in material quality (figure 2.23). Increasing the silane flow beyond the optimal flow was found to degrade material and electrical properties, similar to our earlier reported work with doping of AlGaN [50]. Using the pulsed MOCVD technique, we have been able to grow crack free AlGaN films with thickness greater than 500nm on sapphire substrates. The values of carrier concentration and mobility of the pulsed n-AlGaN films are among the best reported results for high aluminum percentage n-AlGaN on sapphire[49].

![AFM micrographs of n-AlGaN.](image)

**Figure 2.23: AFM micrographs of n-AlGaN.**

### 2.6.4 AlGaN on Silicon

AlGaN plays a crucial role for III-N devices on silicon, in addition to being a part of the device stack in many applications (like HEMTs and LEDs), AlGaN layers are also used as buffer layers for stress reduction to enable growth of crack-free GaN templates on silicon substrates[56]. The large thermal expansion of coefficient mismatch and lattice mismatch between III-N and silicon, leads to tensile stress generation and defects in the film. By utilizing the pulsed MOCVD technique optimized for films on sapphire, as outlined above, high quality AlGaN films on Si(111) were able to be grown. Shown below (Fig. 2.14) is the AFM images
of a 60%Al, AlGaN film on silicon. Like the growth on sapphire, the growths on Si(111) require an AlN buffer layer and here a ~200nm AlN buffer is used. A surface roughness of 0.34nm and 0.46nm are achieved for pulsed AlN buffers and subsequent 300nm thick Al$_x$Ga$_{1-x}$N grown on these buffers respectively. GaN (1.2μm thick) films grown on these AlGaN layers are crack free across the 2” wafer surface and show a surface roughness of 0.23 nm with a XRD FWHM(0002) of 688 arcsecs. This is a remarkable result given that no defect reduction techniques like ELO or in-situ SiN were employed in this work.

Figure 2.24: AFM Micrographs of a) 200nm Pulsed AlN b) 200nm Pulsed Al$_x$Ga$_{1-x}$N and c) 1.2μm GaN on Si(111) substrate.
2.7 Experimental Results: AlGaN APD

Given the success of the growth of high quality of n-type and undoped pulsed AlGaN, solar blind Schottky type AlGaN APDs were fabricated on sapphire substrate. Shown in figure 2.25 is the structure of the device grown for this purpose.

![Figure 2.25: Structure of Schottky AlGaN APD.]

The bottom AlN and the u-Al$_{0.4}$Ga$_{0.6}$N layers serve as the buffer layers for the structure grown on double side polished (DSP) sapphire. The n-Al$_{0.4}$Ga$_{0.6}$N serves as the n-contact layer and the u-Al$_{0.4}$Ga$_{0.6}$N serves as the active region of the device. The wafer was patterned into circular mesas using ICP etching followed by contact metal deposition. For the top contact, 50nm of platinum was used to make a Schottky contact to the u-Al$_{0.4}$Ga$_{0.6}$N. For the n-contact Ti/Al metal stack was evaporated on the etched n-AlGaN to make the ohmic contact. The devices were characterized for IV and photoresponse with illumination from the substrate side. The transparency of sapphire and the buffer layers allows for the illumination of the device from the bottom side. Shown in figure 2.26 is the IV characteristic under dark and under 265nm UV illumination. A gain of greater than $3.5 \times 10^3$ was recorded at 75V.
Figure 2.26: a) Reverse bias characteristics of the AlGaN Schottky APD showing the dark current and photoresponse under 265nm UV illumination. b) Gain calculated from the curves in a).
The Al$_{0.4}$Ga$_{0.6}$N APD shows a detection cutoff at 280nm in the solar blind region. Shown in figure 2.27 is the comparison of the spectral response of the GaN and Al$_{0.4}$Ga$_{0.6}$N APD.

![Normalized Spectral Responsivity](image)

**Figure 2.27: Comparison of the normalized spectral responsivity of GaN and Al$_{0.4}$Ga$_{0.6}$N APDs**

The yield of unshorted devices however was poor, with the vast majority of devices showing premature breakdown at a lower voltage. Shown in figure 2.28 is the optical microscope image of an AlGaN APD after premature breakdown; showing visible damage at the edge of the contact. In chapter 4 of this thesis a contact edge termination technique for III-N APDs is discussed to address the issue of premature breakdown at the contact edge.

![Optical Microscope Image](image)

**Figure 2.28: Optical microscope image of an AlGaN Schottky APD (50μm diameter) after premature breakdown, showing damage at the contact edge.**
2.8 Etch pit density in pulsed AlGaN

The optimized AlGaN/AlN/sapphire samples were etched in hot potassium hydroxide at 120°C for 5 minutes and then imaged with an optical microscope and AFM to qualitatively evaluate the surface defect density. As seen in AFM image in Fig. 2.29, post etching, the sample morphology is unchanged in the micro scale (the white points in the AFM are due to particles from the etching solution). However optical microscope images revealed hexagonal pits on the sample surface, these pits have also been seen by other groups[57] and may be due to threading/mixed dislocations and/or open core screw dislocations [58][59]. Defects such as these can lead to device shorting and catastrophic device failure and have also been seen on bulk substrates [60][61].

![Image of optical microscope and AFM images](image)

Figure 2.29 a) Optical microscope image of KOH etched AlGaN/AlN wafer, scale bar in image is 100µm. b) AFM image post etching on a region in between the hexagonal pits.
2.9 Novel defect isolation technique for III-N devices

The detrimental effect of extended defects was described in section 2.1. Density of defects in the grown material can be reduced by the use of bulk substrates, optimized buffer layers and novel epitaxial techniques the number, however defects in the range of $10^5$ to $10^9$ cm$^{-2}$ are still present in III-N films grown on native and foreign substrates. Herein discussed is a novel post-growth technique to isolate electrically conductive defects from the device. A provisional patent has been submitted based on this work [62].

For the sake of clarity, the concept is first demonstrated for nanowire-based devices. Nanowire devices (LEDs, solar cells, photodiodes) typically consist of an array of 2D structures in parallel. Recent research in the growth of III-N nanowires has shown defect reduction in III-N wires due to dislocation bending in bottom-up nanowires grown by selective area epitaxy [63][64][65]. Nanowires fabricated by top down etching of the conventionally grown III-N material also result in a large percentage of the nanowires being free of defects [66].

Figure 2.30: SEM of GaN nanostructures a) grown by bottom up approach [63] and b) fabricated by top down dry etch followed by wet etch [66].
Figure 2.31: TEM of GaN nanostructures a) nanostructure with single threading dislocation and b) dislocation free nanostructures.

Figure 2.32: Simulated current distribution in GaN nanowire array LED in forward bias with one defective nanowire.
The III-N nanowire LED technology is a disruptive technology and boasts several advantages over planar LEDs in terms of current spreading, light extraction efficiency, lower cost of wafer growth, more stable color temperature and other performance parameters [64][65]. However adoption of this technology would require innovative techniques for defect segregation and for device fabrication.

To illustrate the impact of a defective device in a network, shown in Figure 2.32 is a simulation of a GaN Nanowire LED device that is composed of five separate nanowires, one of which is defective (simulated by using a lower bandgap material). The lower turn-on voltage and resistance of the defective nanowire causes funneling of the current into the defective nanowire resulting in non-radiative loss and heat while also decreasing the current in the other healthy nanowires. The defective nanowires also have higher reverse leakage and it is this characteristic that we exploit to isolate them from the defect free ones.

2.9.1 Process details

A large number of devices based on semiconductors are modifications of the simple p-n junction diode and hence the process is illustrated for pn nanowires. Some examples include LEDs, laser diodes, light detectors, bipolar transistors, etc. However the process described here may be applied to planar devices or discrete devices with similar results (Section 2.9.2). The separate nanowire devices (or branches of the device array/network) are first connected with a common electrode. In the case of p-n diodes or similar devices (e.g. LEDs) this could be the n-doped side of the devices or branches. The other ends of the branches or devices (could be the p-doped side in the case of a diode) are connected to long metal strips (figure 2.33a). The device array is then immersed in a metal-ion-electrolyte such that the metal
strips are immersed in the electrolyte and are biased with respect to a common cathode (figure 2.33b).

![Diagram](image)

Figure 2.33: Defective nanowire device isolation process a) p-n nanowire array with one defective device. One terminal of the devices is connected to a common electrode. A metal strip/stack is connected to the second terminal of each of the devices. b) The array is immersed in a metal-ion-electrolytic solution. The common device electrode is biased with respect to an opposing electrode immersed in the electrolyte. With the application of a voltage to the circuit, higher etch rate of the p-contacts will take place for the defective devices. c) Device array (from #b) is shown after formation of the common second electrode. Due to the etching process the defective branch/devices are effectively removed from the array. d) Shows the device with passivation layer(s).

At a certain reverse bias voltage, the defective branches conduct higher current and the metal strips on the defective branches will have higher etch rates and be consumed faster than the
others (as governed by Faraday’s laws of electrolysis; M. Faraday 1834 [67]), thereby shortening their length and effectively removing the defective device from the network (Figure 2.33c).

In place of a simple metal strip, a stack of metals can be used such that at least one of the metals in this stack is preferentially etched away in the electrolyte. In case of nano-devices where attachment of metal strips is difficult to achieve, deposited metal of suitable thickness may be used. Device passivation prior to the etching process may be implemented to prevent unwanted etching damage to the network/device by the electrolyte. Once the defective nanowires have been isolated, a suitable insulating material may be used as a filler material to mask off the etched/shortened metal contacts so as to be able to easily connect the devices in parallel (Figure 2.33d). The individual devices may also be connected to other components (or layers) like resistors before parallel connection.

2.9.2 Experimental Validation

We have shown the feasibility of this novel approach on 1) discrete devices (commercial packaged LEDs), 2) planar devices (GaN Schottky diodes of 2mm diameter) 3) nanoscale Schottky contacts (~500nm diameter).

Shown in figure 2.34a is the experimental setup for the defect selective etch. Two LEDs one of which was made defective by a high current surge were prepared for defect selective etch by soldering metal strips to the p-contact terminal. Shown in figure 2.34b and c the results of defect selective etch with the defective LED having the shorter metal strip.

The process was also explored for large diameter (2mm) Schottky diodes on GaN/Sapphire and using the defected device isolation technique, devices with lower breakdown voltage and higher leakage current are selectively etched off.
The process was also explored on the nanoscale by the use of self assembled nickel nano-islands on top of the Schottky structure followed by defect etching and it was observed that some of the metal islands were etched off while the others were untouched. Given the defect

Figure 2.34: Experimental validation a) schematic setup for discrete LED network etching, b) and c) show the leads of the LEDs before and after etching with the defective LED having a shorter metal strip. d) results of the defect selective etch on a GaN Schottky device wafer, e) SEM of defect selective etch of a GaN Schottky diode with nickel nano-islands.

The process was also explored on the nanoscale by the use of self assembled nickel nano-islands on top of the Schottky structure followed by defect etching and it was observed that some of the metal islands were etched off while the others were untouched. Given the defect
density of the wafer $\sim 2.5 \times 10^8$ cm$^{-2}$, the average spacing between the defects is $\sim 500$nm and is of the same range as the size and spacing of the metal islands ($\sim 500$nm); due to which some of the islands can be expected to be completely free of defects. The SEM micrograph in figure 2.34e of the Schottky wafer after the etching process shows selective etching of some of the islands while the neighboring islands are intact. By connecting the unetched islands in parallel it is conjectured that a defect free device can be realized, but the process methodology for this is yet to be realized.

In summary, we have demonstrated that the defect etching technique can be used for defective device isolation at the wafer level, component level and nanoscale level. It is at the nanoscale level that this technology can be expected to make the biggest impact to system performance. To this end the process is currently under development to be able to isolate defective areas in LEDs and APD structures.

### 2.10 Chapter references


Chapter 3

Reduction of sidewall leakage using ALD aluminum oxide passivation

The work presented in this chapter was led by John Hennessy et al. at JPL and is the topic of the paper [1], the samples for the study were grown and some of the measurements performed at CNSE.

The sidewalls of the III-N mesa etched devices play a crucial role in device yield and performance. While the bulk defect density of III-N devices can be reduced by the use of high quality bulk substrates, the creation of defects on the sidewalls is inevitable due to the nature of the III-N dry etching process that results in structural damage and unsatisfied dangling bonds.

The sidewalls form a continuous path from between the contacts and can cause high leakage currents due to conduction from defects and surface states. The sidewalls of the device can also lead to microplasma effects and premature breakdown before the bulk of the device
reaches the critical field, for these reasons it is absolutely critical to minimize the impact of sidewalls on device performance.

A number of techniques have been explored to reduce sidewall impact on III-N APDs, namely wet etching [2], photoelectrochemical etching [3], PECVD silicon nitride passivation [4], PECVD silicon dioxide passivation [5] and double mesa etching technique [6].

In this work, we have developed two new techniques for effective sidewall impact reduction namely, Atomic layer deposition (ALD) of aluminum oxide sidewall passivation and Argon ion implantation based edge termination. The first technique is highly effective in reducing sidewall leakage and trap density while the second technique (discussed in the next chapter) reduces the electric field at the contact edges and sidewall, preventing premature breakdown while reducing the leakage current.

Figure 3.1: Leakage current paths in p-i-n III-N APDs
3.1 Sidewall creation by mesa etching

The vertical nature of the vast majority of III-N devices, necessitates mesa etching for both current confinement and device to device isolation. There has been very little success with the wet etching of III-Ns [7] and has been found to be extremely dependent on the defect density and the nature of the exposed planes of the film. Strong bases such as potassium hydroxide have been seen to etch Ga-polar GaN at slow rates, and at a much higher rate at defect locations, and as such are useful in defect characterization[8]. Given the need for uniform anisotropic etching of III-Ns for device fabrication, dry etching techniques have been developed.

3.1.1 Inductively coupled plasma etching

The Inductively couple plasma (ICP) etching technique for III-N makes use of both chemical reaction and physical sputtering to be able to get a high etch rate and anisotropic
etching with smooth sidewalls. In an ICP system, a RF power supply is used to generate a high density plasma in the center of the chamber (figure 3.2) and the ion energy is controlled by a separate power supply that biases the substrate. This allows for independent control of ion density and ion energy. Chlorine is the most commonly used gas for GaN ICP etching due to the high volatility of its reaction byproducts, the addition of Boron Tri-Chloride to the plasma has been seen to result in smoother etched surfaces[9][10]. The ICP power and the RIE power need to be optimized to get smooth etched surfaces without pits or pillars (figure 3.3).

Figure 3.3: Impact of ICP and RIE power on etched surface morphology [27]
3.1.2 Sidewall leakage

The etch rate of GaN in typical ICP process is in the range of 200-300nm/min, in spite of these low etch rates significant plasma damage occurs due to the ion bombardment which can deteriorate the optical and electrical properties of the material[11]–[13]. Furthermore the sidewalls of the mesa-etched features can develop traps, vacancies, defects, dislocations and dangling bonds that can lead to significant leakage currents.

![Diagram of sample and electrical setup for measurement and current vs voltage plot showing the currents from the outer and the inner contacts under reverse bias](image)

Figure 3.4: a) Sample and electrical setup for measurement and b) current vs voltage plot showing the currents from the outer and the inner contacts under reverse bias [14]

Shown in figure 3.4a is the sample setup from reference [14], which shows a mesa etched GaN pn diode where the top p-contact is divided into an inner and outer region, and currents from the two contacts is measured separately. As can be seen in figure 3.4b, the reverse current from the outer contacts close to the sidewall is many orders of magnitude higher than that from the inner contact. This clearly demonstrates the need for techniques to reduce sidewall leakage for mesa etched III-N devices. Given that III-N avalanche photodiodes require very
high voltages (~100V) for operation, the leakage current from the untreated sidewalls can be very high, limiting the signal to noise ratio of the APD. Some of the commonly used methods to reduce sidewall leakage current in III-N devices are smoothing of the sidewalls by the use of wet chemical etching [15] that has been shown to be capable of etching away defective material at the sidewalls, resulting in smoother sidewalls (figure 3.5) and has been shown to reduce leakage current (figure 3.6) [16].

### 3.1.3 Sidewall passivation

The other commonly used technique for sidewall leakage reduction is sidewall passivation by the deposition of an insulating material on the sidewalls.

![Figure 3.5: AFM profile of sidewall before and after wet chemical etching[15].](image)

![Figure 3.6: Dark current in AlGaN APDs before and after wet chemical treatment [16].](image)
Silicon dioxide and silicon nitride are the commonly used sidewall passivation materials using plasma enhanced chemical vapor deposition (PECVD). Shown in figure 3.7 is a schematic of a PECVD setup[17].

![Figure 3.7: Schematic of a plasma enhanced chemical vapor deposition tool for silicon dioxide deposition [17].](image)

By the use of plasma activation of the source species namely silane and nitrous oxide, the temperature of the silicon dioxide deposition can be brought down to the 300C range, enabling the deposition of conformal silicon dioxide on patterned III-N surfaces with or without metal contacts. The reaction is as follows.

\[
3SiH_4 + 6N_2O \rightarrow 3SiO_2 + 4NH_3 + 4N_2
\]
3.2 Development of alumina sidewall passivation using atomic layer deposition

Atomic layer deposition (ALD) was originally developed in the 70’s for the deposition of metal thin films [18], but is now widely adopted for the deposition of dielectric thin films[19][20]. ALD is a chemical vapor deposition technique in which the precursors are sequentially injected with inert purges in between, this enables a layer by layer growth.

The first precursor is injected into the reactor, it adsorbs on the substrate forming a monolayer, an inert gas purge is sent into the chamber to remove any excess reactants and then the next precursor is injected into the chamber which reacts with the adsorbed monolayer to form the

Figure 3.8: Schematic of a remote plasma atomic layer deposition tool[21].

The first precursor is injected into the reactor, it adsorbs on the substrate forming a monolayer, an inert gas purge is sent into the chamber to remove any excess reactants and then the next precursor is injected into the chamber which reacts with the adsorbed monolayer to form the
binary material. Another inert gas purge is done to get rid of the reaction byproducts and excess reactants and the process repeats.

ALD is a self-limiting process; the thickness of the deposited material is dictated by the number of ALD cycles and not by the pulse durations as long as it is sufficient to deposit one monolayer. This allows for extremely controlled and repeatable deposition process.

Many variants of the ALD process and tools exist, for this work, the Oxford Opal ALD system [21] was employed. This tool is equipped with a remote plasma source (shown in Figure 3.8) that enables deposition at low temperatures (~300°C). For the deposition of aluminum oxide using ALD, the commonly used precursors are trimethyl-aluminum for the aluminum source and water or ozone[22] for the oxygen source. For this work we use trimethyl-aluminum and oxygen plasma as the precursors for the deposition of aluminum oxide.

![Figure 3.9: Sequence of the ALD cycle for the deposition of aluminum oxide [21].](image)

Shown in figure 3.9 is the cycle sequence for ALD aluminum oxide deposition. In step-1, trimethyl-aluminum (TMAI) is injected into the chamber causing it to adsorb at the reaction sites. Next in step-2 an inert gas purge step is employed to remove any the unabsorbed
reactants and byproducts. In step 3 plasma cracked oxygen (or H$_2$O in the case of high temperature process) is injected into the chamber to react with the adsorbed aluminum precursor to form aluminum oxide. Finally in step 4 an inert gas purge is used to clear away the reaction byproducts and preparing the surface for the next TMAl pulse.

Below are the process details for the ALD $Al_2O_3$ process developed at JPL for the III-N APD passivation described in this work:

Step 1: TMAl pulse, 30ms

Step 2: Argon purge, 30sccm for 5s

Step 3: Oxygen plasma at 300W, 40sccm for 6s

Step 4: Argon purge, 30sccm for 3s

The substrate temperature was maintained at 300°C and the growth rate was 1A/cycle, the cycle was repeated 300 times to reach the thickness of 30nm used in this work.

3.2.1 Experiment details

GaN APDs were grown on sapphire substrate as described in section 1.6. The APD structures were fabricated with mesa etch up to the n-layer and Ti/Al/Ni/Au n-contact and thin transparent Ni/Au p-contact deposition. Following which, each sample was passivated with different passivation layers, the fabrication was completed with the p-contact and bondpads and the performance of the APDs were compared [1].
Sample Name | Passivation Layer
--- | ---
Sample A | 700nm SiO$_2$
Sample B | 32nm Al$_2$O$_3$ + 700nm SiO$_2$

Figure 3.10: Sample description for the passivation study

Figure 3.11: Cross-section schematic of samples for the passivation study [1]

Sample-A was fabricated with the conventional PECVD silicon dioxide passivation grown at 345C and serves as the control sample for this study. Sample-B was fabricated with a 32nm ALD grown aluminum oxide at 300C layer and capped with 700nm PECVD silicon dioxide (as shown in figure 3.11).

### 3.2.2 Dark current measurement

Devices with diameters ranging from 10μm to 100μm were characterized for dark current using a HP4156C semiconductor parameter analyzer. The dark currents closer to the avalanche voltage exhibited a large variation as much as six orders of magnitude within each sample (see figure 3.12). Hence to make meaningful conclusions a large number of devices were characterized.
Figure 3.12: Variation in dark current for 10μm diameter APDs on (a) Sample A with PECVD SiO$_2$ passivation and b) Sample B with ALD Al$_2$O$_3$ passivation
Figure 3.13: Histogram showing dark current at 60V reverse bias on 25μm diameter APDs in (a) Sample A with PECVD SiO$_2$ passivation and b) Sample B with ALD Al$_2$O$_3$
The improvement in device dark current density by the use of ALD $\text{Al}_2\text{O}_3$ passivation can be clearly seen in the histogram where ALD $\text{Al}_2\text{O}_3$ passivated devices show a lower median dark current density compared to PECVD $\text{SiO}_2$ passivated devices. The ALD $\text{Al}_2\text{O}_3$ passivated APDs also show fewer shorted devices (Column 0), have lower average leakage current and also the devices with the lowest leakage current ($\sim 0.01\text{nA}$) in the series. A large sample set of 25$\mu$m devices were also measured, shown in Figure 3.14 is a histogram comparison of devices, here an improvement of 92% is seen in the median dark current for the ALD $\text{Al}_2\text{O}_3$ passivated APDs.

![Histogram showing dark current at 60V reverse bias for 200 APDs of 25$\mu$m diameter with ALD Al$_2$O$_3$ passivation (in red) and PECVD SiO$_2$ passivation (in white)]

Figure 3.14: Histogram showing dark current at 60V reverse bias for 200 APDs of 25$\mu$m diameter with ALD Al$_2$O$_3$ passivation (in red) and PECVD SiO$_2$ passivation (in white)[1]

The improvement in dark current density with respect to device diameter is shown in figure 3.15. It can be seen that the improvement in dark current density through the use of ALD $\text{Al}_2\text{O}_3$ is carried over even with increasing device diameter. However it is seen that percentage improvement in the median dark current density is lower at higher device diameters with an improvement of 92% for 25$\mu$m devices and compared to only 61% for 100$\mu$m devices.
This is mostly due to the fact that the increase in bulk leakage due to increase in device area is proportional to the square of the mesa diameter whereas the increase in sidewall leakage from the perimeter is proportional to the diameter only, such that the contribution of the sidewalls to the dark current is higher for lower diameter devices, hence this is where the ALD $\text{Al}_2\text{O}_3$ passivation shows the highest benefit.

A sharp reduction in median dark current density is seen for small devices along with an increase in standard deviation of the dark current, this is indicative of the role of bulk defects, when the device dimensions is comparable to the mean separation between the defects.

The improvement in the median and average leakage current in III-N APDs of all diameters through the use of atomic layer deposition of aluminum oxide suggests an improvement in the sidewall interface of the mesa etched material. To understand this further MOS capacitors were fabricated using ICP etched n-GaN as one electrode, ALD or PECVD deposited dielectric and metal contact as the other electrode, and their Capacitance Voltage behavior was studied.

Figure 3.15 Diameter dependence of APD median dark current density at 60V reverse bias with ALD $\text{Al}_2\text{O}_3$ passivation (in red) and PECVD $\text{SiO}_2$ passivation (in blue)[1]
3.3 Capacitance voltage characterization of interface traps

Structural defects, dangling bonds and impurities at interfaces can lead to traps at the interface of the semiconductor and dielectric. Capacitance voltage characterization of a metal oxide semiconductor (MOS) interface using a dc + ac bias can be used to probe the traps at the interface.

![Figure 3.16 Equivalent circuit of the capacitances in the MOS system](image)

Figure 3.16 Equivalent circuit of the capacitances in the MOS system

Shown in figure 3.16 is the equivalent circuit of the capacitances in the MOS system, Here $C_{ox}$ is the oxide capacitance, $C_n$ is the capacitance associated with the conduction band electron charge density, $C_p$ is the capacitance associated with the bulk charge density due to the space charge, $C_p$ is the capacitance associated with the hole charge density and $C_{it}$ is the capacitance due to the interface charge.

For positive voltages on the metal gate, the semiconductor surface (n-type GaN in this case) is heavily accumulated and hence $C_n$ dominates the parallel capacitance network. The total capacitance of the network is now given by the series combination of $C_{ox}$ and $C_n$. (see figure
3.17) Since $C_{ox}$ is much smaller than $C_n$, the equivalent capacitance of the network is governed by $C_{ox}$ and does not show a voltage dependence (In a series capacitor network, the effective capacitance is lower than the lowest capacitance in the network). Hence $C_{ox}$ can be measured by biasing the device in accumulation. The series resistance (or conductance) of the device can also be measured in this mode.

Figure 3.17 Simplified equivalent circuit of the MOS capacitance under accumulation

Figure 3.18 Simplified equivalent circuit of the MOS capacitance under depletion
When a negative bias is applied on the metal gate, the surface of the semiconductor is depleted and the capacitances due to the space charge in the semiconductor and the oxide-semiconductor interface charge dominate the parallel network. The equivalent circuit of the network can be approximated as $C_{ox}$ in series with $C_b + C_{it}$ as shown in figure 3.18.

### 3.3.1 CV characterization of etched-nGaN MOS capacitors

In order to study the behavior of the passivation layers on III-N APDs, etched n-GaN/passivation interface MOS capacitors were fabricated with dry-etched n-GaN as the bottom electrode, 25nm of PECVD $SiO_2$ as dielectric for the Siilica MOS cap and 45nm of $Al_2O_3$ as dielectric for the Alumina MOS cap and were capped with 5nm Ti/250nm Au contacts to complete the MOS structure. The thickness of the dielectrics in the two MOS cap structures were chosen to compensate for the difference in dielectric constants of the two materials so as to achieve similar equivalent electrical thickness.

Figure 3.19: CV characteristic of etched n-GaN MOS capacitors using (a) PECVD $SiO_2$ dielectric and (b) ALD $Al_2O_3$ dielectric [1]
Shown in figure 3.19 is the high frequency CV characteristic of the two MOS capacitor systems. It can be seen here that compared to the $Al_2O_3$ MOS capacitor, the $SiO_2$ capacitor shows significantly higher DC stretch-out, hysteresis and frequency dispersion, indicative of higher charge trapping.

The charge balance in a MOS capacitor system under depletion can be written as

$$\delta Q_G = -(\delta Q_{it} + \delta Q_b)$$  \hspace{1cm} (3.1)

Where $\delta Q_G$ is the change in gate charge due to change in the gate voltage, and $\delta Q_{it}$ and $\delta Q_b$ are the changes in the interface charge and depletion charge respectively. For the same change in the gate charge, interfaces with high trap density result in high $\delta Q_{it}$ and consequently lower $\delta Q_b$ as per equation 3.1, causing lower band bending in the semiconductor. This results in a stretch out of the CV characteristic along the gate bias axis as seen prominently in the $SiO_2$ MOS capacitor (figure 3.19a).

### 3.3.2 Conductance method for calculation of $D_{it}$

In order to quantify the reduction in interface state density ($D_{it}$), the Conductance method is used. Shown in figure 3.20 is the equivalent circuit of the MOS capacitor for conductance measurement. $C_{ox}$ is the oxide capacitance, $C_s$ is the semiconductor capacitance and $C_{it}$ is the interface trap capacitance. The energy loss in the traps is modeled by a series resistance $R_{it}$. In order to simplify the MOS circuit we need to combine the capacitances $C_s$
and $C_{lt}$ (shown in figure 3.20 a and b) in the parallel branches into a single entity $C_p$. To do this we model the branches as parallel impedances.

**Figure 3.20** (a) MOS Capacitor circuit elements with the interface traps modelled as a resistor and capacitor in series (b) simplified circuit for conductance measurement and (c) equivalent circuit showing the measured capacitance and conductance

Impedance of the $C_s$ branch is given by

$$1/Z_s = j\omega C_s$$  \hspace{1cm} 3.2

Impedance of the $C_{lt}$ and $R_{lt}$ branch is given by

$$1/Z_{lt} = 1/(R_{lt} + 1/j\omega C_{lt})$$  \hspace{1cm} 3.3
Here $\omega = 2\pi f$ and $f$ is the frequency of the ac bias used for measurement; $C_{it} = qD_{it}$ and $\tau_{it} = R_{it}C_{it}$ is the interface trap time constant.

From equation 3.2 and 3.3 we can compute the equivalent impedance $Z_e$ of the parallel network using

$$1/Z_e = 1/Z_s + 1/Z_{it}$$  \hspace{1cm} 3.4

Substituting for $Z_s$ and $Z_{it}$ from equations 3.2 and 3.3 in equation 3.4 we get

$$\frac{1}{Z_e} = j\omega C_s + \frac{1}{R_{it} + 1/j\omega C_{it}}$$  \hspace{1cm} 3.5

On simplifying and substituting for $\tau_{it} = R_{it}C_{it}$, we get

$$\frac{1}{Z_e} = j\omega C_s + \frac{j\omega C_{it}}{1 + j\omega \tau_{it}}$$  \hspace{1cm} 3.6

Multiply both numerator and denominator of second term by $(1 - j\omega \tau)$

$$\frac{1}{Z_e} = j\omega C_s + \frac{j\omega C_{it}(1 - j\omega \tau_{it})}{1 + j\omega \tau_{it}(1 - j\omega \tau_{it})}$$  \hspace{1cm} 3.7

On simplifying and separating the real and imaginary terms, we get

$$\frac{1}{Z_e} = j\omega C_s + \frac{j\omega C_{it}}{1 + \omega^2 \tau_{it}^2} + \frac{\omega^2 C_{it} \tau_{it}}{1 + \omega^2 \tau_{it}^2}$$  \hspace{1cm} 3.8
On simplifying and substituting for $D_{lt}$

\[
\frac{1}{Z_e} = j\omega (C_s + \frac{C_{lt}}{1 + \omega^2 \tau_{lt}^2}) + \frac{\omega^2 qD_{lt} \tau_{lt}}{1 + \omega^2 \tau_{lt}^2} \tag{3.9}
\]

The equivalent impedance can now be modeled as an equivalent capacitance $C_p$ in parallel with an equivalent conductance $G_p$ and can now be represented by the equivalent circuit shown in figure 3.19 b.

\[
\frac{1}{Z_e} = j\omega C_p + G_p \tag{3.10}
\]

Where:

\[
C_p = C_s + \frac{C_{lt}}{1 + \omega^2 \tau_{lt}^2} \tag{3.11}
\]

and

\[
\frac{G_p}{\omega} = \frac{\omega q \tau D_{lt}}{1 + \omega^2 \tau_{lt}^2} \tag{3.12}
\]

By measuring the conductance versus frequency and plotting $G_p/\omega$ vs $\omega$ we can calculate $D_{lt}$ easily at the maxima of equation 3.12 when $\omega = 1/\tau_{lt} = \omega_{max}$. This simplifies equation 3.12 to

\[
D_{lt} = \frac{2G_p}{q\omega_{max}} \tag{3.13}
\]
Equations 3.12 and 3.13 allow us to calculate $D_{lt}$ by measuring the frequency dependence of the parallel conductance $G_p$. More complex forms of the above relation may be reached by accounting for the distribution of traps, fluctuations in surface potential and factoring out the impact of series resistance as described in references [23][24][25].

Shown in figure 3.21 is the equivalent parallel conductance ($G_p/\omega$) derived from the measured conductance vs frequency curves after compensating for the series resistance (measured when device is biased in accumulation). The difference in bias ranges for the two devices is due to the difference in flat-band voltage and dc stretch-out as seen in the CV curves of figure 3.19.

The conductance characteristics of the $SiO_2$ MOS capacitor shows significant distortion due to the DC stretch out (as seen in the CV curves of figure 3.19) compared to the $Al_2O_3$ MOS capacitors which show clear peaks in the $G_p/\omega$ vs $\omega$ characteristic. A $D_{lt}$ of $>1x10^{13}$ eV$^{-1}$ cm$^{-2}$ was calculated for the $SiO_2$ MOS capacitor compared to lower than $2x10^{12}$ eV$^{-1}$ cm$^{-2}$ for the ALD $Al_2O_3$ capacitors.

Figure 3.21 $G_p/\omega$ vs $\omega$ characteristic of etched n-GaN MOS capacitors using (a) PECVD $SiO_2$ dielectric and (b) ALD $Al_2O_3$ dielectric[1]
Figure 3.22: Current hysteresis during voltage cycling of passivated APD devices using (a) PECVD SiO$_2$ dielectric and (b) ALD Al$_2$O$_3$ dielectric
In summary the use of aluminum oxide ALD passivation for III-N APDs shows promise in lowering the leakage current, reducing charge trapping and hysteresis due to the impact of the sidewall and shows substantial improvement over conventionally grown PECVD silicon dioxide sidewall passivation. The ALD $\text{Al}_2\text{O}_3$ passivated GaN/Sapphire p-i-n APDs in addition to lower leakage currents, show a reduction in the hysteresis and drift of the IV curve after avalanche breakdown (figure 3.22). A few of the ALD passivated devices still show considerable hysteresis pointing to the presence of other types of defects and traps in the bulk. High fields at the edges of the contacts are also suspected to play a role.

3.4 Chapter references


Chapter 4

Improving APD reliability and reducing dark-current by Ar$^+$ ion implanted edge termination

4.1 Edge breakdown in high voltage devices

III-N materials due to their wide bandgap nature and other electrical properties are finding increasing use in power semiconductor applications that are dominated by silicon and silicon carbide semiconductor devices[1][2]. The two most important III-N power devices namely, the high electron mobility transistor (HEMT)[3][4] and GaN power Schottky diode[5][6] have been extensively researched and have recently entered commercial production[7][8]. Power semiconductor devices are designed to have high breakdown voltages, however one of the common problems with high power devices is the spiking of the electric field at the edges of the contact leading to high leakage[9], premature breakdown[10] and

![Schottky contact](image1)

![SEM micrograph](image2)

![Optical image](image3)

**Figure 4.1:** a) Edge breakdown in SiC Schottky device showing light emission from a sharp point on the contact edge[12], b) SEM micrograph of GaN diode on HVPE substrate after premature breakdown, showing damage to the metal contact on the edges[11], and c) Optical image of AlGaN Schottky APD after premature breakdown.
To counter this, a number of techniques like passivation, guard rings and field plate have been developed for power devices[13][14]. Similar techniques may be adopted for III-N APDs as well, since they too are required to go to high voltages with high reliability and low leakage.

Figure 4.2: GaN Schottky diode a) structure, b) simulated electric field distribution at 150V reverse bias and c) zoomed in image of (b) at the Schottky contact edge.
Shown in figure 4.2 is the simulation of the electric field profile in a typical GaN Schottky barrier diode structure. The structure has a 200nm thick n-type layer with a carrier concentration of $2 \times 10^{18}$ cm$^{-3}$ and a 350nm drift layer of undoped GaN (background electron concentration of $1 \times 10^{16}$ cm$^{-3}$). The diode has a continuous ohmic contact at the bottom and a patterned Schottky contact on top of the mesa. As can be seen in figures 4.2 b) and c) the electric field profile at the high reverse voltage shows field crowding at the contact edges (perimeter of the contact) due to the sharp potential gradient at the contact edges. This causes a localized hotspot of high electric field at the contact edges while the bulk of the drift region is still below the critical field for breakdown. The high field at the contact edges can cause increased leakage current, premature breakdown and damage to the device. The premature breakdown from the edges of the contact prevents taking the bulk of the diode to the critical electric field without causing damage to the device (along the contact perimeter where the field would be much higher than the critical field).

A similar effect is also seen in p-i-n diodes at high reverse bias. Shown in figure 4.3 is the simulation of a 1μm diameter p-i-n diode. The horizontal dimension of the device has been kept small to minimize the simulation time, but is sufficient to show the field distribution and crowding in the device and is representative of the effect that can be expected to be seen in larger scale. The device structure is composed of 200nm n-type GaN with a carrier concentration of $2 \times 10^{18}$ cm$^{-3}$, 350nm of undoped GaN with a electron concentration of $1 \times 10^{16}$ cm$^{-3}$ and 300nm of p-type GaN with a hole concentration of $4 \times 10^{17}$ cm$^{-3}$. As can be seen in the graph on figure 4.3c, the electric field at the contact edges is about 4 times larger than that below the contact in the bulk region and can be detrimental to the device performance of p-i-n diodes and APD structures.
Figure 4.3: GaN p-i-n diode a) structure b) simulated electric field distribution at 150V reverse bias and c) 1-D horizontal section of the electric field below the p-contact.
4.2 Edge termination for high power devices

A number of techniques have been developed for the reduction of the electric field crowding at the contact edges, particularly for Si power devices and more recently for SiC high voltage devices and GaN Schottky diodes on bulk GaN[15]. Some of the techniques are discussed here.

4.2.1 Field Plate

![Field plate based edge termination](image)

Figure 4.4: Field plate based edge termination in a) GaN Schottky diode [16] and b) AlGaN/GaN power HEMT [17].
The field plate edge termination scheme in its simplest form consists of the edge of the metal contact overlapping a dielectric material (typically silicon dioxide or silicon nitride) as shown in figure 4.4a [16]. GaN Schottky[16], pn[9] and HEMT[17] devices with field plate based edge termination have been developed and have shown an improvement in the breakdown voltage and leakage current.

From the simulations done by the authors in reference [16], it can be seen that the breakdown voltage increases with metal overlap due to the increase in lateral spread of the depletion layer away from the contact edge. However beyond a certain overlap distance, when the lateral spread of the depletion region is comparable to the vertical distance, the breakdown voltage saturates[18]. This design requires careful choice of the dielectric material and thickness such that it can cause a lateral spread of the depletion layer in the semiconductor without the dielectric itself breaking-down due to the field exerted on it. The breakdown voltage can be further improved by the use of an optimized beveled field plate or a multistep field plate [19].

Figure 4.5: Edge termination for GaN Schottky diodes a) Beveled dielectric and b) Multi step field plate [19].
4.2.2 Ion implanted edge termination

Recently Baliga et al. reported on the use of argon ion based edge termination for GaN Schottky diodes on bulk GaN substrate. In this technique argon ions are implanted in the periphery of the contact edge creating a highly resistive region that spreads the potential along the surface thereby reducing electric field crowding\[10\]. This is similar to the technique used in SiC power devices except that an ion dose one order of magnitude higher is needed in GaN to create a resistive region compared to SiC [20][21].

![Schematic of SiC Schottky diode with ion implanted edge termination and Increase in breakdown voltage with ion dose](image)

Figure 4.6: a) Schematic of SiC Schottky diode with ion implanted edge termination and b) Increase in breakdown voltage with ion dose [21].
4.3 Development of argon ion implanted edge termination for III-N p-i-n avalanche photodiodes

Given the similar nature of the field crowding problem in both Schottky and p-i-n devices, it was our conjecture that the ion implantation Schottky contact edge termination technique could also be applied to p-i-n III-N APDs. To the best of our knowledge, at the time of this writing, the argon ion-implanted edge termination technique has not been reported for III-N p-n or p-i-n devices.

4.3.1 Ion implanter setup

Ion implanters are commonly used in semiconductor fabs to implant dopants into silicon [22]. Shown in figure 4.7 is the schematic of the Extrion 400-10P ion implanter [23] that was used for this work.

![Schematic of the Extrion 400-10P ion implanter.](image)

Figure 4.7: Schematic of the Extrion 400-10P ion implanter.
Ions are created by a plasma source and then pass through an analyzer magnet that allows the selected ion (argon in this case) to pass through and stops the rest of the ions, based on their different masses. The ion energy can be controlled by the voltage that is applied to the acceleration column and the ion dosage may be controlled by the variable slit and the implantation time. X and Y deflection plates allow the beam to be rastered across the sample stage to cover the entire sample. The ion energy and dosage used for the experiments were chosen based on TRIM (Transport of Ions in Matter [24]) simulations. TRIM makes use of Monte Carlo statistical techniques and quantum mechanical treatments of the collisions of ions and atoms to predict the trajectory of the implanted species in the target material. Shown in figure 4.8 are the results of the TRIM simulation for the implantation conditions used in our experiments, namely an ion energy of 75keV with a dosage of $2 \times 10^{16}$ cm$^{-2}$ on the surface of GaN. As can be seen from the concentration profile (figure 4.8a), the peak concentration is found at a depth of approximately 45nm from the GaN surface.

Figure 4.8: TRIM simulation showing the a) concentration of argon ions vs depth from the GaN surface and b) lateral and vertical spread of the argon ions from point ion-source (shown by the blue arrow) on the GaN surface.
The implantation profile from a point source of ions, in addition to having a depth profile also has lateral penetration and spread (figure 4.8b). This is not of much consequence in the bulk of the implanted region, however in regions close to and under the implantation mask (p-contact metal in our case) penetration of the implant ions upto a lateral distance of approximately 50nm can be expected.

4.3.2 Experiment details

Shown in figure 4.9 is the structure of the sample used in this study. The structure was grown on double side polished sapphire substrate so as to be capable of back illumination. To be able to achieve back illuminated photodiodes, it is essential to grow the device stack on transparent buffer layers (like AlGaN or AlN) or utilize extremely thin GaN buffer layers to minimize absorption of the wavelength(s) of interest outside of the absorption/multiplication region.

```
<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
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<tr>
<td>p-GaN (300nm)</td>
<td></td>
</tr>
<tr>
<td>u-GaN (350nm)</td>
<td></td>
</tr>
<tr>
<td>n-GaN (200nm)</td>
<td></td>
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<tr>
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<tr>
<td>AlN Buffer (35nm)</td>
<td></td>
</tr>
<tr>
<td>DSP Sapphire</td>
<td></td>
</tr>
</tbody>
</table>
```

Figure 4.9: Device structure of the p-i-n sample for the ion implanted edge termination study.
To this end, a thin optimized 35nm AlN and 20nm undoped GaN layer were used as the buffer layers for these devices. The optimized AlN + GaN buffer layer enables the growth of high quality GaN without the need for the 2-4μm thick template layer used conventionally. Shown in figure 4.10 are the AFMs where it can be seen that the GaN grown on the thin buffer structure has a quality comparable to the conventional 4μm thick GaN template.

(a)
(b)

Figure 4.10: AFM of GaN surface on a) DSP sapphire with thin AlN/GaN buffer layer and b) SSP sapphire with 4μm thick layer

The wafer was patterned with circular metal contacts comprising of 120nm Ni/50nm Au using image-reversal photolithography, e-beam evaporation and lift-off. The metal contacts serve as both the implantation mask and as the p-Contact for the devices. Next the sample was implanted with Argon ions with energy 75keV and a dosage of $2 \times 10^{16}$ cm$^{-2}$. A p-i-n control sample was also prepared without implantation. The samples were then patterned and ICP etched to realize circular mesas with diameter larger than the p-Contact. This was followed by lithographic patterning and deposition of 80nm Ti/50nm Au n-contact metal stack. Finally the samples were passivated with 200nm PECVD silicon dioxide and windows were opened.
for probing. TRIM simulations were also done to check for the penetration of ions through the metal mask and it was found that the metal stack used in the experiments, namely 120nm Ni /50nm Au and was more than adequate to stop the penetration of the ions through the metal.

4.3.3 Experimental results of p-i-n devices

The fabricated devices were characterized for current-voltage using a Keithley 6430 sourcemeter. Shown in figure 4.11a is the comparison of the reverse currents (under dark conditions for a typical 20μm diameter device on the standard (unimplanted) and the implanted samples.

The standard sample (blue curve in figure 4.11a) shows higher leakage and premature breakdown (in a large majority of the devices). The current also shows random fluctuations during the voltage sweep indicative of higher noise in the devices. The premature breakdown of the device also leads to the device being shorted, as can be seen in the repeat scan shown in figure 4.11b which shows the device current reaching the current limit at a low voltage (4V) in the second current-voltage scan of the device.

The implanted samples on the other hand (red curve in figure 4.11a) show lower leakage current and lower noise without premature breakdown. The implanted samples also show improved reliability and UV-photoresponse as can be seen in figure 4.11c which shows the dark current and photoresponse characteristic under 360nm UV illumination from the back-side of the wafer.
Figure 4.11: Measured reverse current voltage characteristics showing a) comparison of standard and implanted device and b) result of a subsequent IV scan of the standard device indicating a shorted device c) dark current and 360nm UV photoresponse in the implanted sample.
4.3.4 Simulation of p-i-n devices

In order to understand the improvement in device characteristics in the implanted samples, the devices were modeled using Sentaurus TCAD and the electric field profile in the devices were studied. The implanted regions were simulated by the addition of a single midgap acceptor level to the p-doped GaN as described in reference [25].

Figure 4.12: GaN p-i-n diode with ion implanted edge termination a) structure b) simulated electric field distribution at 150V reverse bias and c) 1-D horizontal section of the electric field below the p-contact.
As can be seen in the simulated electric field profile in figure 4.12, the electric field for the edge implanted sample shows much smaller peaks at the contact edges compared to the standard sample which was shown in figure 4.3c. The reduction in field crowding at the edges (perimeter) of the contact leads to superior device characteristics with no premature breakdown.

4.3.5 Experimental results of p-i-n-i-n devices

To further explore the impact of the ion implanted edge termination, p-i-n-i-n structures were grown and fabricated in similar fashion with a standard unimplanted sample and argon ion implant edge terminated sample. Shown in figure 4.13 is the structure of the sample. The 350nm intrinsic region serves as the absorption region and the 180nm intrinsic region serves as the multiplication region for these devices when illuminated from the bottom.

![Device structure for the p-i-n-i-n sample for the ion implanted edge termination study.](image-url)
Figure 4.14: Measured reverse current voltage characteristics of 20μm diameter devices showing a) comparison of standard and implanted device, b) 360nm UV photoresponse in the implanted sample and c) gain in the implanted sample.
As can be seen from figure 4.14a, the implanted p-i-n-i-n devices show lower leakage current compared to the standard unimplanted sample (similar to the p-i-n devices). The implanted samples show breakdown around 120V with a gain of close to 40,000 under 360nm UV illumination. The breakdown characteristic is less steep compared to p-i-n devices discussed in section 1.6, due to the larger 350nm thick intrinsic region used in the device that slows down the rate of increase of electric field with voltage.

### 4.3.6 Simulation of p-i-n-i-n devices

![Electric field simulations](image)

**Figure 4.15:** Simulated Electric field profile at -130V in the p-i-n-i-n a) Standard device, and b) Argon ion edge implanted device.

Shown in figure 4.15 are the simulated field profiles for the p-i-n-i-n structure of figure 4.11. As can be seen from the electric field simulations shown in figures 4.15, the standard unimplanted p-i-n-i-n sample shows a high degree of field crowding at the contact edges, when compared to the ion-implant edge terminated sample. The field crowding can be seen more clearly in figure 4.16, the zoomed-in electric field at the contact edge for both the devices.
Shown in figure 4.17 is the 1-D horizontal section of the electric field below the contacts, here it can be seen that for the standard unimplanted sample, the electric field at the edges is more than eight times higher than that in the bulk of the sample under the p-contact and is clearly past the critical electric field for GaN (which is estimated at 3MV/cm). It can also be seen
that, within the bulk of the sample both the standard and the implanted sample have the same electric field implying that the effect of the implantation is localized to the contact perimeter.

![Electric Field Diagram](image)

**Figure 4.17:** 1-D horizontal section of the electric field below the p-contact for the standard unimplanted sample in blue and for the implanted sample in red

Initially the implanted device was simulated with the implanted regions starting from the edge of the contact and extending up to the edge of the mesa, these structures did not show a significant reduction in the electric field spike at the edges of the contact. The device structure for simulation was then modified with the implanted region penetrating 50nm into the GaN under the contact edge, this was found to be critical in reducing the electric field at the contact edges. This is also a valid assumption to make, given the approx. 50nm of lateral penetration of the implanted species under the contact edge (as described in section 4.3.2).

The device structures used in this study employed a thick 170nm metal contact that serves as the implantation mask and the p-contact, the use of the thick p-contact precludes the use of top-illumination for these structures due to the near complete light absorption in the thick metal. However top illuminated devices may also be realized with implantation edge termination by the use of a sacrificial mask layer to serve as the implant mask, while ensuring
that the thin transparent p-contact metal contact deposited in a subsequent process step has
its edges (perimeter) overlapping the implanted region.

The p-i-n and the p-i-n-i-n separate absorption and multiplication structure are the most
widely used structures for III-N APDs. The ion-implantation based edge termination shows
promise for increasing the reliability while reducing the dark current, noise and premature
breakdown in III-N APDs. Additionally the prevention of edge breakdown would enable
taking the bulk of the device to higher voltages (and electric field) to realize high photocurrent
gain; making it extremely valuable for Geiger mode devices.

4.4 Chapter references

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Chapter 5

Summary and future directions

5.1 Advanced APD designs

In the course of this work significant progress was made on solving the issues plaguing III-N APDs. The defect density in the films was reduced by improved MOCVD techniques and defect isolation schemes, the sidewall leakage current was reduced by the use of ALD passivation; and the premature breakdown of III-N APDs was reduced by ion-implantation based contact edge termination technique.

The future direction of this project will involve combining these techniques to realize high reliability and high performance visible blind GaN and solar blind AlGaN APDs. It would also enable the realization of more complex device designs that have lower noise, higher quantum efficiency, photon counting and other capabilities. Discussed in this chapter are design improvements beyond the simple Schottky, p-i-n and the p-i-n-i-n designs currently in use for III-N APDs.
One significant step forward would be to make use of heterostructures. The III-N material system with AlN, GaN, InN and its alloys span a wide range of bandgaps (from 6eV for AlN to 0.7eV for InN ) while maintaining the same wurtzite crystal lattice, enabling the growth of heterostructures.

5.1.1 Transparency of higher bandgap AlGaN

Shown in figure 5.1 is the transmission spectra of Al$_x$Ga$_{1-x}$N for different alloy compositions. The transmission spectra shows a sharp absorption cutoff, dependent on the bandgap of the material (figure 5.1 inset) [1].

![Figure 5.1: Transmission spectra of Al$_x$Ga$_{1-x}$N and the bandgap energy vs AlN mole fraction shown in inset [1].](image)
By the use of higher bandgap materials in the buffer layers and contact layers that are in the optical path of the incident radiation of a photodetector, the absorption losses can be minimized leading to higher quantum efficiency. In the case of a 280nm solar blind APD (Al$_{0.4}$Ga$_{0.6}$N active region), by the use of a AlN buffer layer and Al$_{0.6}$Ga$_{0.4}$N n-contact layer; incident radiation with energy below 4.6eV ($\lambda$>260nm) can pass through into the active region with little absorption. This would enable the detector to have higher quantum efficiency (QE) in the range of 260nm to 280nm. While this increase in QE over a small wavelength bandwidth may not be of much interest for wide spectrum imaging applications, it would certainly be of interest for instrumentation, military and communication applications that employ UV sources. UV sources such as UV LEDs and lasers have a very narrow emission spectrum (figure 5.2 [2]) and can be chosen so as to match the high QE detection spectrum of the photodiode.

![Figure 5.2: Emission spectrum of a commercially available UV LED (Optan series from Crystal IS [2]).](image-url)
5.1.2 Polarization charges at III-N heterointerfaces

The high electronegativity of the nitrogen atom gives the covalent bonds in III-Ns a high degree of ionicity. Due to the ionicity of the bonds and the absence of inversion symmetry in the III-N wurtzite crystal structure along the [0001] axis, a strong spontaneous polarization is created in the material leading to induced charges on the surface [3][4][5]. The spontaneous polarization in AlGaN is a function of the alloy composition and increases with Al percentage. Furthermore, strain in III-N films causes piezoelectric polarization that is in the same direction as the spontaneous polarization for tensile strain and in the opposite direction for compressive strain (figure 5.3).

Figure 5.3: Direction of the spontaneous $P_{SP}$ and piezoelectric polarization $P_{PE}$ in GaN-AlGaN heterostructures [4].
Shown in figure 5.3 is the direction of the polarization in AlGaN/GaN heterostructures grown along the [0001] axis (Ga face). The variation in magnitude of polarization in III-Ns with alloy composition leads to a residual charge at heterointerfaces that can influence device operation and performance. This residual charge can attract free carriers leading to the formation of a two dimensional electron or hole gas (2DEG and 2DHG) depending on the direction of the residual polarization. The 2DEG forms the basis of the popular III-N high electron mobility transistor (HEMT) and is of great commercial importance. However residual polarization at heterointerfaces is not always beneficial and is known to reduce the performance of III-N LEDs and laser diodes, prompting research into the development of these devices on non-polar and semi-polar planes of GaN [6][7][8].

Figure 5.4: Calculated sheet charge density at the AlGaN/GaN heterointerface (+σ) as a function of Al alloy composition [4].
Shown in figure 5.4 is the sheet charge density at the AlGaN/GaN heterointerface as a function of Al composition in the AlGaN layer. The polarization at heterointerfaces is an important factor for the development of any III-N device and needs to be considered for APDs as well.

5.2 Development of novel heterostructure SAM APD

GaN separate absorption and multiplication (SAM) APDs under back illumination have been demonstrated by Razeghi et al. [9][10] and are seen to have higher gain and lower noise due to single type of carrier (hole) injection into the multiplication region. Before going into the proposed heterostructure SAM design, let’s look at the p-i-n and SAM designs in detail using TCAD simulations. All the simulations are done at 120V reverse bias with a 200nm n-layer, 250nm intrinsic region, and 300nm p-layer assuming growth along the +c axis. In the case of SAM designs a 125nm absorption and 125nm thick multiplication region (totaling to 250nm) is used so as to be comparable to the p-i-n structure. The carrier concentration of the layers has been set to the typical values measured in our MOCVD grown layers: 2x10^{18} cm\(^{-3}\) for the n-type layer, 1x10^{16} cm\(^{-3}\) for the undoped layer (electrons) and 4x10^{17} cm\(^{-3}\) for the p-type layer.

5.2.1 GaN p-i-n APD

Shown in figure 5.5 is the TCAD simulation of a typical p-i-n GaN APD at 120V reverse bias. A field of 2.7MV/cm is attained in the intrinsic region that serves both as the absorption and the multiplication region. The field shows a sharp drop in the n-GaN region with a voltage drop of 9V but shows a less steep decline in the p-region causing a voltage drop of 47V.
5.2.2 GaN p-i-n-i-n SAM APD

Shown in figure 5.6 are the simulation results for a SAM APD, the n-layer has been reduced to 150nm and a 50nm n-GaN region is inserted in between two u-GaN regions each of 125nm.

Figure 5.6: Structure, band diagram, electric field of a p-i-n-i-n GaN SAM APD simulated at -120V.
From the electric field distribution, it can be seen that the bottom u-GaN layer has a lower electric field and serves as the absorption region while the other u-GaN region with the high electric field (3MV/cm) serves as the multiplication region. The 50nm n-GaN layer acts as a charging layer increasing the field in the multiplication region that is bounded by the p and n regions on either side. The structure is designed for illumination from the bottom (substrate side). The photons that are absorbed in the absorption region result in electron-hole pairs but only the holes drift into the multiplication region while the electrons that drift in the opposite direction are simply collected by the n-contact. The injection of only one type of carrier, holes in this case into the multiplication region results in lower multiplication noise in the APD and higher gain due to the higher hole impact ionization coefficient in GaN [9][10].

A voltage drop of 14V total is seen in the n-GaN layers while a drop of 55V is seen in the p-GaN (when the structure is biased at 120V). By increasing the doping in the n-type and p-type regions, the electric field profile can be made steeper and the voltage drop can be reduced which in addition to increased APD reliability and performance would also simplify the driver circuitry. However this is difficult to achieve without introducing additional defects in the structure.
5.2.3 Novel heterostructure SAM APD

In place of using an n-type layer to act as a charging layer in-between the absorption and the multiplication region, a single AlGaN layer can be used as the multiplication region. The residual polarization charge at the bottom u-GaN/u-Al\textsubscript{0.4}Ga\textsubscript{0.6}N interface results in fixed positive charges at the interface that performs the role of the charging layer. In addition the structure has many other benefits.

An electric field of 4.1MV/cm is achieved in the multiplication region much higher than the field needed for avalanche gain (2.6 – 3.0MV/cm [11][12]) in the material, allowing for the use of a much lower bias voltage of 67V. The field distribution in the absorption and multiplication layers may be tuned further by the use of an intermediate n-type layer as in the conventional SAM structure.

The negative polarization charge at the top u-Al\textsubscript{0.4}Ga\textsubscript{0.6}N/p-GaN interface serves to decrease the electric field in the p-GaN layer within a very small thickness, reducing the voltage drop.
in the p-layer to 35V compared to 55V in the conventional SAM. The voltage drop in the n-layers is also reduced but by a much smaller amount (3V). These values are based on the simulation done at 120V to serve as comparison to the previous structures. The lower voltage drop in the p-layer would also allow for a thinner p-GaN layer making top illumination into the absorption region possible in the 365nm to 280nm wavelength range that the multiplication layer is transparent to.

When operated in the wavelength range of 365nm to 280nm illumination, the lack of photon absorption in the higher bandgap AlGaN multiplication region would also lead to lower noise in the APD due to single type of carrier injection from the absorption region.

Enhancement of quantum efficiency in APDs is possible by the use of a transparent n-contact layer that would allow for illuminating the absorption region from the bottom with no loss in the contact layer. To achieve this we need to grow the structure with transparent buffer layers and make use of a higher bandgap AlGaN based n-layer.

![Hetero SAM APD w/ transparent n-layer](image)

**Sub.**
- n-Al$_{0.4}$Ga$_{0.6}$N
- u-GaN
- u-Al$_{0.4}$Ga$_{0.6}$N
- p-GaN

Figure 5.8: Simulation results of the heterostructure SAM APD at -120V with a higher bandgap Al$_{0.4}$Ga$_{0.6}$N based n-layer.
Shown in figure 5.8 is a simulation of the hetero SAM APD with the n-GaN layer replaced by a higher bandgap n-Al$_x$Ga$_{1-x}$N layer. While the structure has the advantage of a higher bandgap (transparent to radiation with $\lambda > 280\text{nm}$) n-layer, the residual polarization at the n-AlGaN/u-GaN interface (negatively charged) causes a depletion in the n-layer, leading to an increase in electric field and voltage drop in the layer. A peak electric field of 3.7MV/cm is reached in the n-layer and can lead to breakdown in structure away from the multiplication region and is thus undesirable. Also the voltage drop in the n-layer is now increased to 19V compared to 7V seen in the previous structure (hetero SAM APD). A novel solution to this is presented in the next section in the context of p-i-n AlGaN APDs that allows for the use of a transparent n-layer without resulting in an electric field spike and voltage drop in the n-layer.

The heterostructure SAM APD presented in this section can be further optimized by tuning the composition of the AlGaN layer to find the right balance between polarization charge and critical field intensity. AlGaN films grown on GaN layers tend to crack due to the tensile stress developed in the AlGaN layer as discussed in section 2.5. This can however be counteracted by growing the GaN layer on an AlN layer that leads to compressive stress in the film. Using this technique we have successfully grown AlGaN/GaN/AlN on DSP sapphire using the pulsed MOCVD technique for AlN and AlGaN.
5.3 Development of novel solar blind APD with transparent (higher bandgap) n-layer

Due to the low doping efficiency of p-AlGaN, lower bandgap p-GaN is the commonly used p-type layer for AlGaN devices, making it necessary to illuminate AlGaN photodiodes from the n-side (bottom side). When illuminating from the n-side, the absorption losses can be minimized by the use of a higher bandgap material for the n-layer.

5.3.1 p-i-n AlGaN APD with step junction in n-layer

Shown in figure 5.9 is the simulation of a p-i-n APD with an Al$_{0.4}$Ga$_{0.6}$N intrinsic region, a GaN based p-region and an n-AlGaN layer with 20% higher Al alloy composition (Al$_{0.6}$Ga$_{0.4}$N) for the n-region.

![Simulation results of Al$_{0.4}$Ga$_{0.6}$N APD with n-Al$_{0.6}$Ga$_{0.4}$N layer at -120V.](image)

The residual polarization at the Al$_{0.4}$Ga$_{0.6}$N/Al$_{0.6}$Ga$_{0.4}$N interface leads to negative polarization charge at the interface causing a depletion region in the n-layer and a electric field spike. The
electric field at the edge of the n-layer is much higher than what is achieved in the intrinsic region and can lead to a breakdown in the structure even before the intrinsic region reaches the avalanche voltage. This is similar to the effect seen in the structure presented in figure 5.8.

5.3.2 p-i-n AlGaN APD with undoped graded AlGaN interlayer

Instead of using a step junction from n-Al$_{0.6}$Ga$_{0.4}$N to u-Al$_{0.4}$Ga$_{0.6}$N, a compositionally graded interlayer may be grown. Shown in figure 5.10 is the effect of insertion of a 40nm undoped graded layer that grades linearly from 60% AlGaN to 40% AlGaN. The n-Al$_{0.6}$Ga$_{0.4}$N layer thickness was decreased by 40nm to maintain the same thickness of the structure.

![Graph showing electric field profile](image)

**Figure 5.10: Simulation results of Al$_{0.4}$Ga$_{0.6}$N APD with n-Al$_{0.6}$Ga$_{0.4}$N layer and a composition graded u-AlGaN interlayer denoted by uĝ.**

Composition graded AlGaN layers lead to the formation of a 3D polarization charge due to the continuous change in alloy composition causing residual polarization throughout the graded layer [13]. The graded u-AlGaN layer does not show any positive impact on the electric field profile (figure 5.10) with the field still spiking at the interface of the n-Al$_{0.6}$Ga$_{0.4}$N and the graded u-AlGaN layer.
5.3.3 p-i-n AlGaN APD with n-doped graded AlGaN interlayer

When the graded AlGaN layer presented in the previous structure is n-doped, the negatively charged 3D polarization charge in the graded layer can be compensated by the positive charge from the depletion of the n-type dopant in the layer. This causes the field profile to flatten out preventing spiking of the electric field. Shown in figure 5.11 are the simulation results assuming a doping concentration of $2 \times 10^{18} \text{cm}^{-3}$ (n-type) in the composition graded layer (Al$_{0.4}$Ga$_{0.6}$N to Al$_{0.6}$Ga$_{0.4}$N).

![Figure 5.11: Simulation results of an Al$_{0.4}$Ga$_{0.6}$N APD with n-Al$_{0.6}$Ga$_{0.4}$N layer and a composition graded n-AlGaN interlayer denoted by n$\tilde{g}$](image)

<table>
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<th>Sub.</th>
<th>n-Al$<em>{0.6}$Ga$</em>{0.4}$N</th>
<th>n$\tilde{g}$</th>
<th>u-Al$<em>{0.6}$Ga$</em>{0.4}$N</th>
<th>p-GaN</th>
</tr>
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</table>

Figure 5.11: Simulation results of an Al$_{0.4}$Ga$_{0.6}$N APD with n-Al$_{0.6}$Ga$_{0.4}$N layer and a composition graded n-AlGaN interlayer denoted by n$\tilde{g}$. 

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5.3.4 Polarization charge and space charge at the heterointerface

![Graphs showing polarization charge and space charge for different hetero SAM APDs configurations.](image)

Figure 5.12: Simulated polarization charge and space charge in the n-region of the hetero SAM APDs with a) step junction b) undoped graded AlGaN interlayer and c) n-doped graded AlGaN interlayer.
For the structure shown in section 5.3.2 with the 40nm undoped graded AlGaN interlayer, the polarization charge is distributed in the graded layer and is of a lower magnitude than the step junction (figures 5.11a and b). For the structure shown in section 5.3.3, the distributed polarization charge and the space charge coincide and being opposite in polarity and comparable in magnitude cancel each other out. However, the space charge being higher in magnitude, the net charge in the layer is a small positive value causing a small change in the electric field. This can be seen in the electric field profile in figure 5.11 (blue curve) which shows a small ramp in the field value in the graded layer.

The separation of the positive and negative charge due to the space charge and polarization respectively causes the field spike seen at the heterointerfaces in sections 5.3.1 and 5.3.2. By spreading out the polarization field using a graded layer, the value of the polarization charge density can be reduced and brought into the range of carrier concentration that can be achieved by doping the material. For AlGaN with Al < 60%, the electron concentrations in the range of \(\sim 2 \times 10^{18} \text{cm}^{-3}\) can be achieved by silicon doping. To compensate for the polarization charge at the heterointerface having a 20% change in AlGaN concentration (from 60% to 40%), an n-doped graded layer of \(\sim 40\text{nm}\) thickness would be needed.

This technique can also be applied to the hetero SAM APD design presented in section 5.2.3-figure 5.8 by adding a composition graded n-doped AlGaN layer in between the n-Al\(_{0.4}\)Ga\(_{0.6}\)N and the u-GaN layer. The thickness of the graded layer and the doping level can be adjusted to achieve an optimal field profile. All III-N photodiodes and not just APDs stand to benefit from the transparent n-layer technique described in this section. The technique can also be applied to other III-N heterostructure devices to prevent premature breakdown at the interface.
5.4 Ionization engineering for III-N APDs

The band diagram of an APD can be engineered by the use of heterostructures to favor single type of carrier multiplication (electrons or holes). This reduces the charge carrier feedback process during avalanche multiplication and leads to lower noise in APDs. Engineering the band diagram could also allow for lower voltage operation, precise gain and other advantages. Shown in figure 5.13 is the band diagram of a InAlGaAs staircase APD [14][15].

![Band Diagram](image)

**Figure 5.13:** Band diagram of InAlGaAs staircase APD under a) no bias, and b) reverse bias
The conduction band discontinuity between different alloy compositions of the InAlGaAs quaternary material system are used to create steps in the conduction band that cause electron multiplication (arrows in the conduction band of figure 5.13b), while the smaller valence band offsets do not allow for efficient hole multiplication. The structure thus allows for electron multiplication while suppressing hole multiplication leading to lower multiplication noise in the APD [14][15].

5.4.1 Development of novel III-N staircase APD

The values of the conduction band and valence band offsets in the III-Ns is an active area of research and is known to vary with polarization and stress state in the heterostructures [16]. A value of ~0.7eV is commonly reported for the valence band offset and a value of ~2eV for the conduction band offset between AlN/GaN[17][18]. This difference in band offsets in the conduction and valence bands (2eV vs .7eV) should enable the design of staircase APD structures in III-Ns.

Figure 5.14: Test structure for III-N staircase APD with 6 layers of graded AlGaN (30%Al to 0% Al in 40nm).

Shown in figure 5.14 is the structure grown to test the feasibility of III-N staircase APD that has six graded AlGaN layers (steps) to form the staircase. The simulated band diagram for a staircase APD with 4 graded AlGaN layers and the electric field in the structure under reverse
bias at 24V is shown in figure 5.15 (Simulation convergence issues prevented the simulation of more steps and higher voltages).

Figure 5.15: Band diagram of III-N staircase APD under reverse bias

Figure 5.16: AFM image of the III-N Al$_3$Ga$_7$N x 6 staircase structure grown on n-GaN/sapphire template.
Each step in the staircase consists of a 40nm layer of AlGaN where the composition of Al is graded from 30% to 0. This is then followed by the next step starting with 30% AlGaN, creating a conduction band offset at the interface as seen in the band diagram of figure 5.15 (green curve). The large spikes in the electric field are a result of the conduction band offset at the GaN/Al$_{0.3}$Ga$_{0.7}$N interface. Shown in figure 5.16 is the AFM image of the staircase structure grown on 4μm thick n-GaN on sapphire template. The structure is crack free with excellent surface quality. However when p-GaN was grown on the structure the surface was cracked and extremely rough. For the purposes of testing the staircase design, the structure without the p-GaN was used with Schottky contacts and top illumination.

Measurements from most regions of the wafer showed large dark current and premature breakdown with some regions showing negative photocurrent (Photo-Current < Dark-Current). However measurements from a few other regions showed reliable photoresponse and gain (figures 5.27 a and b). The shape of the photoresponse and gain curve is very unusual and shows step jumps starting at 10V and is probably due to the polarization charge build up in the staircase layers that is depleted as the voltage is increased. Unfortunately the nature of the gain process could not be verified by temperature dependent IV due to device shorting once the temperature was increased beyond 100°C.

The III-N staircase design could pave the way to obtain APDs with low operating voltages and controlled gain. Future directions would involve development of crack free p-GaN on the structure and integrating the other techniques discussed in this thesis mainly ALD passivation and contact edge termination to improve the leakage current and reliability. Staircase APDs with different number of stairs (steps) will need to be grown and modeled to study the nature
of the gain in these devices. The staircase layer could be used as the multiplication layer in SAM APDs.

Figure 5.17: Measurement results of staircase III-N APD with Schottky contact, a) Two consecutive measurements of dark current and UV photoresponse in the staircase APD (current limit set to 1μA) and b) the corresponding gain.
5.5 Photon counting APDs

Silicon photomultiplier (SiPM) or multi-pixel-photon-counter (MPPC) are photon counting APDs that consist of a parallel array of APDs with quenching resistors [19][20] and have applications in commercial, medical, space and particle physics research applications [21]. Shown in figure 5.18 is a picture of a Hamamatsu MPPC and the corresponding equivalent circuit [22].

Figure 5.18: Picture of a) multiple pixel photon counter and b) the equivalent circuit [22].
The wide-bandgap nature of the III-Ns allows for highly resistive undoped material. The resistivity of GaN can be increased by iron (or chromium) doping to realize semi-insulating nature ($10^3$ to $10^9 \ \Omega \cdot \text{cm}$) [23][24]. The creation of deep traps by ferrous doping compensates for the residual n-type concentration present in conventionally grown undoped GaN [25][24]. The design of the APD proposed here employs highly resistive GaN (or AlGaN) as a bulk quenching resistor for an array of micro pixel APDs.

5.5.1 Development of novel III-N micropixel APD

Shown in figure 5.19 is the structure and simulated electric field in the proposed micropixel GaN APD. The structure employs n-GaN islands embedded within undoped GaN to modulate the field laterally and vertically in the structure. The i-GaN layer below the n-island layer serves as the quenching resistor and is made resistive (by iron doping if needed) while the i-GaN above the n-island serves as the absorption and multiplication region for the APD. The structure works similar to a SAM APD with n-islands creating a high field region between the n-islands and the p-GaN compared to the rest of the structure. An avalanche breakdown in any of the pixels is isolated from the rest due to the resistive GaN layer, in effect creating the equivalent circuit shown in figure 5.18b.

We have done some preliminary research and development into the growth of this structure and have found ion implantation based n-type doping to be the technique of choice to realize the n-islands. Resistive GaN is grown on an n-template up to the point indicated by the arrow in figure 5.19a. The surface of the structure is then patterned with photoresist to create an implantation mask with circular openings and then implanted with silicon ions to create the n-islands.
Figure 5.19: III-N micropixel avalanche APD a) Structure of the APD showing the doping concentration in the layers (the arrow in the picture shows the stage at which growth is stopped for implantation doping) and b) electric field profile in the APD at 80V reverse bias.
The energy and dose is chosen so as to attain the required depth and electron concentration in the material. Upon mask removal and annealing the implanted atoms are incorporated in the lattice and activated. Ion implantation based doping of GaN is an active area of research with groups reporting electron concentrations as high as $5 \times 10^{19} \text{cm}^{-3}$ for silicon implanted GaN[26]. Once the n-islands are created the rest of the structure (i and p-GaN layers) is grown to complete the APD. The fabrication of the APD is similar to the technique discussed in section 1.6 with the exception that the mask for the n-islands (used prior to implantation) and the mesa (used after full device is grown) need to be designed and aligned such that the mesa border (perimeter) does not cut through the n-islands. By keeping the n-islands away from the mesa sidewall, the high field regions along the sidewall can be prevented thereby reducing leakage and increasing reliability.

An APD structure with embedded n-islands was grown and fabricated into devices. Upon testing, the avalanche breakdown voltages were found to be much higher than that predicted by simulation and is believed to be due to low doping of the n-islands. This is possibly due to incomplete activation or desorption of the implanted silicon ions upon GaN regrowth, given the shallow implantation depth (50nm) and the high growth temperatures of MOCVD GaN ($1030^\circ \text{C}$) this is plausible. Many other groups working on implantation doping of GaN have employed a sacrificial AlN based annealing cap layer [27][28].

The future directions of this project would need the optimization of the n-island process and the development of masks and fabrication procedure for alignment of the mesa such that the array of n-islands are contained within the mesa and not exposed along the sidewall. The development of iron doped semi-insulating GaN would also be required or may be acquired from commercial vendors given the widespread availability of this technology [29][30].
5.6 Closing comments

The research presented in this work is a significant step forward in the realization of reliable III-N APDs for imaging, instrumentation, communication and sensor applications. However much work is needed before practical devices can be feasibly realized. The rapid development of low defect and low cost bulk substrate technology for GaN and AlN would be enabling for APDs. Much of the work described in this work employed high temperature AlN buffer layers on sapphire and thus can be easily ported onto bulk AlN substrates. Substrate removal (or thinning) techniques would be an important technology for back illuminated APDs. Such technology is already in development and use by many research groups and companies for back emitting LED and other devices [31][32][33]. The development of practical III-N APDs would open new frontiers for product development and scientific research.

5.7 Chapter references


