High-k gate stack on compound semiconductor channel materials for low power, high performance digital logic applications

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HIGH-K GATE STACK ON COMPOUND SEMICONDUCTOR CHANNEL MATERIALS FOR LOW POWER, HIGH PERFORMANCE DIGITAL LOGIC APPLICATIONS

By

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Abstract

Group III-V compound semiconductors such as InGaAs and InGaSb are actively being considered as channel materials for low power, high performance digital logic applications due to superior carrier transport properties such as mobility and saturation velocity. The high density of interface states at high-k dielectric and III-V interface that results in pinning of Fermi level is one of the major challenges that need to be addressed before III-V CMOS becomes a mainstream technology.

In this thesis, the introduction reviews the mature III-V HEMT parameters and technologies to emphasize the compound semiconductor material advantages. Description of challenges of III-V MOSFET technology which have to be addressed concludes the Chapter.

Chapter 2 reports on interface passivation using an in-situ MBE grown amorphous Silicon layer between GaAs/InGaAs and gate dielectric. To understand interfacial chemistry, various analytical techniques have been used and the correlation between the analytical and electrical data is obtained. MOS capacitors on n- and p-type GaAs with TaN/HfO₂ gate stack and self-aligned, planar, depletion and enhancement mode MOSFETs were fabricated and electrical data is studied. A “fully in-situ” process has been developed which resulted in lower EOT and higher thermal stability of gate stack.
A higher mobility channel material, namely $\text{In}_x\text{Ga}_{1-x}\text{As}$ is studied and effect of a-Si passivation on electrical properties of MOSCAPs and MOSFETs has been examined in Chapter 3.

A buried channel InAlAs/InGaAs architecture for improvement of mobility and the capping with a 2 ML InGaAs layer to improve subthreshold slope has been demonstrated. Additionally, Chapter 4 describes integration of these channels with alternative high-k gate dielectrics. The electrical properties of MOSCAPs, inversion type, enhancement-mode MOSFETs on these gate oxides are studied.

Chapter 5 reports efforts to improve contact resistance of the source-drain Ohmic contacts to InGaAs quantum well channel by MBE re-growth of heavily doped InAs film. Strain related and surface preparation related morphology of re-grown InAs film and dependence on MBE growth parameters is examined. Contact resistivity of metal and re-grown InAs and also between InGaAs channel and re-grown InAs film has been measured.

Finally, Chapter 6 contains summary and future directions.
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None of this would have ever been possible without the love and patience that was shown by my dearest Swami, Bhagawan Sri Sathya Sai Baba. Swami, thank you for showing me the path.

I dedicate this work to all those people who have inspired me through these years. I thank you from the bottom of my heart.
Out of the night that covers me,
Black as the Pit from pole to pole,
I thank whatever gods may be
For my unconquerable soul.

In the fell clutch of circumstance
I have not winced nor cried aloud.
Under the bludgeonings of chance
My head is bloody, but unbowed.

Beyond this place of wrath and tears
Looms but the Horror of the shade,
And yet the menace of the years
Finds, and shall find, me unafraid.

It matters not how strait the gate,
How charged with punishments the scroll,
I am the master of my fate:
I am the captain of my soul.

William Ernest Henley (1849-1903)
CHAPTER 1

INTRODUCTION

1.1 Introduction

The tremendous success of Complementary Metal Oxide Semiconductor (CMOS) technology is due to the scalability of MOS Field Effect Transistor (MOSFET) and this constitutes the Moore’s law which basically states that the number of transistors in an integrated circuit roughly doubles every two years (Fig. 1). Scaling down the transistor dimensions and the thickness of gate dielectric (SiO\textsubscript{2}) has been adequate for achieving the required device performance for several technology nodes while the increase in the drain current has been at the expense of exponentially increasing gate leakage current resulting in excessive power dissipation (1).

![Transistor Scaling](image)

Fig. 1: Scaling of the physical gate length of a transistor vs. year. 15 nm gate length devices (30 nm technology node) are expected to be in production by the year 2010, according to Moore’s law (1).
The thickness of SiO$_2$ has been scaled down to 1.2 nm and has successfully been implemented for the 90 nm technology nodes (2) but further reducing the thickness has resulted in unacceptably large leakage currents. The gate leakage which increases exponentially due to the tunneling through the thin gate dielectric results in large static power dissipation. As can be seen from the graph below (Fig. 2), the power density will be as high as 200 W/cm$^2$ as we get into sub-20 nm technology node which is near the physical limit at room temperature (3).

![Graph showing active and passive power density vs. transistor gate length.](image)

Fig. 2: Active and passive power density vs. transistor gate length. Power density can be as high as 200 W/cm$^2$ for 22 nm technology nodes and beyond (3).

One of the major technological breakthroughs that kept the Moore’s law alive is the introduction of high-k gate dielectrics. Hafnium (4) and Zirconium (5) based dielectrics were actively studied and at the 45 nm node, the industry started to implement HfO$_2$ as the gate dielectric. The following graph shows the gate leakage current versus the capacitance equivalent thickness for various semiconductor-oxide systems (6).
Fig. 3: Gate leakage density as a function of capacitance equivalent thickness for various semiconductor-oxide systems. For the same CET, Si/SiO$_2$ shows 3-4 orders of magnitude higher leakage current density in comparison to Si/high-k or III-V/high-k (6).

The other major innovation is the introduction of biaxially tensile-strained silicon on relaxed SiGe for NMOS (7) and uniaxially compressive-strained SiGe layer on Si substrate for PMOS (8) for enhanced carrier mobility (fig. 4 and fig. 5).
Fig 4: Enhanced electron mobility (below, fig. 5) due to tensile strained Silicon lattice for NMOS transistor (7) and compressively strained Silicon lattice for higher hole mobility for PMOS transistor (8).

Fig. 5: Electron mobility as a function of electric field for unstrained Silicon and Si-Ge channels (8)

As transistors are aggressively being scaled to sub-15 nm technology nodes, it becomes difficult to maintain the required device performance without exploring new channel materials and new device architectures. Owing to the superior carrier transport properties such as high electron mobility (in materials such as InGaAs, InAs etc.) and high hole mobility (in materials such as GaSb, InGaSb etc.) and high injection velocity, group III-V based compound semiconductors are being extensively researched for high performance,
low power logic applications (9). These materials are considered as the primary candidates in comparison to other materials such as Germanium, Carbon Nanotubes and Graphene to replace Si based channels for sub-15 nm node logic devices (fig. 6).

Fig. 6: Cross sectional TEM images of transistors showing gate length for various technology nodes. Alternative channel materials such as CNT, Nanowires and III-V based devices are being actively researched for future technology nodes (9).

1.2 Group III-V based semiconductor devices

Traditionally, group III-V semiconductors such as GaAs, InGaAs, InP etc. are used in high frequency, high power analog applications. Common examples of these applications include power amplifiers in cell phones, micrometer and millimeter wave communications, imaging, radar and radio astronomy – applications where high gain and low noise at high frequencies are required. These applications typically employ a Metal
A high electron mobility transistor (or a modulation doped FET), shown below, uses GaAs or InGaAs channels sandwiched between epitaxially grown AlGaAs or InAlAs layers, respectively. Due to the conduction band alignment in AlGaAs-GaAs or InAlAs-InGaAs, free electrons diffuse into the lower band-gap material, in this case, GaAs or InGaAs near the interface and a potential barrier confines these electrons into a thin sheet of charge called 2 dimensional electron gas (2DEG). In contrast to a MESFET device, which has a doped channel and as a consequence, lot of ionized impurities, a 2DEG has significantly lesser scattering resulting in a very high electron mobility device structure. The following figures (fig. 7) show the cross section of the device and the band diagram of a AlGaAs-GaAs HEMT structure (10).

Fig. 7: Cross section of the AlGaAs-GaAs device structure and the associated band diagram showing two dimensional electron gas (10).

Electron mobility in such GaAs channel devices was measured to be as high as 6E6 cm²/V-sec at 4K (11).

1.3 III-Vs for Logic Applications: HEMT vs. MOSFET
In Analog applications such as micrometer and millimeter wave applications, a transistor (HEMT or MESFET) is used as an amplifier. In this case, the figures of merit that are of interest are frequency response (maximum frequency $f_{\text{max}}$, cut-off frequency $f_T$), transconductance $g_m$, channel conductance $g_d$ etc.

In Logic applications such as in a microprocessor, a transistor (MOSFET) is used as a switch. In this case, the figures of merit (fig. 8) that are of interest are ON current $I_{\text{on}}$, OFF current $I_{\text{off}}$, threshold voltage $V_T$, threshold voltage dependence on gate length ($V_T$ roll-off), drain induced barrier lowering ($V_T$ dependence on $V_{DS}$), subthreshold swing, operating voltage ($V_{DD}$), intrinsic gate delay, etc. (12).

![Fig. 8: Subthreshold region characteristics of a MOSFET showing the important figures of merit such as $I_{\text{on}}$, $I_{\text{off}}$, SS, DIBL and $V_T$ (12).](image)

The following figure (fig. 9) depicts the cross-section and corresponding band-diagram of both HEMT and MOSFET. As can be seen, HEMT is a Schottky gated device with the gate metal deposited directly on top of the semiconductor. In a MOSFET, a large band-gap dielectric material separates the gate metal and semiconductor. In the latter case, the
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conduction band offset is much larger than in the former case resulting in significantly lower gate leakage current (13).

In addition to the high gate leakage currents in Schottky junctions compared to Metal-Oxide-Semiconductor gate stack, HEMTs cannot be used in digital logic CMOS applications due to the following issues (14):

![Fig. 9: Cross section images of a Schottky gated HEMT and a MOSFET and their associated band diagrams (13)](image)

(1) Scaling: To have good electrostatic control of the scaled down transistor device, the equivalent oxide thickness must be small. The ITRS predicts an EOT of 0.6 nm for 15 nm technology node. While it is possible to achieve low EOT using a high-k dielectric (for example, 5 nm thick ZrO2 gives an EOT of 0.8 nm with acceptable gate leakage), it is not feasible to design a HEMT with low gate leakage and high mobility and
hence high drive current with a thin top barrier whose dielectric constant is approximately 12.

(2) Power dissipation: The gate leakage in a metal-oxide-semiconductor gate stack is significantly smaller than in a Schottky gated device such as a HEMT due to the much larger conduction band offset between the large bandgap gate oxide and the semiconductor. As mentioned above, the conduction band offset between the top barrier semiconductor and metal gate is small resulting in Schottky emission of carriers resulting in high off-state currents which leads to excessive static power dissipation.

1.4 III-Vs as Channel Materials in MOSFETs: Advantages and Challenges

As mentioned earlier in the section, III-Vs have superior carrier transport properties such as high electron mobility and high injection velocities. The following table summarizes the electron mobility, band-gap and electron saturation velocity of III-V semiconductors and Si (measured at RT).

Table 1: Comparison of room temperature electron mobility, electron saturation velocity and band gap of channel materials such as Si, GaAs, InGaAs, InAs and InSb.

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>In_{0.5}GaAs</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>at n_e=1E12cm^{-2}</td>
<td>600</td>
<td>7,000</td>
<td>10,000</td>
<td>15,000</td>
<td>30,000</td>
</tr>
<tr>
<td>(cm^2/V.s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saturation</td>
<td>1.0</td>
<td>1.2</td>
<td>0.8</td>
<td>3.5</td>
<td>5.0</td>
</tr>
<tr>
<td>Velocity(10^7cm/s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Band-gap (eV)</td>
<td>1.11</td>
<td>1.43</td>
<td>0.7</td>
<td>0.36</td>
<td>0.17</td>
</tr>
</tbody>
</table>
The device speed which is described by the intrinsic gate delay (15) is often described by the equation

\[ \tau_i \approx \frac{Q}{I_{D_{sat}}} \approx \frac{C_G V_D}{I_{D_{sat}}} \]

where, \( Q \) is the inversion charge density, \( I_{D_{sat}} \) is drain current in saturation, \( C_G \) is gate capacitance and \( V_D \) is supply voltage.

Therefore, it can be seen that higher the drain current, lower is the intrinsic gate delay (Fig. 10) and thus higher device performance (16).

Fig. 10: Intrinsic gate delay as a function of gate length for Silicon NMOSFET, InGaAs and InAs HEMT as a function of gate length. Note that the supply voltage for III-Vs is about 2X lower as compared to Silicon based devices (16).

The intrinsic gate delay can also be written as

\[ \tau_i \approx \frac{L_g}{V_{inj}} \]

where \( L_g \) is the gate length and \( V_{inj} \) is the injection velocity of the carriers. As mentioned above, III-V
materials have approximately 5X higher injection velocity (Fig. 11, 12) in comparison to Silicon (17,18).

Fig. 11: Electron injection velocity for channel thicknesses of 10 nm, 5 nm and 3 nm for channel materials such as Si, GaAs, InP, Ge, InAs and InSb. For the same channel thickness, InAs and InSb have about 5X higher injection velocity (17).

Fig. 12: Electron injection velocity as a function of gate length for Si, SiGe, In$_{0.53}$GaAs, In$_{0.77}$GaAs and InAs (18).

The intrinsic gate delay is directly proportional to square root of the effective mass and the extrinsic delay is inversely proportional to the square root of the effective mass while the source injection velocity is inversely proportional to square root of effective mass.

The electron concentration which is proportional to density of states which is determined
by band structure is lower in III-Vs. If the parasitic capacitance is high, the speed benefit is reduced and the benefit is primarily due to reduced supply voltage that is used for the operation of a III-V MOSFET.

One of the major disadvantages of III-Vs that were thought to have affected MOSFET performance is the low density of states of these materials. The conduction band density of states of InGaAs is lower than Silicon (2E17/cm³ vs. 3E19/cm³) and this would result in low inversion charge density. For example, while InAs can store only one-third the number of electrons in comparison to Silicon (fig. 13), due to the 5X increase of the injection velocity, the drain current will be about 80% higher than a Silicon based channel at the same drain voltage (19).

Fig. 13: Comparison of inversion charge and ON current for different channel materials. Even though the inversion charge is lower in III-Vs, the ON current is higher as compared to Silicon based channels for a supply voltage of 0.5V (19).

Another important metric that is used for comparison of channel materials is called the energy-delay product and is given by the product of intrinsic gate delay and dynamic
energy. The dynamic energy is given by the product of gate capacitance and the square of the supply voltage. Thus the intrinsic energy delay product is given by:

\[ EDP_i = \frac{C_g V_d^2 \tau_i}{W} \]

while the extrinsic gate delay is directly proportional to cube of supply voltage and inversely proportional to square root of effective mass.

\[ EDP_{ext} \propto \frac{V_d^3}{m_{eff}} \propto \frac{V_d^3}{\sqrt{m^*}} \]

While scaling down the supply voltage has become difficult in short channel devices \((V_T \text{ has to be kept high to have low subthreshold leakage current})\), the supply voltage can be reduced in III-Vs due to the low voltage overdrive or \((V_d-V_T)\) that is needed to achieve high average velocity in the channel.

As can be seen from the graph below, for a 100 nm gate length channel device, a III-V device offers two orders of magnitude (fig. 14) lower values of energy-gate delay (20).

Fig. 14: Comparison of energy delay product as a function of gate length for Si, InGaAs and InSb channel materials. Antimonide based transistors show approximately two orders of magnitude lower EDP as opposed to Silicon for the same gate length (20).
Challenges:

There are several challenges that need to be overcome before III-V MOS can become a mainstream logic technology. The primary challenge for the realization of III-V MOS technology is development of a defect free, low interface state density oxide - III-V interface. Unlike the Si-SiO$_2$ interface, which is considered completely defect free, with an interface trap density in the range of $10^9$ to $10^{10}$/cm$^2$-eV, the native oxide on GaAs is thermodynamically unstable. Therefore a high-$k$ oxide on GaAs/InGaAs channel materials becomes a natural choice. In the case of GaAs-high-$k$ oxide interface, owing to the presence of Ga$^{3+}$, Ga$^{5+}$, As-O and Ga-O bonds at the interface, the Fermi level is pinned due to the high density of interface states. Therefore some form of surface passivation is required that effectively passivates the surface thereby preventing pinning of the Fermi level. Several passivation techniques such as NH$_4$OH surface treatment; a-Si, a-Ge interface passivation layers; PH$_3$ passivation etc. have been developed for GaAs and the interface state density in such cases is typically around $1E11$/cm$^2$-eV, which is very close to the values observed in Si-high-$k$ systems. For InGaAs, the trap densities are in the range of low $1E12$/cm$^2$-eV. In this work, a thin in-situ MBE grown a-Si is used as a passivation layer and the lowest D$_{it}$ obtained is $2E11$/cm$^2$-eV for LaAlO$_3$/Si/GaAs system and $1.5E12$/cm$^2$-eV for GdScO$_3$/a-Si/InGaAs.

The other challenges that need to be addressed is the development of a buried III-V channel system such that there is no degradation of mobility due to the remote Coulomb scattering effect from the presence of high-$k$ gate oxide. Additionally, due to the low thermal stability and low solid solubility of III-V materials, the contact resistance of the
source-drain metals with the underlying semiconductor is quite high due to low carrier concentration in the source-drain regions. To address this issue and to eliminate high temperature anneals, MBE re-grown InAs based source-drain regions are developed in this work.

Even though the channel is comprised of an III-V material, the device has to be successfully fabricated on a Silicon substrate. The direct growth of GaAs on Si was tried by several groups but because of the large lattice mismatch between Si and and III-V materials, GaAs or InGaAs cannot be directly grown on Silicon. The 8% lattice mismatch between Si and In$_{0.53}$GaAs results in various types of defects (fig. 15). Thus, buffer architecture with a large bandgap material between Silicon substrate and InGaAs channel material is required to account for and to accommodate the dislocations.

Fig. 15: Commonly observed defects due to the direct growth of III-V on Silicon substrate (21)
To address this issue, recent papers from Intel have used a 1.5 µm thick III-V buffer on top of which the channel is grown (21), fig. 16.

Fig. 16: 1.3 micron thick III-V buffer is grown on top of Silicon to accommodate defects that arise due to lattice mismatch (21)

The following graphs (fig. 17) show the input and output characteristics of the InGaAs QW FET grown on top of a Silicon substrate.

Fig. 17: Output and input characteristics of a III-V QW FET grown on top of Silicon substrate (21)
1.5 Outline

In this work, III-V metal-oxide-semiconductor technology with amorphous Silicon interface passivation has been developed. The motivation of this work is to explore the feasibility of using III-V compound semiconductor materials as a channel material in n-type MOSFETs for high performance, low power digital logic applications for sub-15 nm node logic technologies. To prevent the high density of interface states that is typically seen in oxide-III-V systems and thereby prevent pinning of the Fermi level, an in-situ MBE grown amorphous Silicon interface passivation layer is employed. The structural properties of the gate stack including the interfacial chemistry and the electrical properties of both metal-oxide-semiconductor capacitors (MOSCAPs) and field effect transistors (MOSFETs) are systematically studied. In addition to the studies on passivation of the interface between high-k dielectric and the semiconductor, various channel materials have been explored including GaAs, In$_{0.20}$GaAs, In$_{0.55}$GaAs, In$_{0.77}$GaAs and InAs, device performance of MOSFETs with both surface channels and buried channels is investigated, integration of these high mobility channels with alternative high-k dielectrics such ZrO$_2$, LaAlO$_3$ and GdScO$_3$ is demonstrated and lastly, InAs based source-drain contacts by MBE re-growth to improve contact resistivity is investigated.

In the introduction part (Chapter 1) of this thesis, conventional III-V compound semiconductor based devices such as GaAs based high electron mobility transistors are briefly discussed. Owing to the high gate leakage in these Schottky gated devices, the feasibility of using such devices for low power, high performance logic is examined.
Finally, the advantages of using III-V materials as a channel in a MOSFET device are explained and the challenges that need to be overcome for making III-V MOS a mainstream technology are discussed. In this thesis, high mobility n-type MOSFETS employing GaAs, InGaAs and InAs channel materials is demonstrated.

In chapter 2, passivation of GaAs using an ultra-thin in-situ MBE grown amorphous Silicon interface passivation layer is studied. It has been found that 1.5 nm thick a-Si is required to prevent Fermi level pinning for an ex-situ deposited gate dielectric. The interfacial chemistry along with the structural properties of the gate stack is studied using transmission electron microscopy, angle-resolved X-ray photoelectron spectroscopy and energy dispersive X-ray spectroscopy. The capacitance-voltage and current-voltage characteristics of MOS capacitors on both n- and p-type GaAs are studied along with the thermal stability of the gate stack. Depletion mode and enhancement mode GaAs MOSFETs with 1.5 nm thick a-Si interface passivation layer, 10 nm thick HfO₂ high-k gate oxide and TaN gate metal are designed, fabricated and the electrical properties are discussed. To scale down the thickness of Silicon passivation layer, an in-situ process for gate dielectric deposition has been developed. In addition to reducing the equivalent oxide thickness and improving the thermal stability of the gate stack, in-diffusion of silicon can be suppressed by scaling down the thickness of Silicon passivation layer to 0.5 nm. Finally, an enhancement mode GaAs MOSFET with 0.5 nm thick a-Si, 10 nm thick in-situ e-beam deposited HfO₂ with TaN metal gate is demonstrated.
In chapter 3, the primary focus is on engineering the channel to achieve high mobility and high drain current. Electrical properties of MOSFETs with ALD deposited HfO$_2$ gate dielectric incorporating channel materials such as In$_{0.20}$GaAs and GaAs/In$_{0.20}$GaAs are investigated. To realize higher drive currents, In$_{0.53}$GaAs surface channel and In$_{0.52}$AlAs/In$_{0.53}$GaAs buried channel MOSFETs with HfO$_2$ gate dielectric are demonstrated. Alternative passivation layers such as MBE grown amorphous Aluminum is investigated and the effect of Silicon IPL, Aluminum IPL and no passivation layers on the frequency dispersion of CV characteristics of p-type InGaAs MOSCAPs is compared.

The integration of alternative high-k gate dielectrics such as ALD ZrO$_2$, MBE grown binary rare-earth oxides such as LaAlO$_3$ and GdScO$_3$ with GaAs and In$_{0.53}$GaAs is demonstrated in chapter 4. The thermal stability of electrical characteristics of p-type GaAs MOSCAPs with amorphous MBE grown LaAlO$_3$ is thoroughly investigated including the effect of post metallization anneal on the accumulation capacitance, equivalent oxide thickness and hysteresis is studied. The effect of a-Si passivation on the electrical characteristics of InGaAs MOSCAPs such as interface trap density and frequency dispersion is discussed. The advantages of passivating InGaAs with a-Si is further demonstrated in MOSFETs – surface channel, inversion type, enhancement mode MOSFETs with 0.5 nm a-Si show lower subthreshold slope and lower gate leakage in comparison to MOSFET devices without any passivation. A similar effect is seen on MOSFET devices with MBE grown amorphous GdScO$_3$ gate oxide. Amorphous silicon passivation of InGaAs MOSCAP samples with GdScO$_3$ show frequency dispersion of less than 3%/dec. and a lower interface trap density at the valence band edge in
comparison to InGaAs samples without a passivation layer. Lastly, the integration of InGaAs with ALD ZrO$_2$ is demonstrated. Although ZrO$_2$ is not amorphous, due to its high dielectric constant, it is considered as an alternative high-k dielectric for future technology nodes. Additionally, precursors for atomic layer deposition of ZrO$_2$ are well developed and ALD is a commercially viable technique for mass production in today’s semiconductor fabrication facilities.

The advantage of obtaining a high drain current by using an III-V compound semiconductor based channel material is lost if the source-drain contact resistance is poor. Due to the lower thermal stability of these materials in addition to the poor solid solubility of the dopant species in III-Vs, source-drain contact resistances are typically higher than those in Silicon. In chapter 5, an alternative to the conventional ion implantation followed by high temperature implant activation is the MBE re-growth of source-drain regions using a suitable III-V material. In this work, heavily n-doped InAs is re-grown after surface treatment of the InGaAs surface. The surface morphology of the re-grown InAs film is studied as a function of surface treatment and growth temperature. Even though MBE is considered a line-of-sight growth technique, using migration enhanced epitaxy and elevated growth temperatures, smooth, continuous, conformal InAs films were obtained. Contact resistivity measurements between the InAs film and a TiW metal, grown by both in-situ and ex-situ deposition techniques were studied. Finally, morphology of the re-grown In(Ga)As films was optimized and PN junction leakage currents were measured between the heavily n-doped InAs and p-doped underlying InGaAs.
All the major conclusions of the work are summarized in Chapter 6. As part of the future
directions, the effect of a-Si passivation on the degradation in the electron mobility in the
inversion channel is studied. Various high-k gate stacks such as ZrO$_2$/InGaAs,
ZrO$_2$/Al$_2$O$_3$/InGaAs, Al$_2$O$_3$/InGaAs and in particular, the effect of a thin a-Si layer (thin
SiO$_x$ layer) on the carrier mobility will be investigated. Additionally, short channel
effects that are seen in sub-micron gate length channel InGaAs MOSFETs will be studied. Lastly, Antimonide based material systems, namely, GaSb and InGaSb channel
materials will be investigated for the demonstration of high mobility p-channel
MOSFETs.

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CHAPTER 2

Passivation of GaAs with in-situ MBE Grown Amorphous Silicon

2.1. Introduction

One of the primary issues with Metal-Oxide-Semiconductor (MOS) devices on GaAs and InGaAs is the occurrence of frequency dispersion of CV characteristics in accumulation region (1). This dispersion in CV characteristics or the reduction of maximum capacitance with increasing measurement frequency is attributed to a high density of interface states that results in a pinned Fermi level. The elimination of this anomalous frequency dispersion of the accumulation capacitance of III-V MOS devices is the motivation behind surface treatment and studies related to interface passivation. In this case where the Fermi level is pinned, the gate voltage is essentially used in charging and discharging of the interface traps as opposed to controlling the thickness of the depletion layer in the semiconductor.

Fermi level pinning refers to when the Fermi level at the oxide/GaAs interface is pinned at approximately the midgap. That is, the position of Fermi level $E_f$ does not vary with respect to gate bias and the corresponding CV curve essentially remains flat and shows no distinction between depletion and accumulation regions. Fermi level is said to be unpinned when the $E_f$ at the oxide/GaAs interface can move a distance of $2\Psi_B$ (bulk potential) resulting in strong inversion caused by gate bias, where $\Psi_B$ is $E_f$ measured from the intrinsic level $E_i$. The cartoon shown (Fig. 1) below demonstrates pinning of the Fermi level due to presence of excessive interface states.
Fig. 1: Energy band diagram showing the pinning of the Fermi level due to the high number of interface traps at the interface of oxide and a III-V semiconductor.

The native oxide of GaAs exhibits As$^{5+}$ and As$^{3+}$ oxidation states, Ga$^{3+}$ and Ga$^{1+}$ oxidation states and Ga-O and As-O bonds. Spicer et al. (2) have reported that the high density of interface states is a result of different surface species including Ga-O bonds, As-O bonds, elemental As, As and Ga antisites. Hale et al. (3) have reported that the disruption of As-O bonding at the dielectric/GaAs interface results in a pinned interface. Hinkle et al. (4) have reported that Ga-O bonds may be primarily responsible and probably the most important species to control and it has also been reported that deposition of a Ga sub-oxide maybe necessary for a low defect density. In addition, it has been observed by several groups that the dispersion is significantly more pronounced on n-type GaAs than for a p-type GaAs. More recently, Hinkle et al. (5) have reported that the presence of a stable sub-oxide Ga$_2$O or Ga$^{1+}$ oxidation state does not detrimentally affect the device characteristics and in contrast, the removal of the Ga$^{3+}$ oxidation state (Ga$_2$O$_3$ sub-oxide) is of utmost importance to achieve reduction of frequency dispersion.
It has been further demonstrated that on Al$_2$O$_3$/GaAs (111)A interface, significantly less Ga$_2$O$_3$ or Ga$^{3+}$ state led to unpinning of the Fermi level, resulting in superior CV and MOSFET characteristics (6).

### 2.2 Interface Passivation techniques

For the 15 nm technology node and beyond, where the gate lengths are deeply scaled, it is imperative to use a high-k dielectric to obtain a low equivalent oxide thickness so that a good electrostatic control of the device is maintained. Additionally, a high-k gate oxide is necessary to improve the subthreshold slope, since the subthreshold swing depends on the value of oxide capacitance (and interface trap capacitance) (7). To prevent oxidation of GaAs or InGaAs and thereby reduce the density of interface states, it is advantageous to deposit the high-k dielectric through an in-situ process i.e. without breaking the ultra-high vacuum, but, from a commercial, high volume manufacturing point of view, an ex-situ process such as atomic layer deposition is preferred. Additionally, precursors for ALD deposition of high-k dielectrics such as HfO$_2$, ZrO$_2$ are well developed.

Several groups have reported both in-situ and ex-situ surface cleans and interface passivation techniques - MBE grown Gallium Gadolinium oxide (GaGd)$_2$O$_3$ (8), (NH$_4$)$_2$S or Sulphur passivation (9), atomic layer deposition of oxides such as Al$_2$O$_3$ or HfO$_2$ (10), in-situ MBE grown amorphous Silicon (11) or Germanium (12) layers are among the most commonly used techniques. MBE grown Gallium Gadolinium oxide is considered promising due to the formation of electrically inert bonds at the interface such as Ga-O-
Ga rather than As-O bonds. Atomic layer deposition of Al$_2$O$_3$ or HfO$_2$ results in the formation and subsequent conversion of volatile interfacial layer products into the high-k oxides. In this work, we have used an ultra thin (0.5 nm), in-situ MBE grown amorphous Silicon as the interface passivation layer and in this chapter, passivation of GaAs and InGaAs will be discussed in detail.

2.3 Passivation of GaAs with in-situ MBE grown Amorphous Silicon

It was previously discussed, the native oxide of GaAs has a mixture of Ga and As oxidation states in addition to As-O bonds and Ga-O bonds which determine the extent of pinning of the Fermi level. By capping the surface with a passivation layer or by using a suitable surface cleaning technique prior to oxide deposition, the density of As-O bonds and the Ga oxidation states can be significantly reduced. In this experiment, 250 nm thick GaAs was grown by MBE on a two-inch n$^+$ GaAs substrate and in-situ encapsulated with 0.5, 1, 1.5 and 2.5 nm thick amorphous Silicon (a-Si) interface passivation layer (IPL). After the growth of a-Si IPL, the sample is removed from the high vacuum MBE chamber and is placed in a physical vapor deposition chamber for deposition of HfO$_2$ gate oxide. To determine the effect of oxide scaling, 4, 7 and 10 nm thick HfO$_2$ was deposited. After oxide growth, 200 nm thick TaN gate metal was grown by RF sputtering a Tantalum target in a N$_2$+Ar ambient. Post deposition anneal of the samples was performed at a temperature of 500°C for 5 mins. in N$_2$ and post metallization anneal was performed in a temperature range of 500°C to 800°C in N$_2$ ambient. The backside Ohmic contact is made by soldering Indium onto the GaAs surface.
The figure shown below (fig. 2) is the high frequency (1 MHz) capacitance-voltage characteristics measured from -1V to +3V on GaAs n-MOS capacitors with variable a-Si thicknesses. The samples without any passivation layer and those with 0.5 nm and 1 nm thick a-Si IPL displayed poor CV characteristics with large frequency dispersion and stretch-out indicating a huge interface trap density and consequently a pinned Fermi level. On the other hand, samples that had a 1.5 nm and 2.5 nm thick a-Si showed good CV characteristics with a clear distinction between depletion and accumulation regions indicating a good control of the depletion width by the gate voltage (fig. 2).

![Graph showing capacitance-voltage characteristics](image)

**Fig. 2:** High frequency CV characteristics of n-GaAs MOSCAPs with variable thickness of amorphous Silicon interface passivation layer. At least 15Å of a-Si is needed to prevent Fermi level pinning.

In figure 3, high frequency CV characteristics for n-GaAs MOSCAPs with 1.5 nm thick amorphous Si and HfO$_2$ thicknesses of 4 nm, 7 nm and 10 nm are shown. The samples have good n-type CV behavior indicating a clear distinction between depletion and
accumulation and it can be seen that the accumulation capacitance increases as the oxide thickness is reduced. Thus it can be safely concluded that for samples with an ex-situ deposited HfO$_2$, a minimum a-Si thickness of 1.5 nm is required to prevent oxidation of the GaAs surface and thus prevent pinning of the Fermi level (13).

Fig. 3: High-k dielectric scaling: High frequency CV characteristics of n-GaAs MOSCAP with variable thickness of HfO$_2$ and 15A of amorphous Silicon passivation layer.

The dielectric constant of HfO$_2$ gate oxide can be determined from the slope of the EOT plotted as a function of the physical thickness of the oxide, k-value of HfO$_2$ is found to be 22 (fig. 4, shown below). It can be further seen from the figure below the linear dependence of EOT on the physical thickness of HfO$_2$. The straight line intersects the y-axis at ~ 1.5 nm indicating the contribution of the a-Si passivation layer to the EOT. For the sample with 4 nm thick HfO$_2$, EOT was determined to be 2.1 nm. Also shown in the inset is the dependence of the gate leakage current density on the EOT. It can be seen that leakage current density increases with decrease in oxide thickness and for the 4 nm thick HfO$_2$, gate leakage is ~ 1 mA/cm$^2$ measured at $V=V_{fb}+1V$. 
Fig. 4: Equivalent oxide thickness (EOT) measured as a function of HfO₂ thickness. Slope of the line gives the dielectric constant as 22 for HfO₂. Inset shows gate leakage current density vs. EOT – $J_g$ is 1 mA/cm² for 4 nm thick HfO₂.

Hysteresis which indicates the amount of charge in the oxide can be observed by sweeping the gate voltage from -1V to +3V and again immediately from +3V to -1V (bi-directional sweep) is shown below (fig. 5). Clearly, as the physical thickness of oxide is reduced, the charge in the oxide is also seen to decrease.
Fig. 5: Bi-directional sweep CV characteristics showing hysteresis (oxide charge). As can be seen, oxide charge gets smaller as thickness of HfO₂ is reduced.

The sensitivity of CV measurements to oxide thickness as seen from the difference in hysteresis in addition to the clear distinction between depletion and accumulation regions indicating a good control of the space charge region by the gate voltage indicates that the Fermi level is not pinned.

To obtain an understanding of the GaAs/a-Si interface, high resolution transmission electron microscopy of the gate stack analysis was performed. The a-Si was seen to be partially oxidized with the interface between a-Si and GaAs remaining atomically sharp without any visible degradation after 500°C anneal. To estimate the thickness of the oxidized Si layer, TEM analysis was performed on a sample with 2.5 nm thick a-Si, the image is shown below (fig. 6). As can be seen, the a-Si layer is partially oxidized as SiOₓ layer showed brighter contrast and the thickness of the oxidized layer is about 1.4 nm, which is in agreement with the result obtained on the MOSCAP with 1.5 nm a-Si.
Fig. 6: High resolution TEM image of the gate stack annealed at 500°C. Amorphous Silicon passivation layer gets partially oxidized during high-k deposition.

Energy dispersion x-ray spectroscopy was performed (fig. 7, shown below) to determine the elemental composition of the stack layers. The circles indicate the spots from where the EDX spectra were taken. EDX spectra showed a high Arsenic content in the Si/SiO\textsubscript{x} layer with the X-ray peak intensities corresponding to a As/Si ratio of about 0.5 to 0.8. Thus, it can be concluded that the interface passivation layer is a partially oxidized SiAs alloy (14).

Fig. 7: EDX spectra indicate a high MBE-induced Arsenic content in Silicon passivation layer.

To probe the sub-surface chemical states, angle resolved X-ray photoelectron spectroscopy was performed on samples with no passivation layer and 1.5 nm thick a-Si layer. In angle-resolved X-ray Photoelectron Spectroscopy, the sampling depth d is given
by the product of mean free path and sine of the incident angle and in the experiment, the incident angle is varied from 24° (corresponding to bulk) to 82° (corresponding to sample surface). The figure shown below (fig. 8) is the As 2p spectra with and without 1.5 nm thick Si IPL. As can be seen from the XPS spectra, the oxidation state of Arsenic in Si-As-oxide is different from As-oxide. This is a clear indication that Arsenic is indeed present and is alloyed with Silicon in the interface passivation layer.

![Fig. 8: Angle-resolved XPS As 2p spectra from samples with and without Si passivation layer. The different oxidation states of As in AsO\textsubscript{x} and AsSiO\textsubscript{x} clearly indicate that As is present and is alloyed with Silicon.](image)

The figure shown below (fig. 9) is the XPS atomic concentration profile of a sample with 1.5 nm thick a-Si. The IPL is partially oxidized showing higher oxygen content at the surface with about 30-50% atomic percent of Arsenic in Silicon.
Fig. 9: XPS atomic concentration profile indicates about 30-50% atomic percent of Arsenic in Silicon.

Figure shown below (fig. 10) shows the profiles of covalent and oxidized silicon in the samples with different thicknesses of a-Si. The profile of SiO\textsubscript{x} is similar in all samples indicating that the thickness of SiO\textsubscript{x} is about 0.5 nm.

Fig. 10: Sample with 15Å thick amorphous silicon shows a strong signal of covalent Silicon at the interface.

The sample with 0.5 nm thick Si shows no Si increase with the angle indicating that there is complete oxidation throughout the entire Si thickness. The other two samples with 1
nm and 1.5 nm thick Si show an increase in the Si signal and in the 1.5 nm thick Si sample, Si signal is significantly stronger than the SiO$_x$ signal indicating that the presence of unoxidized or covalent Silicon at the interface is key to the prevention of Fermi level pinning. To further prove that covalent Si needs to be present at the interface, a sample with 1.5 nm thick a-Si was exposed in air for 20 mins. before loading into the XPS chamber and another sample was exposed to air for two weeks before loading into the XPS chamber. The figures shown below (fig. 11) show the XPS spectra and the corresponding CV characteristics.

Fig. 11: XPS spectra and corresponding CV characteristics of a sample exposed in air for 20 minutes and another sample exposed for two weeks. Presence of covalent silicon at the interface is key to prevent Fermi level pinning (as seen from the top graph) and thereby good n-type CV characteristics.
It can be seen that in the sample that was exposed for 20 mins, unoxidized silicon is present at the interface resulting in an unpinned Fermi level and good n-type CV characteristics. For the sample that was left for two weeks, Si was completely oxidized resulting in poor CV with high frequency dispersion and thus, a pinned Fermi level.

**Improvement in thermal stability of the gate stack with a-Si IPL:**

The following is a high resolution TEM image (fig. 12) of the high-k gate stack on MBE grown GaAs. The sample consists of 1.5 nm thick a-Si IPL, 4 nm HfO$_2$ and 200 nm thick TaN gate metal and the stack was annealed at 700°C in N$_2$ ambient for 5 mins.

![High resolution TEM image](image)

**Fig. 12:** High resolution TEM image of gate stack with 15A a-Si and 40A HfO$_2$ annealed at 700°C.

As can be seen from the TEM image, the gate stack is thermally stable up to 700°C with an atomically sharp interface between a-Si and GaAs and no intermixing of layers in the stack. Shown below (fig. 13) are the high frequency CV (1 MHz) and IV characteristics of the sample annealed at temperatures 600°, 700°, 800° and 850°C in an N$_2$ ambient for 5 mins. As can be seen from the CV plot, the sample shows well behaved
n-type CV characteristics up to 850°C. The leakage current density is seen to increase progressively with temperature with a maximum current density of about 1 mA/cm² after annealing at 850°C. It is to be noted that a similar experiment on a sample without a-Si passivation showed degraded CV and IV characteristics after annealing at 700°C. This improvement in the thermal stability of the gate stack due to the presence of a-Si passivation layer is advantageous because of the need to anneal the gate stack at high temperatures for activating the implanted species into the source and drain regions during the fabrication of a MOSFET.

Fig. 13: CV and IV characteristics of n-GaAs MOSCAPs measured on samples annealed at temperatures ranging from 600°-850°C. The gate stack is thermally stable up to 850°C even though the leakage current increases after 800°C anneal.

2.3 Depletion and Enhancement Mode GaAs MOSFETs with 1.5 nm a-Si and ex-situ PVD HfO₂

The ultimate proof for an unpinned Fermi level would be the demonstration of an inversion mode, Enhancement mode or a normally OFF MOSFET. In this case, the channel is inverted by the gate voltage thereby proving that the Fermi level can swing from the valence band into the conduction band. However, for the direct coupled FET
logic (DCFL) applications, both enhancement (positive $V_T$) and depletion (negative $V_T$) mode devices are required (15). In this logic system, the d-mode FET acts as a resistor for the enhancement mode MOSFET. Thus, it is important to demonstrate successful operation of both depletion (normally ON) and enhancement mode devices.

For a depletion mode device, an undoped 70 nm GaAs channel with a top AlGaAs layer (doped with Silicon to a concentration of $3E17 \text{ cm}^{-3}$) was grown by MBE on a semi-insulating GaAs substrate. A 1.5 nm thick a-Si passivation layer was grown in-situ followed by 3.6 nm thick PVD grown HfO$_2$. A 200 nm thick TaN gate metal was deposited by RF magnetron sputtering a Ta target in a N$_2$ and Ar ambient. Long channel devices were patterned by contact lithography followed by dry etch of the gate metal. A second lithography is performed to open windows for source and drain regions followed by dry etch of the gate oxide. The sample is cleaned by diluted HCl solution before loading the sample into the e-beam evaporator for Au-Ge-Ni Ohmic contacts. The contacts are formed by annealing the sample in nitrogen ambient at 400°C for 30 seconds. All measurements were performed using a Keithley semiconductor characterization system at room temperature.

The graphs shown below (fig. 14) demonstrate the input ($I_d-V_g$) and output ($I_d-V_d$) characteristics of 100 µm gate length GaAs channel with 3.6 nm HfO$_2$ gate oxide and TaN gate metal. The device turns ON at a threshold voltage of -0.7V with a subthreshold slope of 700 mV/dec. The device demonstrated a maximum transconductance of 3.6 mS (260 mS/mm scaled to a 1 µm channel). Additionally, the device demonstrated a good
control of the drain current by the gate voltage with a maximum mobility of 1100 cm$^2$/V.sec.

![Input (I_d-V_g) and output (I_d-V_d) characteristics of depletion mode GaAs MOSFET with a-Si IPL and HfO$_2$ gate oxide.](image)

The good control of the drain current by the gate voltage indicates the effectiveness of the a-Si passivation layer in reducing the density of interface states even though the device exhibits a high subthreshold slope. The low mobility and hence the low drive current which is inherent to GaAs channel MOSFETs suggests that high Indium content InGaAs channels is a better option for the realization of n-type III-V MOSFETs and are dealt with in detail in the next chapters.

In addition to a depletion type MOSFET device, it is important to demonstrate a normally OFF or an enhancement mode GaAs MOSFET. Enhancement mode MOSFET with GaAs channel with 1.5 nm a-Si passivation layer and 10 nm HfO$_2$ gate oxide were fabricated on semi-insulating GaAs substrates. The following figure (fig. 15) shows the cross-section of the structure.
The structure consists of a 70 nm thick GaAs undoped channel with a 100 nm thick AlGaAs barrier followed by a p-type AlGaAs layer doped with Carbon to a concentration of $2 \times 10^{17}$ cm$^{-3}$ resulting in a modulation doping in the channel to a concentration of $7 \times 10^{11}$/cm$^2$. The source and drain regions were implanted with Si$^+$ to a dose of $1 \times 10^{14}$/cm$^2$ at a dose of 50 keV. The following image is the high-resolution TEM image of the gate stack after annealing at 700°C. The 1.5 nm Si passivation layer is partially oxidized during deposition of HfO$_2$ resulting in a SiO$_x$ thickness of 1.9 nm (fig. 16).

Fig. 16: TEM image of the gate stack after 700°C anneal showing oxidation of a-Si IPL.

Target thickness of a-Si was 15Å.
The following plots (fig. 17) show the input characteristics, output characteristics and the gate leakage of a long channel (100 µm gate length) device.

![Graphs showing input and output characteristics and gate leakage of a long channel device.](image)

Fig. 17: Subthreshold (I_d-V_g) and output (I_d-V_d) characteristics and gate leakage of an enhancement mode GaAs N-MOSFET.

The device demonstrated a threshold voltage of +0.1V and a subthreshold swing of 170 mV/dec. corresponding to a interface trap density of 1.1E13 cm^2/eV. The device demonstrated a low gate leakage (30 nA) and a transconductance of 0.9 mS/mm – shown below, (90 mS/mm maximum transconductance scaled to a 1 µm channel) at a drain voltage of 4.5V. The effective channel mobility is 1000-2000 cm^2/V.sec (fig. 18) and is likely underestimated due to the over-estimation of the channel charge (16).
2.4 In-situ deposition of high-k gate stack

It has been shown that the pinning of the Fermi level at the interface between GaAs and an ex-situ deposited HfO$_2$ can be effectively prevented by a 1.5 nm thick in-situ deposited amorphous Silicon interface passivation layer. The a-Si IPL was thermally stable up to 800°C, thus minimizing the possibility of oxidation of the underlying GaAs. It was found that the a-Si layer is partially oxidized during ex-situ deposition of HfO$_2$, thereby contributing about 1.5 nm to the equivalent oxide thickness (EOT). In this section, a full in-situ process is demonstrated where the thickness of the a-Si IPL is reduced that results in significant reduction of the EOT. However, it has to be noted that even though the oxide is deposited in-situ, i.e. without breaking high vacuum, Si IPL is still required to prevent Fermi level pinning, that cannot be completely eliminated. However the IPL thickness can be reduced to 0.25 nm using a full in-situ high-k deposition process.
MOS capacitor (MOSCap) samples were grown on n-type and p-type (001) GaAs substrates, and semi-insulating substrates were used for MOSFET structures. The MOSCap structures consist of 150 nm thick doped \(2 \times 10^{18} \text{ cm}^{-3}\) buffer layer, followed by 80 nm GaAs layer doped with silicon at \(5 \times 10^{17} \text{ cm}^{-3}\) for n-type or carbon at \(5 \times 10^{17} \text{ cm}^{-3}\) for p-type capacitors. InGaAs MOSCaps have an additional 12 nm In\(_{0.2}\)Ga\(_{0.8}\)As doped with Si at \(5 \times 10^{17} \text{ cm}^{-3}\). For MOSFET the structures include undoped 150 nm thick buffer layer, a 100 nm Al\(_{0.3}\)Ga\(_{0.7}\)As barrier layer, portion of which was doped to \(5 \times 10^{17} \text{ cm}^{-3}\) with Si, and a 70 nm thick undoped GaAs layer for enhancement mode operation.

After the completion of MBE growth of the III-V group materials, amorphous Si interface passivation layer was deposited at room temperature \textit{in-situ} at 0.4 ML/min followed by in-situ deposition of a 10 nm thick HfO\(_2\) gate oxide using reactive electron beam evaporation at room temperature in an oxygen pressure of \(3 \times 10^{-6}\) Torr.

Samples with varying \(a\)-Si thickness of 0, 0.5, 1, 1.5 nm were grown for GaAs MOSCaps and of 0, 0.25, 0.5, 1 nm were grown for InGaAs devices to verify effect of scaling. All the samples were annealed at 600°C for 5 minutes (post-deposition anneal) in N\(_2\). A 200 nm thick TaN metal was deposited \textit{ex-situ} by physical vapor deposition (PVD) and the back contact was made with Indium. The TaN based Metal-Oxide-Metal (MOM) structures were fabricated to determine the dielectric constant of the \textit{in-situ} grown high-k gate oxide. For MOSFET structures, the source and drain regions were implanted with Si\(^+\) at 50 keV and a dose of \(1 \times 10^{14} \text{ cm}^{-2}\). The implanted species were activated in a rapid thermal anneal furnace at 750°C for about 10 seconds. Metal source/drain Ohmic contacts were made using Ni-Au-Ge alloy.
Cross-sectional transmission electron microscopy (TEM) image of the gate stack is shown below (fig. 19). The HfO$_2$ layer formed by \textit{in-situ} deposition and oxidation of Hf was found to be nano-crystalline with tetragonal/monoclinic distorted fluorite phase and appeared to be oxidized throughout the entire thickness. The interface between GaAs/Si is clean and atomically sharp with the Si layer being amorphous and uniform in thickness. Similar to the case of \textit{ex-situ} HfO$_2$ deposition, the $a$-Si layer is oxidized at least partially during \textit{in-situ} growth of HfO$_2$ indicating that the $a$-Si layer plays a critical role in preventing penetration of oxygen to the GaAs surface. Another important feature of the $a$-Si layer is the high content (up to 50 at. \%) of arsenic due to low growth rate of Si in the MBE chamber. Alloying with As and oxidation increase the total thickness of the IPL as seen in the TEM image.

Fig. 19: High resolution TEM image of the gate stack with $a$-Si IPL, 10 nm thick \textit{in-situ} e-beam deposited HfO$_2$.

Figure below (fig. 20) shows high frequency and quasi-static capacitance-voltage (C-V) characteristics of GaAs MOSCaps revealing a small stretch-out thus indicating an unpinned Fermi level, in contrast to a large stretch-out on a sample without Si
passivation, when GaAs surface is oxidized during HfO$_2$ deposition. The gate leakage current (shown below) measured on a GaAs MOSCap with 1.5 nm $\alpha$-Si and 10 nm HfO$_2$ was found to be as low as 5 µA/cm$^2$ at $V=V_{fb}+1$V.

Fig. 20: High frequency (1 MHz) and quasi-static CV measurements of n-GaAs MOSCAP with in-situ HfO$_2$ with and without a-Si. On the right is the IV measurements showing oxide breakdown.

An unpinned Fermi level was observed on both n-type and p-type GaAs MOS capacitors with $\alpha$-Si passivation: Figure below (fig. 21) shows the high frequency C-V characteristics on GaAs MOS Capacitors with 0.5 nm a-Si and 10 nm HfO$_2$. 

![Graph showing C-V characteristics and IV measurements.](image-url)
Fig. 21: High frequency (1 MHz) CV characteristics of n- and p-GaAs MOSCAPs with 5A a-Si and 10 nm in-situ HfO$_2$.

2.4.1 Reduction of Equivalent Oxide Thickness (EOT)

The n-GaAs MOSCAPs with 1.5 nm Si IPL demonstrated a maximum accumulation capacitance of 1.6 $\mu$F/cm$^2$ corresponding to an EOT of ~2.2 nm. The dielectric constant of in-situ HfO$_2$ was found to be ~26 as measured on TaN based metal-oxide-metal (MOM) samples with scaled HfO$_2$. To verify the effect of scaling, the samples with varying Si IPL thicknesses of 0, 0.5, 1, and 1.5 nm were grown on n-GaAs. From the figure shown below, it is seen that the capacitance in accumulation increases with decreasing $a$-Si thickness, resulting in a low EOT of 1.6 nm for samples with 0.5 nm Si IPL. Scaling of EOT is shown in the figure below. Comparing the EOT for samples with ex-situ and in-situ grown HfO$_2$, we find that by this in-situ deposition process, the EOT obtained is ~1.6 nm which approaches the value obtained on the MOM structures without any interfacial layer (fig. 22). Further reduction in EOT can be achieved by scaling down the oxide thickness.
Fig. 22: Amorphous Silicon scaling: CV characteristics of n-GaAs MOSCAPs with 0.5, 1 and 1.5 nm thick a-Si. EOT is reduced from 3.2 nm to 1.6 nm due to the in-situ deposition process of high-k oxide.

The effective passivation with an ultra-thin a-Si was also observed on InGaAs samples. MOS-Caps with an IPL as thin as 0.25 nm (shown below, fig. 23) show good C-V characteristics and it is observed that the hysteresis is independent of the Si IPL scaling, but scales with HfO₂ thickness and, therefore, is likely due to the charge present in the high-k oxide.
Fig 23: High frequency CV characteristics of n-InGaAs MOSCAPs with variable thickness of a-Si IPL. MOSCAP with a-Si as thin as 2.5Å shows good n-type CV behavior.

2.4.2 Improvement in thermal stability and suppression of Silicon in-diffusion (17)

In addition to the advantageous effect of a-Si scaling on EOT, the choice of appropriate a-Si thickness is critical to prevent Fermi level pinning due to oxidation of the III-V surface. That is why an ultra-thin a-Si layer is still needed to change the oxidation chemistry and as well as to behave as a barrier for oxygen penetration. On the other hand, if an a-Si layer is not completely oxidized (as shown below, fig. 24), it can serve as a source of donor impurities diffusing into III-V at elevated temperatures resulting in significant change of the dopant concentration. Silicon is a n-type dopant in GaAs and upon annealing at high temperatures tends to diffuse into the underlying semiconductor thereby resulting in an increase in the dopant concentration – as seen from the increase in the minimum capacitance of the CV graphs.
Fig. 24: GaAs N-MOSCAP with 15A thick a-Si. Increase in minimum capacitance, $C_{\text{min}}$, with anneal temperature indicating increase in dopant concentration due to the in-diffusion of Si into underlying GaAs

To investigate in-diffusion of Si to the III-V structure, p-type GaAs MOS capacitors with 0.5 nm and 1 nm Si IPL were grown and annealed at different temperatures. Figure below (fig. 25) shows that the samples with 0.5 nm thick Si demonstrated good C-V characteristics even after annealing at high temperatures, whereas the conductivity type was changed from p- to n-type in the case of the samples with 1 nm thick Si. This result indicates the effect of Si in-diffusion from un-oxidized Si layer and shows that the a-Si IPL should be entirely oxidized to prevent detrimental Si diffusion at high temperatures above 700 °C.

Fig. 25: GaAs p-MOSCAP with 15 A thick a-Si (left graph). Conductivity changes from p- to n-type as observed from CV characteristics indicating that Si (n type dopant) has diffused into p-GaAs. If Si thickness is 0.5 nm, entire Si layer is oxidized and CV remains p-type even after high temperature anneal.
2.5 Summary

The effective passivation of GaAs with an in-situ MBE grown amorphous Silicon passivation layer has been demonstrated. Further, it is shown that 1.5 nm thick a-Si is required to prevent oxidation of GaAs, thereby preventing Fermi level pinning for an ex-situ deposited high-k gate dielectric. It was seen that the presence of unoxidized Silicon or covalent Silicon is key to prevent Fermi level pinning even though a-Si layer gets partially oxidized during gate oxide deposition. The thickness of a-Si IPL can be scaled down to 0.5 nm using an in-situ high-k gate dielectric deposition process. In addition to reduction in the EOT, the thermal stability of the gate stack is seen to improve with scaling down a-Si IPL thickness.

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CHAPTER 3

Higher Mobility Channel Material: In$_x$Ga$_{1-x}$As

3.1 Metal-oxide-semiconductor capacitors and FETs: Fabrication procedure

The following section explains the general procedure used for the fabrication of MOS capacitors (MOSCAPs) and field effect transistors (MOSFETs). Samples are grown on 2” GaAs or InP substrates in ultra high vacuum (~1E-10 Torr) using a conventional effusion-source molecular beam epitaxy (MBE) reactor (Veeco Modular Gen II) equipped with an Arsenic cracker producing Arsenic flux. N-type doping is done with Silicon and p-type doping is done with Carbon. After the III-V growth, amorphous Silicon passivation layer is grown in-situ by MBE by heating a Silicon target and by maintaining the substrate temperature at ~ 100°C. For in-situ deposition of the oxide, 0.5 nm of a-Si is grown and HfO$_2$ high-k oxide is grown by e-beam evaporation of Hf target in an oxygen pressure of 2E-6 Torr. For other ex-situ oxides, namely ALD ZrO$_2$ and MBD LaAlO$_3$ and GdScO$_3$, the samples are further capped with a 200 nm thick Arsenic layer to prevent oxidation of the III-V surface. Arsenic is desorbed by heating the sample at 400°C before deposition of the oxide.

The samples are annealed in a N$_2$ ambient at temperatures ranging from 500°C to 800°C for 5 minutes to reduce the bulk defects in the oxide. Tantalum nitride (TaN) gate metal (~ 200 nm) is deposited by RF sputtering of tantalum target in an ambient of N$_2$ and Ar. TaN is used as a gate for both MOSFETs and MOSCAPs. After gate patterning
by contact lithography, TaN is dry etched using CF$_4$+O$_2$ chemistry. Other gate metals have been used including Ni, Pd and Al (to determine the effect of work function on flatband voltage in MOSCAPs) and these are deposited by e-beam evaporation of the metal target through a shadow mask. The MOSCAP device area varied from 4E-4 cm$^2$ to 0.0625E-4 cm$^2$.

For the fabrication of a MOSFET, the sample is further processed by implanting the source and drain regions with Si$^+$ ions at a dose of 1E14/cm$^2$ at an energy of 50 keV. Implantation activation is performed by annealing the sample in a rapid thermal anneal system at a temperature of 750°C for 15 seconds in a N$_2$ ambient. Source and drain regions are patterned using a second mask followed by etching of the gate oxide. Ohmic contacts are made by e-beam evaporation of Au-Ge-Ni (alloyed contacts) or Pd-Ge (non-alloyed) and the contact is formed by annealing the samples at 400°C.

The following picture (fig. 1) shows the plan view of a processed MOSFET sample.

![MOSFET sample](image)

**Fig. 1:** Optical image of a processed ring-like MOSFET showing gate, source and drain regions.

### 3.2 MOS Capacitors on InGaAs
3.2.1 Interface trap density by conductance method

Introduction:

Interface trap density ($D_{it}$) is an important parameter that is used to characterize oxide-semiconductor interfaces. The density of interface traps varies across the semiconductor band-gap and the accurate knowledge of the density of interface states is of paramount importance for qualifying any oxide-semiconductor system.

There are several factors that lead to deviation of the measured Capacitance-Voltage (CV) curves from the ideal model predictions. These factors are work function differences, oxide charges (interface trap charge, fixed oxide charge, mobile oxide charges and oxide trapped charge), poly-silicon depletion etc (1). The following cartoon (fig. 2) depicts the charges that are present in the gate oxide and at the oxide-semiconductor interface.

Fig. 2: Cartoon showing charges that are present in a MOS system [1]

The mobile oxide charges are due to ionic impurities such as Na, K etc. Oxide-trapped charge is due to trapped electrons or holes in the oxide bulk and maybe positive or negative and depends on the oxide thickness. The fixed oxide charge is primarily due to...
structural defects in the oxide film. Interface trap charges are positive or negative charges and are due to oxidation induced defects, metal impurities and other defects due to bond-breaking processes. In the case of III-V – high-k oxide system, the interface states are due to As-O, Ga-O bonds; Ga$^{3+}$, Ga$^{5+}$ ionic states etc. Unlike other oxide charges, interface-trapped charge is in electrical communication with the underlying semiconductor and can be charged or discharged by the application of gate voltage. In the case of Si-SiO$_2$ interface, $D_{it}$ can be reduced by annealing in a forming gas ambient whereas for a III-V – high-k oxide, some kind of a surface passivation scheme is necessary to reduce the density of the interface states. The following cartoon (fig. 3) shows the distortion of the CV curve (p-type semiconductor) that arises due to the presence of interface states and the associated circuit diagram showing the oxide capacitance, $C_{ox}$, in series with the semiconductor capacitance (a parallel combination of inversion capacitance, depletion capacitance, accumulation capacitance and capacitance due to interface states).

Fig. 3: Non-ideal capacitance-voltage characteristics of p-type semiconductor showing the distortion in the CV curve. The equivalent circuit of a MOS system with interface traps [1].
Measurement of Capacitance and Conductance:

Capacitance-voltage (CV) and conductance-voltage (GV) measurements are conducted on MOS structures where a gate voltage \( V_g \) is applied between the metal and semiconductor. The measurements consist of applying a small sinusoidal voltage with a frequency “f” (usually in the range of 100 Hz to 1 MHz) and amplitude of 50 mV (2) on top of the gate voltage. CV and GV measurements were performed at room temperature using a HP impedance analyzer.

The small periodic gate voltage causes the bands and the surface potential to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty (3). The traps will respond only if the characteristic response time is of the order of the measurement frequency “f” and contribute to the measured impedance. The following cartoon (fig. 4) shows the band diagram of an n-type MOS structure with a bias voltage applied between metal and semiconductor.
Fig. 4: Band diagram of a n-MOS structure with bias voltage applied between metal and semiconductor (3)

The ac voltage is applied on top of the gate bias, represented by the vertical arrows, which moves the bands and the Fermi level up and down, causing the traps within the oscillation amplitude (brighter shaded region) to periodically fill and empty. The filling and emptying of the interface traps allows for measurement of interface state distribution from CV measurements.

Conductance method relies on measurement of capacitance and parallel conductance of the MOS structure. The measured values of capacitance $C_m$ and measured value of conductance $G_m$ (measured in a parallel combination) contain all the contributions from the measured MOS structure. The following figures (fig. 5) show the measured equivalent circuit (of the measured set-up) of the MOS structure consisting of oxide capacitance $C_{ox}$, parallel capacitance $C_p$ and parallel conductance $G_p$.

![Equivalent circuit showing capacitance and conductance](image)

Fig. 5: Equivalent circuit showing capacitance and conductance (measured in a parallel setup) (3).
The following figure (fig. 6) shows the equivalent circuit consisting of oxide capacitance $C_{ox}$, depletion layer capacitance $C_d$, capacitance due to interface traps $C_{it}$, resistance due to interface states $R_{it}$ and series resistance $R_s$. The fact that the trap time constant varies strongly as a function of trap depth is modeled by putting a series of “n” trap capacitances and resistances in parallel.

![Equivalent circuit diagram](image)

**Fig. 6: Equivalent circuit including $C_{ox}$, $C_d$, $R_s$ and interface traps (indicated by a series connection of $R_{it}$ and $C_{it}$) (3)**

In the conductance method, interface traps are detected through the energy loss resulting from the changes in the occupancy produced by small variations in the gate voltage and this energy loss is measured as the equivalent parallel conductance $G_p$. In addition to the energy loss associated with capture and emission, interface traps also hold an electron for some time after capture which results in a capacitance $C_{it}$. 
The following figures (fig. 7) show the C-V characteristics of a p-type InGaAs with a-Si passivation layer and 15 nm thick GdScO$_3$ gate oxide. The capacitance was measured on devices with Ni gate metal deposited through a shadow mask and the area of the device ranged from 1E-4 cm$^2$ to 4E-4 cm$^2$ (100 x 100 micron and 200 x 200 micron pads). The figures show the C-V measured at a frequency ranging from 1 MHz to 500 Hz with the gate voltage swing of +2V to -2V. On the right side is G-V data measured on the same device measured as a function of frequency (ranging from 100 Hz to 1 MHz) at various bias voltages ranging from 0V to 1V (measured in depletion).

![Fig. 7: CV characteristics of p-InGaAs with GdScO$_3$ gate oxide and a-Si IPL. Top right is the conductance-voltage (G-V) measured at various bias voltages.](image)

There are several techniques to extract $D_{it}$ and some of them include Terman method, combined high-low frequency measurement, conductance method etc. In the Terman method (high frequency method), the $D_{it}$ is extracted by measuring the stretch-out in the high frequency CV curve and comparing it to the ideal CV curve. For III-V devices, this method can lead to large discrepancy because the room temperature CV can have significant contribution from the capacitance due to the interface states, hence CV needs
to be measured at low temperatures to “freeze-out” the interface states and therefore remove the contribution of C_{it}.

In the high-low frequency method, the D_{it} is extracted from a high frequency CV curve, but acquiring a true high frequency curve (without the contribution due to interface states) is often difficult and could result in under-estimation of D_{it} if 300°C measurements are used.

Both capacitance and conductance measurements contain identical information about interface states but greater inaccuracies arise in extracting D_{it} from capacitance and this is not applicable to conductance since it is directly related to interface traps.

**Conductance method: Principle**

In the conductance method, the admittance of the device is measured by a bridge (HP impedance analyzer) and the oxide capacitance is measured in strong accumulation (4). The admittance is converted into impedance and the reactance of the insulator capacitance is subtracted from the impedance and the resulting impedance is converted back into admittance. This results in depletion capacitance in parallel with the R_{s}C_{s} network of the interface states. At a given bias, G_{p}/\omega is measured as a function of frequency and the G_{p}/\omega curve goes through a maximum which is equal to C_{s}/2. Once semiconductor capacitance is known, D_{it} can be calculated by the equation D_{it} = C_{s}/qA where, A is the capacitor area and q, the charge.
In the conductance method, interface traps are detected by the loss that results from the change in the occupancy that is caused by the small variations in the gate voltage. This energy loss is measured as equivalent parallel conductance $G_p$.

### 3.3 $\text{In}_{0.20}\text{GaAs and GaAs/In}_{0.20}\text{GaAs channel MOS Devices}$

Surface passivation of GaAs with a thin in-situ MBE grown a-Si layer was demonstrated in chapter 2. In this chapter, primary focus is on a ternary III-V semiconductor, namely InGaAs. $\text{In}_x\text{Ga}_{1-x}\text{As}$ based channels are considered attractive due to the higher electron mobility compared to GaAs. (Electron mobility increases as the content of Indium increases with a simultaneous decrease in the bandgap. The bandgap of GaAs and InAs is 1.4 eV and 0.3 eV while the electron mobility changes from 4000 to 30,000 cm$^2$/V-sec. 53% Indium content InGaAs (lattice matched to InP substrate) has a bandgap of 0.75 eV and an electron mobility of about 10,000 cm$^2$/V-sec.)

The following figures (fig. 8) demonstrate the capacitance-voltage characteristics of two InGaAs MOSCAP sample with and without a-Si passivation layer. As can be observed from the CV curves, InGaAs samples without a-Si show good n-type CV behavior indicating an unpinned Fermi level or a weakly pinned Fermi level. It can be argued that InGaAs channels do not need any form of surface passivation but as can be seen from the CV behavior of InGaAs passivated with a-Si, the sample shows lower frequency dispersion indicating a lower interface trap density and lower hysteresis.
indicating lower oxide charge. The figure on the bottom shows the leakage current density of the two samples after annealing at 600°C, as can be seen from the IV measurements, the sample with Silicon passivation layer shows an order of magnitude lower leakage current indicating that the oxidized Si passivation layer (SiO$_x$) acts as a protection layer for the underlying gate stack from the high temperature anneal. Thus it can be concluded that even though high Indium content InGaAs channels does not need any interface passivation, passivating with a thin amorphous Silicon results in lower interface trap density at the band-edge and lower leakage current density.
Fig. 8: CV characteristics (top) of n-InGaAs MOSCAP with and without a-Si passivation layer and gate leakage current density (bottom) measured against gate voltage.

In this section, field effect transistors with low content Indium channels, namely In$_{0.20}$GaAs channels (grown on GaAs wafers) with a-Si IPL and ALD HfO$_2$ oxide are demonstrated (5).

The following are the results obtained on enhancement mode, inversion type MOSFETs with In$_{0.20}$GaAs surface channel and a GaAs/In$_{0.20}$GaAs buried channels. The III-V structures were fabricated by MBE on semi-insulating GaAs wafers and the following diagram shows the cross-section of an InGaAs surface channel MOSFET. The structure (fig. 9) consists of 15Å thick MBE grown a-Si IPL, 4 nm thick ALD HfO$_2$ gate dielectric and a 200 nm thick TaN gate metal. A carbon doped AlGaAs layer (2E17 cm$^{-3}$) was grown to provide modulation p-type doping to the 12 nm thick InGaAs channel. Buried channel devices consisted of a 3 nm thick undoped GaAs layer on top of the InGaAs channel. Ex-situ HfO$_2$ gate oxide was deposited by atomic layer deposition after 48 hours. Source and drain regions were implanted with Si$^+$ at an energy of 50 keV to a dose of 1E14/cm$^2$ and the implanted species were activated at 740°C in an rapid thermal anneal system in N$_2$ ambient. Aug-Ge based source-drain Ohmic contacts are deposited and the contacts are formed by annealing the sample at 400°C.
Fig. 9: Cross section of the structure used for InGaAs MOSFET with TaN metal gate and HfO$_2$ dielectric

The input and output characteristics of the surface channel In$_{0.20}$GaAs MOSFET are shown below (fig. 10). The device is a normally OFF transistor with a threshold voltage of +0.2V. The device exhibits good control of drain current by the gate voltage with low gate leakage current and an $I_{on}/I_{off}$ ratio of $10^3$ and a subthreshold slope of 290 mV/dec.

Fig. 10: Input and output characteristics of In$_{0.20}$GaAs surface channel MOSFET
The following figure (fig. 11) show the cross-section of GaAs/In$_{0.20}$GaAs buried channel device and the input and output characteristics.

Fig. 11: Cross section of the structure used for GaAs/InGaAs buried channel MOSFET with TaN metal gate and HfO$_2$ dielectric

Buried channel device architectures with a top barrier layer consisting of a semiconductor material (of a higher bandgap) have higher electron mobility compared to a surface channel due to three reasons:

1. Scattering due to surface roughness is minimized because of smooth interface with MBE grown top barrier in comparison to larger surface roughness due to an oxide
2. Better carrier confinement in the channel due to the high conduction band offset with the large bandgap semiconductor
3. Reduced effect of remote Coulomb scattering due to the presence of high-k gate oxide
The degradation of the electron mobility due to remote Coulomb scattering effect from a high-k gate dielectric is discussed below. Dielectric constant of a material is a result of the combined contribution of the electronic and ionic polarization. Electronic polarizability varies inversely with the bandgap of the material and due to the large bandgaps of high-k oxides, contribution from the electronic polarizability is minimal and therefore the dielectric constant of high-k oxides is primarily due to the ionic polarizability between the highly polarizable (soft) metal-oxygen bonds. Associated with soft metal-oxygen bonds are low-energy optical phonons and due to these low energy optical phonons, the effect of Coulomb scattering is maximum thereby resulting in large degradation of the carrier mobility. In contrast, in a low-k (k=3.9) dielectric such as in SiO₂, the hard Si-O bonds yield a reduced ionic polarization and effect of Coulomb scattering is minimal on the carrier mobility.

The buried channel InGaAs MOSFET device shown below demonstrated a threshold voltage of +0.65V indicating a normally OFF device. This device showed an \( I_{on}/I_{off} \) ratio of 50 and it has to be noted that the OFF current is limited by the PN junction leakage and not by the gate leakage. Additionally, this device has a poor subthreshold slope in comparison to the surface InGaAs channel indicating a much higher interface trap density. By measuring the gate-channel capacitance and by integrating the channel charge, the mobility on this device is estimated to be 450 cm²/V-sec at a sheet carrier density of 1E11 cm⁻².
Fig. 12: Input and output characteristics of GaAs/InGaAs buried channel MOSFET

The following (fig. 13) is a high resolution TEM image of the gate stack annealed at 750°C with 10 nm HfO$_2$, 0.25 nm a-Si interface passivation layer on InGaAs (developed by the in-situ process explained in chapter 2).

Fig.13: TEM image of gate stack showing 0.25 nm thick a-Si IPL and 10 nm HfO$_2$ on InGaAs.
Thus, demonstration of an enhancement mode, inversion type InGaAs surface and buried channel MOSFETs is further proof of an unpinned Fermi level and the effectiveness of the a-Si passivation layer in reducing the density of interface states.

It has to be noted that the top semiconductor barrier (dielectric constant ~ 12) results in additional contribution to the equivalent oxide thickness and careful optimization of the thickness of the top barrier is required.

3.4 Buried channel InAlAs/InGaAs MOSFETs

To prevent degradation of carrier mobility due to the remote Coulomb scattering effect due to a high-k gate oxide, employing buried channel architecture will significantly improve the carrier mobility and therefore improves the drive current. By growing a barrier layer on top of the InGaAs channel, typically with a higher bandgap III-V material such as InAlAs or InP (due to the large conduction band offset with InGaAs), electron mobility is shown to be significantly improved.

In this section (6), the electrical characteristics of In\(_{0.53}\)GaAs based buried channel MOSFET devices is discussed and the effect of a 2ML thick In\(_{0.53}\)GaAs grown on top of the InAlAs top barrier layer on subthreshold characteristics is discussed. The following (fig. 14) is the high resolution TEM image of the gate stack after annealing at 600°C with 200 nm thick TaN gate metal, 10 nm thick HfO\(_2\) gate dielectric, 5 nm thick In\(_{0.52}\)Al\(_{0.48}\)As top barrier, 10 nm thick In\(_{0.53}\)Ga\(_{0.47}\)As channel grown on InAlAs buffer
region. In this sample, the QW was directly doped with Si to a doping concentration of 1E18/cm³. Direct doping was used instead of modulation doping to improve source-drain contacts. Pd-Ge based Ohmic contacts were made by e-beam evaporation and sample was annealed at 400ºC.

Fig. 14: TEM image showing InGaAs QW with InAlAs top barrier, 10 nm thick HfO₂ and TaN gate metal

In₀.₅₂Al₀.₄₈As/In₀.₅₃Ga₀.₄₇As buried quantum well channel structures are grown by MBE. Lattice matched InAlAs is an ideal material due to the large conduction band offset with InGaAs but an Al containing top barrier layer results in pinning of the Fermi level at the semiconductor-oxide interface due to the oxidation of the top Al containing layer. To fabricate a buried channel with an InAlAs top barrier layer, the top barrier layer is usually covered with an Al-free layer which results in increased equivalent oxide thickness. In this experiment, the top InAlAs barrier layer is covered with 2ML of In₀.₅₃GaAs to prevent oxidation of InAlAs (during gate dielectric deposition) and the subthreshold characteristics of the two devices (with and without 2ML InGaAs layer) are discussed.
The following is the angle-resolved XPS spectra of the two samples, one with InAlAs top layer and another with InGaAs/InAlAs top layer. As depicted by the angle-resolved XPS spectra, the oxidation rate of InAlAs is 3-5 times faster resulting in a high density of As-O bonds that give rise to the high density of interface states. The As 2p spectra was taken from the sample after a 30 minute exposure to air. As-O bonds can be found within 0.7-1 nm in InAlAs, though InGaAs is oxidized within 0.2-0.3 nm.

Fig. 15: ARXPS spectra of InAlAs/InGaAs sample (top) and sample covered with 2ML of InGaAs on top of InAlAs
The following (fig. 16) are the input characteristics and of the sample with HfO$_2$ deposited directly on top of InAlAs. The device exhibits an $I_{on}/I_{off}$ ratio of ~ 10 with a subthreshold slope of about 2.2 V/dec corresponding to an interface trap density of 3E14/cm$^2$-eV (measured at the vicinity of the conduction band). It is important to note that the trap density obtained from the subthreshold slope is typically higher than the values obtained by capacitance-voltage of conductance methods.

The device has a high ON current, by linear scaling, the drain current is as high as 400 mA/mm for a 1 micron long channel at 1V with a maximum transconductance of 0.4 mS.

Fig. 16: Input, output characteristics of InAlAs/InGaAs buried channel MOSFET and graph (bottom) showing drain current and transconductance drawn on a linear scale.
In an effort to reduce the oxidation of the top InAlAs layer and to reduce the density of interface traps, the top barrier was covered with a 2 ML thick InGaAs layer while the rest of the structure was unchanged. The input and output characteristics of this device are shown below (fig. 17). In this sample, the subthreshold swing is significantly reduced down to 150 mV/dec. corresponding to an interface trap density of about 1.3E13 /cm²-eV near the conduction band. In addition to the reduced subthreshold slope, due to the reduced interface charge, the device operated as an enhancement mode device with a threshold voltage of + 0.15V

![Fig. 17: Input and output characteristics of InAlAs/InGaAs buried channel MOSFET covered with 2ML InGaAs layer.](image)

Gate-channel capacitance was measured (fig. 18) to determine the effective channel mobility. From the gate channel CV measurements, the large stretch-out of the CV curve of the sample with the gate stack deposited directly on InAlAs barrier is due to the high D_it which contributes to the surface charge when CV curve is integrated resulting in underestimated low field electron mobility. To separate the mobile and trapped charges, a correction method was used and the graph shown below includes the corrected mobility of the device.
Fig. 18: Gate-channel split CV measurements on InAlAs/InGaAs and 2ML InGaAs/InAlAs/InGaAs MOSFETs and the extracted mobility (right side graph). Star indicates hall mobility.

In order to verify the correction procedure, Hall mobility (at zero gate voltage) is also measured and is indicated by the star on the graph. This value, a Hall mobility of 1800 cm$^2$/V.s at a sheet carrier concentration of 3e12/cm$^2$ closely corresponds to the bulk mobility of InGaAs limited by ionized donor scattering with a doping concentration of 1E18/cm$^3$. This confirms that a high ON current can be obtained in a buried channel even with extremely high $D_{it}$ and the efficiency of a buried channel architecture to improve the channel transport. The result suggests the possibility of further reduction of barrier thickness and improvement in EOT.

### 3.5 Alternative Passivation of InGaAs: Aluminum IPL

As was shown in Chapter 2, section 2.4.3, if the thickness of Silicon IPL is more than 0.5 nm, high temperature anneal of the samples results in increased minimum capacitance indicating an increase in the dopant concentration of the underlying semiconductor. The
reason for the increase has been attributed to the in-diffusion of Silicon (Silicon being a n-type dopant in GaAs). This was further observed in p-type GaAs where the p-type CV characteristics changed into n-type CV after 700°C indicating a change in the conductivity of the semiconductor.

In an attempt to getter Silicon and therefore prevent any diffusion, a bi-layer passivation layer consisting of alternating layers of Silicon and Aluminum were deposited onto n-type GaAs and CV characteristics were measured. The figures below (fig. 19) show the frequency dispersion CV characteristics of two n-GaAs samples with just Si IPL and Si-Al bi-layer IPL annealed at 600°C. The bottom two graphs indicate high-frequency (1 MHz) CV of the two samples annealed at temperatures 600°C – 800°C. As can be seen, even though Si- Al bi-layer IPL shows a lower EOT, growing Al along with Si did not getter Silicon and did not prevent in-diffusion, as can be seen in the increase of the minimum capacitance in samples annealed at 700°C and 800°C anneal temperature.
Fig. 19: CV characteristics of n-InGaAs MOSCAP with Si IPL and Si+Al bi-layer IPL. Top graphs show frequency dispersion and bottom CV graphs show temperature dependence of CV characteristics.

Al bi-layer IPL shows a lower EOT, growing Al along with Si did not getter Silicon and did not prevent in-diffusion, as can be seen in the increase of the minimum capacitance in samples annealed at 700°C and 800°C anneal temperature.

In an attempt to completely eliminate Si as the passivation layer and thereby prevent in-diffusion into the underlying semiconductor and to test alternative passivation materials, amorphous Aluminum was grown by MBE immediately after III-V layer growth. The following graph (fig. 20) shows the effect of Al scaling on the EOT of n-GaAs MOSCAPs with 0.5 nm and 1.5 nm thick Al IPL. It can be seen that 0.5 nm of Al can be used to prevent oxidation of GaAs surface and therefore prevent pinning of the Fermi level.

Fig. 20: CV characteristics of n-GaAs MOSCAP with 0.5 nm and 1.5 nm thick Al passivation layer.
Further experiments were done on n- and p-type InGaAs samples with 0.5 nm Al passivation layer. The following figures (fig. 21) show the CV frequency dispersion, $G_p/\omega$ vs. frequency and interface trap density measured on p-InGaAs MOSCAP with HfO$_2$ gate oxide and Al IPL.

![Graph of CV characteristics](image1)

**Fig. 21:** Frequency dispersion of CV characteristics of p-InGaAs MOSCAP with 0.5 nm thick Al IPL, G-V characteristics measured at various bias voltages and extracted $D_{it}$ (bottom graph).

The CV characteristics measured on p-type InGaAs annealed at 700°C demonstrate large frequency dispersion indicating a huge density of interface traps at the edge of the valence band. Conductance-voltage measurements were performed on the sample parallel
conductance $G_p/\omega$ is plotted against omega ($= 2\pi f$). As can be seen from the plots above, the sample annealed at 700°C showed a lowest $D_{it}$ of $2 \times 10^{13}$/cm$^2$-eV which is almost an order of magnitude higher $D_{it}$ than the values observed in the case of p-InGaAs with a-Si IPL.

The following graphs (fig. 22) compare the n-InGaAs CV frequency dispersion on measured on samples with no passivation (a), Si IPL (b) and Al IPL (c). As can be seen from the frequency dispersion, Si IPL showed least frequency dispersion indicating least $D_{it}$ on Si passivated samples. However, accurate values of $D_{it}$ in the case of n-type InGaAs could not be extracted due to the fact that there was no clear peak in the $G_p/\omega$ curves measured at any bias voltage in depletion. This absence of a clear peak in the $G_p/\omega$ curves indicates that the generation and recombination through bulk traps is the dominant mechanism for the energy loss rather than the generation recombination through interface traps. In the case where generation and recombination through the bulk traps dominates the energy loss, a peak in the $G_p/\omega$ will not be observed because the loss due to this process is independent of the gate bias (7).

From the CV measurements on samples with no IPL, a-Si IPL and Al IPL, it can be concluded that a-Si resulted in unpinning of the Fermi level in addition to providing a low density of interface states both at band-gap and band edges.
Fig. 22: Comparison of CV characteristics (measured at various frequencies) of n-InGaAs without any passivation layer, a-Si IPL and Al IPL. Frequency dispersion is least on sample with a-Si IPL.

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CHAPTER 4
Integration of GaAs/ InGaAs with Alternative High-k Gate Dielectrics

4.1 Introduction

The excellent material and electrical properties of SiO₂ has resulted in successful scaling of CMOS technology up to the 45 nm technology node. Due to the exponential increase in the leakage current with reduced SiO₂ thickness, the semiconductor industry has replaced SiO₂ with a hafnium based high-k gate dielectric for the 45 nm node (1). There are several requirements for a material to be considered as a gate dielectric; namely, high dielectric constant, should remain amorphous even after annealing at high temperatures, possess large conduction and valence band offsets so that it behaves as a potential barrier for both electrons and holes, low density of defects in the bulk and also at the semiconductor-oxide interface, etc. Figure 1 demonstrates the variation of dielectric constant with bandgap of some gate oxides (2). It is interesting to note that the bandgap varies inversely with the dielectric constant. Therefore, it is advantageous to select an oxide with a large enough bandgap (~ 5-6 eV) and within the dielectric constant range of 20-30.

![Fig. 1: Electronic bandgap vs. dielectric constant of common dielectric materials](image_url)
Hafnium based dielectrics suffer from inherent disadvantages, namely, lower crystallization temperature, charge trapping which causes larger hysteresis and threshold voltage instability, lowered channel mobility due to remote coulomb scattering etc (3). Additionally, HfO$_2$ films are generally polycrystalline which increases the gate leakage current. For aggressively scaled gate lengths (sub 15 nm nodes and beyond), it is important to maintain a low equivalent oxide thickness (0.5 nm for a 6 nm long channel) so that a good electrostatic control of the device is maintained along with low leakage currents (4). Thus, it is necessary to evaluate alternative gate dielectrics which have a high dielectric constant and retain their amorphous nature after high anneal temperatures.

4.2 MBE grown rare-earth ternary oxides

Several recent publications on the integration of rare-earth ternary high-k dielectrics with silicon (5), germanium (6) and InGaAs (7) highlight the potential of gate oxides such as LaAlO$_3$, GdScO$_3$, LaLuO$_3$ etc. These oxides are considered promising due to their high dielectric constants ($k=20-31$), large optical bandgaps ($E_g>5eV$) and high conduction and valence band offsets ($\Delta E_c$ and $\Delta E_v > 2eV$ with Si). Additionally, these oxides maintain their amorphous phase up to high annealing temperatures (800$^\circ$C – 1000$^\circ$C) making them viable for gate-first MOSFET fabrication process.
Table 1: Roadmap from front end processes of ITRS: Rare earth ternary oxides are considered attractive alternative gate dielectrics for future technology nodes.

4.2.1 MBE Lanthanum Aluminate (LaAlO$_3$)

Table 1 is from the 2007 version of the front-end processes road-map of the ITRS. While the Hf based dielectrics would need further investigation, the ITRS proposes to undertake research activities in ternary oxides (8). As mentioned above, these rare-earth oxides distinguish themselves by their high thermal stability of the amorphous phase at high anneal temperatures. Table 2 shows a comparison of dielectric constants, bandgaps and band offsets of these oxides with Si (9).

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>$\kappa$</th>
<th>$E_g$ (eV)</th>
<th>Band offsets with Si (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>8.9</td>
<td>3.5  4.4</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>25</td>
<td>5.9</td>
<td>1.5  3.4</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>26</td>
<td>5.9</td>
<td>1.4  3.3</td>
</tr>
<tr>
<td>LaAlO$_3$</td>
<td>24</td>
<td>6.2</td>
<td>1.8  3.2</td>
</tr>
<tr>
<td>GdScO$_3$</td>
<td>23</td>
<td>5.2</td>
<td>2.0  2.5</td>
</tr>
</tbody>
</table>

Table 2: Comparison of dielectric constant, bandgap and band offsets (with Si) of gate dielectric materials.

4.2.1.1 GaAs MOSCAPs with a-Si IPL and MBE grown LaAlO$_3$

Device structure and MOS capacitor fabrication:
The samples consisted of 150 nm carbon doped buffer layer (2E18/cm³) followed by an 80 nm thick GaAs layer doped with carbon (5E17/cm³) using a conventional MBE reactor equipped with an As cracker producing As₂ flux. GaAs was grown on p-type (001) GaAs at 575C and then cooled down to 400C under As₂ flux and further down in vacuum. For in-situ passivation, two options were used, (1) in-situ deposition of a-Si followed by arsenic cap layer and (2) arsenic capping layer only. The Si IPL was grown at 100C substrate temperature. The samples were shipped to another MBE system where the arsenic was thermally desorbed in UHV at 300C and a 2 x 4 surface reconstruction was verified by RHEED before the growth of the oxide. Oxide growth is done at 100C in molecular oxygen at a background pressure of 2E-6 Torr followed by in-situ annealing at 340C in a mixture of molecular O₂ and O₃. Following the oxide growth, TaN gate metal was deposited ex-situ by PVD and the samples received a post metallization anneal ranging from 500C-800C for 5mins in N₂ ambient. MOS capacitors were fabricated by patterning the gate followed by dry etch of TaN and the back contact was made by soldering Indium.

Fig. 2: High resolution TEM image of gate stack with LaAlO₃/a-Si/GaAs after 800C anneal
Figure 2 is a high resolution TEM image of the gate stack annealed at 800C. It can be seen that the interface between the oxide and the underlying semiconductor is atomically sharp with no visible low-k interfacial layers. Capacitance-voltage measurements on the p-GaAs MOSCAPs show clear distinction between depletion and accumulation (fig. 3a) with a frequency dispersion in accumulation less than 5%/dec. The gate leakage on the sample that was passivated remains low at $J_g < 1\text{mA/cm}^2$ at $V=V_{fb}+1\text{V}$ even after 800C (fig. 3d) anneal while it is to be noted that there is a degradation in gate leakage after 700C anneal in samples that were not passivated with a-Si.
Fig. 3: (a) High frequency (1 MHz) CV characteristics of p-GaAs MOSCAP showing improvement in oxide capacitance, stretch out and hysteresis with anneal temperature. (b) Interface trap density measured on MOSCAPs with and without a-Si IPL measured as a function of gate voltage. (c) Progressive improvement in EOT with annealing – EOT measured on sample annealed at 800C sample has the same value of EOT on sample without a-Si. (d) Gate leakage vs. applied gate voltage on samples annealed at temperatures ranging from 600C to 900C.

Also, an improvement in the C-V characteristics with annealing is noticed in samples that were passivated with 0.5 nm thick a-Si. With annealing temperature, it can be seen that there is a progressive increase in accumulation capacitance while the hysteresis is almost negligible for the sample annealed at 800C in addition to an improvement in the C-V stretch-out. Interface trap density at the midgap measured by conductance method on the 800C sample is 2E11/cm²-eV, which is similar to the value measured on Si/High-k devices (fig. 3b). Also, the EOT measured on the passivated sample annealed at 800C is about 5.5 nm (fig. 3c) which is about the value measured on the sample without any passivation. Thus, it can be concluded that a-Si does not
contribute to the EOT and at the same time providing high thermal stability in addition to significant improvement in the oxide-semiconductor interface properties (10).

To further understand the role of a-Si in the improvement of electrical properties of MOSCAPs, TEM along with EDX studies were performed. The figure (fig. 4) shown below

Fig. 4: TEM and corresponding EDX spectra of LaAlO$_3$/a-Si/GaAs MOSCAPs annealed at 600C and 800C. SiO$_x$ layer between LaAlO$_3$ and GaAs visible on the 600C sample gets diffused at 800C into the oxide.

is the TEM image of two samples along with corresponding EDX spectra for samples with 1.5nm a-Si annealed at 600C and 800C. While a thin SiO$_x$ layer is visible at the interface on the sample annealed at 600C and confirmed by the corresponding EDX spectrum, the sample that was annealed at 800C shows no such interlayer. From the EDX spectra, the La and Si peaks are clearly separated after annealing at 600C whereas the Si profile overlaps with the La peak indicating diffusion of SiO$_x$ into the LaAlO$_3$ without
any diffusion into the underlying semiconductor. The increase in the accumulation capacitance and reduction in EOT can be explained by the fact that the low-k SiO\(_x\) diffuses into LaAlO\(_3\) at 800\(^\circ\)C and the contribution of SiOx to the EOT is minimized. Also, the presence of this interfacial SiO\(_x\) layer accounts for the lower gate leakage.

4.2.1.2 InGaAs MOS devices with MBE grown LaAlO\(_3\)

Due to the higher electron mobility of InGaAs compared to GaAs, focus of III-V research has shifted to InGaAs channel material. In this section, the LaAlO\(_3\)-In\(_{0.53}\)Ga\(_{0.47}\)As interface is assessed with a goal to demonstrate surface channel, inversion type, enhancement mode MOSFETs with a low density of interface traps. To reduce the interface trap density, a thin layer of a-Si passivation layer is employed which would also improve the thermal stability of the gate stack and to address the source-drain contact resistance problem, the implanted species was activated at a high anneal temperature. The following figure (fig. 5) shows the cross-section of the structure that was used to fabricate p-MOSCAPs and MOSFETs
Fig. 5: Cross section of the structure used for InGaAs MOSCAPs and MOSFETs with LaAlO$_3$ gate oxide.

The samples consisted of 150 nm thick carbon doped buffer layer followed by 80 nm thick InGaAs channel layer that was doped by carbon to a concentration of 2e17/cm$^3$. To determine the effect of a-Si passivation, a sample with 0.5 nm thick a-Si IPL and a sample without any passivation layer were grown. Both the samples were further capped with Arsenic to prevent surface oxidation while the samples are shipped to another MBE system for LaAlO$_3$ deposition. Before oxide growth, the samples were thermally desorbed at 300C and 15 nm thick LaAlO$_3$ was grown on the two samples followed by in-situ annealing in a mixture of molecular oxygen and ozone.

MOS capacitors were processed by depositing 150 nm of Ni through a shadow mask and the back contact was made by soldering Indium. The samples were annealed at a temperature range of 500C-700C after Ni metallization. MOSFET fabrication was done by growing a 200 nm thick TaN by sputtering a Ta target in a mixture of N$_2$+Ar plasma. Ring-like FETs are defined with gate length ranging from 3 microns to 50 microns and length to width (L/W) ratio of ~ 140 to ~ 10. The gate pattern was defined by contact lithography followed by TaN dry etch by a CF$_4$ plasma. Following the removal of TaN gate metal, the samples were implanted with Si+ ions (dose of 1E14/cm$^2$ and energy of 50 keV) into the source and drain regions followed by rapid thermal anneal at 750C for 15 seconds to activate the implanted species. The source and drain regions were further defined using a second mask and the gate oxide was effectively removed by a mixture of
dry etch (etching in CF$_4$+O$_2$ chemistry) and wet etch (by dipping the sample in 1:1 HCl for 2 mins). Source-drain Ohmic contacts were defined by electron beam evaporation of Pd/Ge followed by annealing the contacts at 400°C for 30 seconds in N$_2$.

![Diagram of MOSFET structure]

Fig. 6: Cross section of the InGaAs channel MOSFET and optical image of a processed ring-like MOSFET showing gate, source and drain regions.

The figures above (fig. 6) show the cross-section of the MOSFET structure with surface In$_{0.53}$GaAs channel with the implanted source and drain regions and the source-drain Ohmic contacts. The figure on the right is the optical image of fabricated ring-type MOSFET devices with the gate, drain and source regions.

Capacitance-voltage measurements on the two samples, a-Si passivated and non-passivated sample show good p-type CV behavior with a clear distinction between depletion and accumulation region indicating good control of the depletion width by the gate voltage. The two graphs shown below (fig. 7) depict the frequency dependence measured in the 1 MHz to 100 Hz range. The sample that was passivated shows lower frequency dispersion and smaller stretch-out in comparison to the non-passivated one indicating the effect of the passivation on the interface states and the reduction of interface trap density (Dit) at the edge of the valence band. In addition, the valley (difference between Cox and Cmin for 100 Hz CV curve) is much deeper for the a-Si
passivated sample indicating reduction of Dit at the mid-gap. Interface trap density was calculated by measuring conductance at different bias voltages measured in depletion. The Dit as calculated was in the range of $2 \times 10^{12} \text{cm}^{-2}\text{eV}$ on the passivated sample while it was of the order of $1 \times 10^{13} \text{cm}^{-2}\text{eV}$ on the non-passivated sample.

![CV characteristics measured on p-InGaAs MOSCAPs with and without a-Si passivation layer.](image)

Also, the passivated samples show a leakage current density of about $10 \text{ mA/cm}^2$ at $V_g=1\text{V}$ after 700C while the gate leakage degraded after 700C on the non-passivated sample. Thus it can be concluded that even though In$_{0.53}$GaAs surface does not necessarily need any surface passivation, passivating with a-Si results in lower Dit and lower gate leakage.

The effect of a-Si passivation is further seen on the electrical characteristics of surface channel InGaAs MOSFETs. Though both devices, a-Si passivated and non-passivated demonstrate good control of the drain current by the gate voltage, the sample that was not passivated shows significantly higher gate leakage due to the degradation of the gate stack by high temperature (750C) anneal. In comparison, the sample that was
passivated shows much lower gate leakage current resulting in an Ion/Ioff ratio of 1E4 while the Ion/Ioff ratio was ~ 300 on the non-passivated sample. The subthreshold characteristics of both samples are shown in the figure below (fig. 8).

These are inversion type, enhancement mode or normally OFF devices and both the devices show a positive threshold voltage of +0.2V and +0.4V. The subthreshold slope on the passivated sample is 140mV/dec. while the slope on the non-passivated sample is 300mV/dec (11).

Fig. 8: Subthreshold characteristics (Id-Vg) and Ig-Vg of InGaAs n-MOSFETs with and without a-Si passivation layer.

The subthreshold slope gives a direct measure of the interface trap density and depends on the temperature, oxide thickness and interface trap capacitance. The equation that describes these quantities is shown below:

$$ S = \frac{2.3kT}{q} \left(1 + \frac{C_d}{C_{ox}} + \frac{C_{it}}{C_{ox}}\right) $$

where, Cd is the depletion layer or space charge layer capacitance, Cox is the oxide capacitance given by the capacitance measured in accumulation and Cit is the interface
trap capacitance. From the above equation, the Dit is calculated to be $2\times10^{12}/cm^2$-eV and $1\times10^{13}/cm^2$-eV for the passivated and non-passivated samples respectively.

The output characteristics of the two devices are shown below (fig. 9) and as mentioned above, both devices show good control of drain current gate voltage. The channel resistance measured in the linear regime is 1.4 kΩ/sq. for the passivated and 1.6 kΩ/sq. for the non-passivated device. It is interesting to note that this value of channel resistance is 3X times higher than the channel resistance observed in a HEMT device.

![Output Characteristics of InGaAs MOSFETs with and without a-Si passivation](image)

**Fig. 9:** Output characteristics (Id-Vd) of InGaAs MOSFETs with and without a-Si passivation layer

Though the bulk mobility of In$_{0.53}$GaAs is about 8000 cm$^2$/V.sec at room temperature, the mobility in a surface channel device (in the proximity of a high-k oxide) gets significantly degraded due to several scattering mechanisms. The most prominent of them are remote coulomb scattering due to the proximity of the high-k dielectric, scattering due to surface roughness and possibly degradation due to the interface trap
density. Mobility of the electrons in the inversion channel can be determined in a MOSFET device by measuring the gate-channel capacitance and determining the inversion charge density and from the inversion charge density, the mobility can be extracted provided the geometry of the device is known. This method is commonly called as split-CV method and can be applied to fabricated MOSFET devices. The gate channel capacitance is measured by measuring CV between the gate and source-drain (shorting the source and drain terminals). The following are the equations that were applied to calculate mobility:

\[ Q_{\text{inv}} = \int_{-\infty}^{V_g} C_{\text{ge}}(V_g) dV_g \]

\[ \mu_{\text{eff}} = \frac{L}{W} \frac{J_d(V_g)}{V_d Q_{\text{inv}}(V_g)} \]

The following figure (fig. 10) shows the gate channel capacitance measured at a frequency range of 1MHz to 500 Hz and the calculated mobility.

![Fig. 10: Gate channel CV measured on InGaAs MOSFETs and the extracted mobility from split CV measurements.](image)

The shift in the flat band voltage of the CV plots with frequency can be attributed to charges in the bulk of the oxide and also to the interface trap charges. As seen from the mobility curve, a maximum mobility of 1500 cm²/V.sec was calculated. To further
understand the contribution of Dit towards the degradation in mobility, temperature dependent IV and gate channel measurements were performed at a temperature range of 77K-300K. The following figure (fig. 11) shows the subthreshold Id-Vg characteristics of both samples measured at room temperature and also 77K.

![Fig. 11: Id-Vg characteristics of InGaAs MOSFET measured at variable temperature range](image)

It is interesting to note that at 77K, both a-Si passivated and non-passivated sample show very similar subthreshold slope and hence the interface trap density must be similar on both samples at 77K. The mobility (fig. 12) measured on the passivated sample at room temperature is significantly higher than the mobility on the non-passivated sample. However, the mobility at 77K is seen to increase for the a-Si passivated sample and to decrease on the non-passivated device. A decrease in the mobility at lower temperature is a strong evidence of remote coulomb scattering due to the oxide and interface charges. An increase in the mobility at 77K indicates that the mechanism is weakened due to the presence of SiO\text{x} layer.
Fig. 12: Mobility extracted from InGaAs MOSFETs measured at room temperature and at 77K

To verify the effect of scaling the oxide thickness, Id-Vg measurements were performed on MOSFETs with 10 nm thick LaAlO₃. As seen from the plot below (fig. 13), the drain current and the maximum transconductance scale with the oxide thickness but there is no effect on the mobility implying that the reduced oxide charge in the sample with thinner oxide does not play a significant role in the degradation in the mobility.

Fig. 13: Drain current and transconductance measured on MOSFETs with LaAlO₃ oxide thicknesses of 10 nm and 20 nm.
Thus, it can be concluded that passivating InGaAs surface with a 0.5 nm thick a-Si interface passivation layer improves the leakage current and the interface trap density in comparison to the non-passivated InGaAs surface. Also, MOSFETs with a-Si passivation showed improved mobility due to the reduction in the strength of the remote interactions of the electrons with the high-k oxide. Additionally, it can be concluded that there is no significant effect of interface trap density and oxide charge on the mobility and the primary mechanism responsible for mobility degradation is remote coulomb scattering.

4.2.2 MBE Gadolinium Scandate

4.2.2.1 InGaAs MOS device with MBE GdScO$_3$

Gadolinium Scandate is a ternary rare-earth oxide with a dielectric constant of 23, a bandgap of 5.6 eV and conduction and valence band offsets to Si more than 2 eV. Moreover is has been shown that the oxide retains its amorphous phase up to anneal temperatures of 800C-1000C. In this part of the chapter, the integration of amorphous MBE grown GdScO$_3$ on In$_{0.53}$GaAs will be described. The structural properties of the gate stack, quality of GdScO$_3$/InGaAs interface and the effect of a thin a-Si interface passivation layer on key electrical parameters like gate leakage, equivalent oxide thickness (EOT) and the interface state density (Dit) will be discussed.

The details of III-V epi structure and the fabrication details of MOS capacitors and MOSFETs were discussed above in section 4.2.1.2. GdScO$_3$ gate oxide is grown by the co-deposition of Gd and Sc in oxygen ambient at a pressure of 1E-6 Torr with the ratio of
the metallic elements maintained close to unity. To determine the effect of a-Si passivation on GdScO$_3$/InGaAs interface, two samples – one passivated with a-Si and the other, without any interface passivation technique were grown and fabricated alongside. The figure shown below (fig. 14) is the high resolution TEM image of the gate stack annealed at 800C.

![High resolution TEM image of the gate stack with GdScO$_3$/a-Si/InGaAs annealed at 800C anneal](image)

Fig. 14: High resolution TEM image of the gate stack with GdScO$_3$/a-Si/InGaAs annealed at 800C anneal

The interface between InGaAs and the high-k oxide remains atomically sharp and the GdScO$_3$ film reveals the irregular contrast typical of amorphous materials. A very thin layer of SiO$_x$ is also visible at the interface resulting from the oxidation of the a-Si passivation layer.
Fig. 15: CV characteristics of p-InGaAs MOSCAPs with GdScO$_3$ gate dielectric. Sample passivated with a-Si shows lower frequency dispersion in accumulation.

The figure shown above (fig. 15) is the capacitance-voltage measurements obtained in the frequency range of 1MHz to 200Hz of the two samples annealed at 700C, with and without a-Si passivation (12). The samples that were passivated exhibit lower frequency dispersion (< 3%/dec.) in accumulation compared to the non-passivated sample indicating a reduced Dit at the valence band edge in addition to a reduced fixed oxide charge leading to a more positive flat band voltage. Also, the passivated sample revealed a lower EOT in comparison to the non-passivated sample. The dielectric
constant was measured from the physical thickness of the oxide film and the k value is determined to be 11 which is significantly lower than the k value of ALD deposited GdScO3 (k=23). The difference in the dielectric constants can be attributed to the stoichiometry of the thin film. Additionally, the a-Si IPL increases the thermal stability of the gate stack as seen from the gate leakage current density plot shown below (fig. 16). \( J_G \) is 1 mA/cm\(^2\) at \( V_g = -2V \) on the passivated sample and is two orders of magnitude lower than on the non-passivated sample.

![Gate leakage current density measured on MOSCAPs with and without a-Si passivation](image)

Fig. 16: Gate leakage current density measured on MOSCAPs with and without a-Si passivation

Interface trap density is determined by conductance method where Gp or parallel conductance is measured as a function of frequency for various bias voltages measured in depletion. The peak of the Gp/w gives a measure of the semiconductor capacitance from which the Dit can be calculated. The following graphs (fig. 17) show Gp/w vs. w for difference bias voltages.
Consider interface traps lie at a particular energy in the bandgap. For an appropriate band bending, the Fermi level corresponds to this energy and for this position of the Fermi level, a particular carrier density exists that determines the capture rate of these interface traps. If the applied small-signal frequency corresponds to this particular capture rate, a peak loss occurs. If the frequency is higher or lower, the loss is reduced because the interface traps fail to respond. Shown below (fig. 18) is Dit measured as a function of bias voltage for both the passivated and non-passivated samples. It can be seen that the midgap Dit on both samples is approximately 2E12/cm2-eV and the sample that has been passivated shows lower Dit at the edge of the valence band.
Inversion type, surface channel, enhancement mode MOSFETs with GdScO₃ were fabricated and the figures shown (fig. 19) below describe the input and output characteristics of the two devices, a-Si passivated and non-passivated samples. Both devices show very similar transistor parameters – threshold voltage of +0.3V, subthreshold slope of 130mV/dec, Ion/Ioff ratio of ~ 1E5 and transconductance of 65 mS/mm with the only notable difference being the gate leakage – the a-Si passivated sample shows significantly lower gate leakage current. It is to be noted that the OFF current is determined by the PN junction leakage for the a-Si passivated sample while the gate leakage determines the OFF current for the control sample. Both devices exhibit excellent control of the drain current by the gate voltage with a channel resistance of ~ 1.6kΩ/sq. measured in the linear region (13).

Fig. 18: Interface trap density as a function of bias voltage extracted from G-V measurements for GdScO₃/InGaAs MOSCAPs with and without a-Si passivation.

Fig. 19: Input and output characteristics of GdScO₃/InGaAs MOSFETs with and without a-Si passivation
The table shown below (table 3) benchmarks the channel resistance, subthreshold slope and the corresponding Dit (obtained from subthreshold swing) on surface channel, inversion type In_{0.53}GaAs MOSFETs with the same channel doping (3E17/cm^3) against various high-k gate oxides. The calculated values of Cit and Dit indicate the advantages of GdScO_3 over ZrO_2 and LaAlO_3 and also improvement of the interface quality due to the passivation of InGaAs with a-Si.

Table 3: Comparison of subthreshold swing, Dit extracted from subthreshold swing and channel resistance of ZrO_2/InGaAs, LaAlO_3/InGaAs and GdScO_3/InGaAs MOSFETs.

<table>
<thead>
<tr>
<th>Subthreshold swing (mV/dec)</th>
<th>Dit from Subthreshold swing (nA/cm^2-V)</th>
<th>Channel resistance in linear region (kΩ/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si</td>
<td>No a-Si</td>
<td>a-Si</td>
</tr>
<tr>
<td>5 nm ZrO_2</td>
<td>-</td>
<td>95</td>
</tr>
<tr>
<td>15 nm LaAlO_3</td>
<td>140</td>
<td>290</td>
</tr>
<tr>
<td>15 nm GdScO_3</td>
<td>130</td>
<td>160</td>
</tr>
</tbody>
</table>

In summary, the integration of molecular beam deposited GdScO_3 with In_{0.53}GaAs is demonstrated and it has been shown that GdScO_3 remains amorphous after 800C anneal making it suitable for a gate-first MOSFET fabrication process. Passivating InGaAs with a-Si significantly improved the thermal stability of the gate stack in addition to providing a lower EOT and reduced frequency dispersion in accumulation.

4.2.3 ALD Zirconium Oxide

From a commercial, high-volume manufacturing perspective, atomic layer deposition of high-k oxides is preferred in comparison to physical vapor deposition or molecular beam deposition. In addition, precursors for the ALD growth of ZrO_2 are well developed. In
this portion of the chapter, the integration of ALD ZrO$_2$ with In$_{0.53}$GaAs will be discussed including the electrical properties of NMOS and PMOS In$_{0.53}$GaAs capacitors and surface channel, inversion type, enhancement mode MOSFETs.

In$_{0.53}$GaAs n- and p-MOSCAPs with ALD ZrO$_2$

In the case of GaAs or 20% In content InGaAs, it has been shown that the Fermi level is pinned around the midgap. The main reason for the pinning of the Fermi level is due to the As-O and the presence of Ga$^{3+}$ states that are detrimental to the device performance. Unpinning of the Fermi level in this case is only possible through surface treatment or by insertion of a thin passivation layer. It has been previously shown that ammonium sulphide surface treatment or inserting a thin layer of amorphous Germanium or Silicon effectively passivates the surface. Here, we study the effect of ALD ZrO$_2$ on a bare higher Indium content (53% In or InGaAs lattice matched to InP) InGaAs and determine if In$_{0.53}$GaAs is a more robust material with respect to Fermi level pinning.

The epitaxial structure consists of 300 nm thick InGaAs layer doped with 3E17/cm$^3$ with Si for N-MOS and 3E17/cm$^3$ with Be for P-MOS is grown by MBE on top of InP substrate. ALD ZrO$_2$ is grown at 320°C by a metal-organic precursor and to study the scalability of oxide, variable thicknesses of 5nm, 7nm, 10nm and 15nm are grown. Post deposition anneal was performed at 350°C for 5min in NH$_3$ followed by in-situ deposition of 20nm thick TiN followed by ex-situ deposition of 200nm thick TaN by
physical vapor deposition. Post metallization anneal was performed in N\textsubscript{2} ambient at a temperature range of 500C-800C.

MOSCAPs were fabricated by making the gate pattern and etching TaN/TiN by dry etch in a fluorine based chemistry. Back side ohmic contact is made by soldering In onto the InP surface. To determine the effect of difference in the work function on the CV characteristics, three additional metals including Ti, W and Ni were deposited by electron beam evaporation through a shadow mask on InGaAs sample with 7nm thick zirconia.

Both n- and p-MOS capacitors showed good CV characteristics (fig. 20) with a clear distinction between depletion and accumulation regions indicating good control of the depletion width by the gate voltage (14). A small frequency dispersion of less than 5\% in accumulation was observed indicating an unpinned Fermi level.

![Fig. 20: Frequency dispersion of CV characteristics of n-InGaAs MOSCAP with ALD ZrO\textsubscript{2}. Inset shows 1 MHz CV of p-InGaAs MOSCAP with ZrO\textsubscript{2} gate oxide.](image)

The dielectric constant of the oxide can be determined by plotting the EOT against the thickness of the oxide and the slope of the line gives the k-value. As observed
from the figure shown below (fig. 21), the k value of ZrO$_2$ was determined to be $\sim 25$. The straight line of the EOT vs. thickness plot intersects the y-axis near zero, indicating the formation of a very thin, if any, low-k interfacial layer.

![EOT vs. Thickness Plot](image)

Fig. 21: Equivalent oxide thickness vs. ZrO$_2$ thickness. An EOT of 0.8 nm is measured for 5 nm thick ZrO$_2$.

The gate leakage current density vs. EOT is shown below (fig. 22) and it is observed that it scales with the oxide thickness. For an oxide thickness of 5 nm, the EOT was determined to be 0.8 nm and the gate leakage is reasonably low at $J_g = 0.1$ A/cm$^2$ measured at $V = V_{fb} + 1$V while the oxide breakdown occurs at 3V.

![Current Density vs. EOT](image)
Fig. 22: Gate leakage current density vs. equivalent oxide thickness measured on InGaAs MOSCAP without a-Si passivation. Inset shows leakage current measured on samples with variable oxide thickness of 5 nm, 10 nm and 15 nm.

TEM/EELS and XPS depth profiling were performed on the samples to get a better understanding of the interface quality and to see if the any oxidation of InGaAs occurs while oxide deposition. High resolution TEM image and EELS pattern shown below (fig. 23) indicate that the InGaAs/ZrO$_2$ interface is smooth and atomically clean without any interfacial layer. EELS analysis indicates that the Zr and O profiles reduce abruptly from the oxide region into the TiN layer, although some Zr and O signals can be observed close to the interface with TiN which could possibly be related to the surface roughness between the two layers. XPS depth profiling demonstrates very abrupt changes in the concentration near the surface and there is no shift of In, Ga and As peaks thus indicating no surface oxidation of the semiconductor.

Fig. 23: TEM image of the gate stack with EELS spectra. Zr and O profiles end abruptly at the interface from oxide region indicating that the semiconductor is not oxidized.
Shown below is a figure (fig. 24) demonstrating high frequency (1MHz) CV measurements on NMOS capacitors with different gate metals (Ti, W, Ni and TiN). It can be seen that flat band voltage is shifted towards more positive side for metals with higher work function which is a good indication that the Fermi level is rather unpinned on the these samples.

![Figure 24](image)

**Fig. 24:** High frequency CV of n-InGaAs MOSCAP with various gate metals. Shift in the flat band is seen due to the change in the work function of the gate metals.

In summary, the integration of ALD ZrO$_2$ with high-Indium content In$_{0.53}$GaAs is demonstrated. The small frequency dispersion of CV characteristics in addition to sensitivity of the flat band voltage to gate metal work function and good control of the electric field by the gate voltage seen on oxide scaling experiments provide solid evidence that the Fermi level is unpinned. It can thus be concluded that In$_{0.53}$GaAs is a much more robust material in comparison to GaAs or low content InGaAs with respect to Fermi level pinning.

**Surface channel, Inversion type, In$_{0.53}$GaAs Enhancement mode MOSFETs with ZrO$_2$**
The ultimate proof for an unpinned Fermi level would be demonstration of an enhancement mode MOSFET. In an E-mode device, the channel is normally OFF or there exists no channel at zero gate bias. For an N-MOSFET, the device turns ON for a positive gate voltage meaning that the surface potential is equal to more than twice the value of the bulk potential or the semiconductor under the gate is inverted from p-type to n-type at this gate voltage.

MOSFETs were fabricated on MBE grown p-In_{0.53}GaAs epitaxial layer on InP. ZrO$_2$ was grown by ALD followed by TiN/TaN gate metal deposition. After patterning the gate and dry etch of gate, the source and drain regions were implanted with Si$^+$ ions at an energy of 50 keV to a dose of 1E14/cm$^2$. The implanted species were activated at 700C for 10 seconds and using another mask, source and drain windows are defined followed by etching of ZrO$_2$. Pd/Ge based Ohmic contacts were made by e-beam evaporation and the contacts were annealed at 420C for 30 seconds. To determine the effect of oxide scaling on device performance, devices were fabricated on samples with 5 nm and 10 nm thick oxides.

High resolution TEM image shown below (fig. 25) of the gate stack annealed at 800C reveals atomically sharp interface between InGaAs and ZrO$_2$. The ZrO$_2$ film appears to be monoclinic at lower anneal temperatures while phase transformation at 800C to crystalline ZrO$_2$ is observed.
Fig. 25: TEM image of the gate stack after 800C anneal. ZrO$_2$ seems to have crystallized after high temperature anneal.

The following figures (fig. 26) show the subthreshold ($V_d = 50$mV) characteristics and transconductance for devices with 5 nm thick ZrO$_2$. The device is normally OFF and turns ON at a threshold voltage of $+0.25$V. The drain current increases with a subthreshold slope of 100 mV/dec. providing an Ion/Ioff ratio of 10,000. It is important to note that the OFF current is determined by gate leakage (15).

Fig. 26: Id-Vg and Ig-Vg characteristics of InGaAs MOSFET with ALD ZrO$_2$. Transconductance and drain current measured in linear regime is shown on the right side plot.
The output characteristics shown below (fig. 27) demonstrate excellent control of the drain current by the gate voltage with an Idmax of 160 mA/mm at Vg=1V with a channel conductance in linear region Gdmax equal to 490 mS/mm.

Fig. 27: Id-Vd characteristics measured on InGaAs MOSFET with ALD ZrO$_2$. Channel conductance measured in linear region is shown on the right side plot.

The following graph (fig. 28) shows the maximum drain current Idmax of 300mA/mm and maximum transconductance Gm max of 310 mS/mm measured in saturation region.

Fig. 28: Transconductance and drain current measured in saturation region on InGaAs n-MOSFET with ALD ZrO$_2$ gate dielectric.
Mobility on this surface channel device was extracted by split CV method where the gate channel capacitance is measured by shorting the source and drain and measuring CV between gate and shorted source-drain. The following graphs (fig. 29) show the gate-channel CV and the mobility obtained on this device. A maximum mobility of 2250 cm$^2$/V.sec at a sheet carrier density of 3E11/cm$^2$ was obtained.

Fig 29: Gate channel CV and the extracted mobility measured on ZrO$_2$/InGaAs MOSFET.

For low bandgap semiconductors such as In$_{0.53}$GaAs where the bandgap is 0.75 eV, band-to-band-tunneling can be significant source of leakage that could contribute to the OFF current. Under a strong applied electric field, electrons in valence band can tunnel through the forbidden bandgap and when they reach the conduction band, electron-hole pairs are created. To further understand the dominant leakage mechanisms that contribute to the OFF current, Id-Vg measurements were performed at a temperature range of 300K-77K and it is observed that at 77K, gate leakage is significantly reduced. To determine if the PN junction current also contributes to the leakage, the PN junction current was measured (shown below, fig. 30) and it is seen that the junction leakage is several orders of magnitude lower at lower temperatures. This indicates that gate leakage
and PN junction leakage current are primarily responsible for OFF current and band-to-band-tunneling component is only a small portion of junction leakage. In such a case, OFF current maybe related to defects caused while implantation or rather due to the existence of defects that are not annealed out by implant activation (16).

![Graphs showing reduction in OFF current with lowered temperature](image)

**Fig. 30:** Reduction in OFF current with lowered temperature as measured on InGaAs MOSFET with ZrO$_2$ gate dielectric. Gate leakage and junction leakage reduces with lower temperature indicating that OFF current may be defect related.

The following TEM image (fig. 31) of the source-drain regions confirms the belief that the defects that are caused by the high energy ion implantation are not annealed out by the thermal treatment. Thus it can be concluded that to achieve a high $I_{on}/I_{off}$ ratio, annealing out the end of range defects is necessary.
In summary, successful integration of ALD ZrO$_2$ with In$_{0.53}$GaAs was demonstrated. It has been shown that high Indium content In$_{0.53}$GaAs is a robust channel material which does not need any surface passivation. The sensitivity of CV characteristics to the gate metal work function together with a low frequency dispersion of CV indicates an unpinned or a weakly pinned Fermi level. The demonstration of an inversion type enhancement mode MOSFET is further proof that the Fermi level is indeed unpinned.

References:

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CHAPTER 5

Source-Drain Ohmic Contacts to InGaAs by MBE re-grown InAs

5.1.1 Introduction

Due to the low thermal stability of III-V semiconductors, GaAs and InGaAs channel MOSFETs cannot be subjected to high annealing temperatures. In conventional Silicon based MOSFET devices, source-drain regions are implanted with n-type dopants for the realization of N-MOSFETs and p-type dopants for P-MOSFETs and implant activation annealing is performed typically at 1100°C whereas for InGaAs, anneal temperatures more than 750°C is unsuitable. At such low activation temperatures, a very small percentage of implanted species get activated thus resulting in a high source-drain contact resistance. Unlike in Silicon based CMOS technologies, there are no equivalents to self-aligned silicides (salicides) for III-V materials but the same advantage can be achieved by self-aligned MBE re-growth of a heavily doped III-V semiconductor at the source and drain regions.

III-V semiconductor growth by Molecular Beam Epitaxy (MBE) permits high concentrations of dopants in shallow regions that can be in direct contact to the channel material. For example, InGaAs and InAs can be doped as high as 1E20/cm³ with Silicon (n-type dopant in III-Vs) and because of such high dopant concentrations, very low (contact resistivity less than 1E-8 Ohm/cm²) source drain contact resistances are envisioned [1]. In this work, heavily doped InAs (and graded InGaAs-InAs) is grown at
the source-dRAIN region after patterning the gate. InAs is chosen as the III-V material because in InAs, the Fermi level is pinned inside the conduction band [2] and theoretically there should be not be a Schottky barrier between the contact metal and re-grown InAs.

The components of source-drain (SD) series resistance are described below (fig. 1) with possible solutions to minimize the individual components.

Fig. 1: Components of source-drain resistance in a MOSFET: R1 is resistance between metal and re-grown III-V semiconductor, R2 is the resistance between re-grown III-V and InGaAs QW and R3 is the access region resistance.

Resistance R1 is the resistance between the metal and re-grown InAs. R2 is the resistance between InAs and InGaAs quantum well and R3 is the access region resistance.

The metal-semiconductor resistance (R1) depends on the sheet resistance of the re-grown InAs film, sheet resistance of the contact metal and the quality of the semiconductor surface. Heavily doped 50 nm thick InAs blanket (in-situ grown) films
typically have a sheet resistance of about 25 Ohms/sq. and the sheet resistance of the contact metal should roughly have an order of magnitude lower sheet resistance (about 5 Ohms/sq.). In this work, blanket InAs (50 nm thick) and gradient In$_{0.66}$GaAs-InAs films (20 nm graded InGaAs-InAs and 30 nm InAs) with a 9E19/cm$^3$ dopant concentration have shown sheet resistance values ranging between 15-30 Ohms/sq. The sheet resistance and surface morphology of the blanket film is shown to be heavily dependent on the growth temperature (temperature was varied from 420°C to 550°C). The contact resistivity of metal-semiconductor junctions have been shown to be less than 1E-8 Ohm/cm$^2$ for both in-situ [3] and ex-situ [4] deposited Ohmic contacts. Surface preparation prior to metal deposition has proven to be advantageous in lowering the resistivity for both InGaAs and InAs films. For ex-situ deposited metals, the surface is cleaned with NH$_4$OH solution and for in-situ deposited contacts, atomic hydrogen was employed [5].

The resistance of InAs-InGaAs junction (R2) could be high due to the large barrier between InAs and In$_{0.53}$GaAs. However, the built-in barrier can be controlled by grading the layer composition. It has been shown (fig. 2) that a graded InGaAs has a lower resistance in comparison to InAs-GaAs junction and an abrupt InAs-GaAs alloy [6].
In this work, the re-grown InAs layer consisted of 50 nm thick graded In$_{0.66}$GaAs-InAs layer. The resistance between the re-grown n$^{++}$ In(Ga)As and the InGaAs quantum well was measured by patterning TLM structures and by plotting the resistance between the pads as a function of the pad separation.

Access resistance (R3) or the resistance between contact and channel is another component of the series resistance and this is minimized by undercutting the pre-patterned gate by wet etching the semiconductor and then filling the under-cut with the re-grown In(Ga)As. In this proposed process, the re-grown In(Ga)As is in direct contact to the quantum well thus completely eliminating any access resistance. Unlike Atomic Layer Deposition or Chemical Vapor Deposition, Molecular Beam Epitaxy is a line-of-sight growth and the grown film can be non-conformal. However, using Migration Enhanced Epitaxy, the Indium adatom mobility can be increased [7] by increasing the
growth temperature (T ~ 520°C) and the undercut that is created by wet etch of InGaAs can be completely filled (fig. 3).

![Diagram of re-growth of InAs after InGaAs wet etch]

**Fig. 3**: Re-growth of InAs after InGaAs wet etch. Re-growth at the undercut is important to reduce access region resistance.

For enhanced nucleation especially at the under-cut, the wet etch is carefully optimized [8] to create smooth surface with good diffusion properties and simultaneously ensuring that the gate dielectric is not attacked by the wet chemistry. The resulting undercut due to the wet etch also ensures that the InAs film is discontinuous because of the overhanging gate stack. Using a HF:H₂O₂:H₂O wet chemistry, InGaAs can be etched reliably and reproducibly with an etch depth of about 75 nm. Thus a direct contact to the quantum well, which is typically 20 nm below the surface, can be achieved.

The following cartoon (fig. 4) depicts the process flow that is proposed for realization of an InGaAs quantum well channel MOSFET with MBE re-grown InAs source-drain regions.
Fig. 4: Proposed re-growth technology using a hard mask, re-grown InAs, lift-off and in-situ deposited metal contacts.

MBE is used to grow a 10 nm In$_{0.77}$GaAs QW channel with an InGaAs top barrier. Sheet resistance and sheet carrier concentrations are typically about 250 Ohms/sq. and 2E12/cm$^2$ respectively on such structures. After the III-V growth, a 10 nm thick HfO$_2$ gate oxide is grown in-situ by e-beam evaporation of Hf and followed by a 50 nm thick TaN gate metal. After the deposition of TaN, a 200 nm thick hard mask, either Si$_3$N$_4$ or SiO$_2$ is deposited by plasma enhanced chemical vapor deposition (PECVD).

After the gate is patterned, Si$_3$N$_4$/SiO$_2$ hard mask, TaN gate metal and HfO$_2$ gate oxide are dry etched in a CHF$_3$+O$_2$ and CF$_4$+O$_2$ chemistry such that the III-V layers remain untouched. After the dry etch process, InGaAs is wet etched such that an undercut is formed and simultaneously ensuring that the wet chemistry does not reach the underlying
InAlAs layer. The etch depth is roughly 75 nm when etched in a HF:H₂O₂:H₂O mixture (HF:H₂O₂:H₂O = 0.1:1:50) for 15 seconds.

The morphology of the re-grown In(Ga)As film heavily depends on the quality of the top InGaAs layer. Therefore, InGaAs surface was treated and tested with various acid and oxygen plasma treatment as well as base and oxygen plasma treatment and it was found that HCl+DI water (1:1) gave the best results (fig. 5) in terms of surface roughness of the re-grown In(Ga)As film. The following plan view FIB images show the surface morphology of the re-grown In(Ga)As film with different surface treatments:

![Surface Treatment Images]

Fig. 5: Effect of the surface treatment on the surface morphology of the blanket In(Ga)As film. HCl:H₂O (1:1) treated surface gave the smoothest morphology in comparison to other surface treatments.
After surface treatment, the sample is loaded into the MBE and 50 nm thick n++ In(Ga)As is grown. The sample is now transferred into a RF sputtering chamber without breaking vacuum via a transfer module where 50 nm thick TiW metal is deposited by sputtering a TiW target. The sample is now dipped in buffered oxide etch (BOE) and sonicated for lifting off Si$_3$N$_4$/InAs/TiW from the top of the gate ensuring that there is no electrical short between TaN gate metal and TiW source-drain contact metal.

In this work, surface morphology and resistivity of In(Ga)As films on both semi-insulating and p-doped InP substrates has been optimized. Additionally, strain related and surface preparation related morphology and the dependence on the MBE growth parameters have been evaluated. A source-drain re-growth technology is proposed which includes deposition of a Si$_3$N$_4$/SiO$_2$ hard mask, etching of the hard mask and the high-k gate oxide, wet etch of InGaAs, surface preparation before InAs re-growth and lift-off of hard mask. Also, the reverse junction leakage of p-n++ InGaAs/InAs junction has been measured and a relation between the surface morphology and leakage current is proposed. Finally, a low-resistance re-growth contact to both the surface and sidewall of InGaAs quantum well is demonstrated.

5.1.2 Growth optimization of In(Ga)As films

In order to obtain a low sheet resistance ($R_s \sim 20$ Ohms/sq.), low contact resistivities ($\rho_c < 1E-8$ Ohm-cm$^2$) and a smooth surface morphology, various samples with In(Ga)As blanket films were grown on both semi-insulating and p-type InP substrates. Growth
temperature was varied from 420°C to 550°C and migration enhanced epitaxy was used for all samples. All the samples consisted of a 2 nm thick In$_{0.53}$GaAs (NID) layer grown on a 340 nm thick InAlAs (NID) buffer on InP substrates. The top conducting layer consisted of a n$^{++}$ InAs or In(Ga)As layer that was doped with Silicon to a concentration of 9E19/cm$^3$. For some samples, bulk InAs was grown on top of In$_{0.53}$GaAs while on some samples, a graded structure was used; the structure consisted of a 20 nm thick InAs grown on a 30 nm thick In$_{0.66}$GaAs-InAs. The following table (table 1) describes the growth conditions, sheet resistance and the resulting surface morphology:

<table>
<thead>
<tr>
<th>#</th>
<th>Doped layer structure</th>
<th>Growth conditions</th>
<th>Sheet resistance, $\Omega$/sq.</th>
<th>Morphology</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-1292</td>
<td>20 nm InAs / 30 nm gradient In$_{0.56}$GaAs-InAs</td>
<td>MEE, 500C</td>
<td>25</td>
<td>Smooth InAs surface</td>
</tr>
<tr>
<td>N-1291</td>
<td>20 nm InAs/30 nm gradient In$_{0.56}$GaAs-InAs</td>
<td>MEE, 550C</td>
<td>62</td>
<td>Islanding of InAs</td>
</tr>
<tr>
<td>N-1290</td>
<td>6 nm InAs – 200C, No MEE / 45 nm InAs MEE 550C</td>
<td>MEE, 550C</td>
<td>83</td>
<td>Increased islanding of InAs at lower growth temp.</td>
</tr>
<tr>
<td>N-1289</td>
<td>50 nm InAs</td>
<td>MEE, 550C</td>
<td>16</td>
<td>Rough InAs surface</td>
</tr>
<tr>
<td>N-1288</td>
<td>50 nm InAs</td>
<td>MEE, 500C</td>
<td>20</td>
<td>Smoother InAs surface compared to N-1289, resembles &quot;orange peel&quot;</td>
</tr>
<tr>
<td>P-1141</td>
<td>20 nm InAs</td>
<td>MEE, 450C</td>
<td>150</td>
<td>InAs islands</td>
</tr>
<tr>
<td>N-1260</td>
<td>30 nm InAs</td>
<td>MEE, 450C</td>
<td>27</td>
<td>InAs islands</td>
</tr>
</tbody>
</table>

Table 1: Description of III-V structure, growth conditions and the resulting sheet resistance and surface morphology of blanket In(Ga)As films grown on semi-insulating InP substrates.

Sheet resistance was measured using a 4-point probe and the surface morphology was characterized by a SEM, cross sectional Focused Ion Beam (FIB) and high resolution transmission electron microscopy (TEM). The following images (fig. 6) show the surface morphology and cross section of the films grown at different temperatures:
Fig. 6: Plan view and cross sectional images showing the surface morphology of blanket In(Ga)As grown at temperatures 450°, 500° and 550°C by migration enhanced epitaxy.

As can be seen, 500°C growth temperature is optimum resulting in a smooth epitaxial film with a sheet resistance of 25 Ohms/sq. The following image (fig. 7) is the cross sectional FIB showing a surface roughness of ~10 nm.
Fig. 7: Cross sectional FIB image showing the surface roughness of blanket In(Ga)As.
Surface roughness is approximately 10 nm.

High resolution TEM images (fig. 8) of this sample are shown below:

Fig. 8: High resolution TEM images showing the high defect density in the InAs/gradient InGaAs layer.
As can be seen, the top In(Ga)As layer has a high defect density due to the softer nature of InAs.

For the measurement of reverse current leakage of n$^{++}$ In(Ga)As grown on p-type InGaAs, optimization of In(Ga)As films on p-type InP substrates was carried out. The following table (table 2) describes the sample structure, growth temperature and the measured sheet resistance. As can be seen, In(Ga)As growth on p-InP substrates is
markedly different than the growth on semi-insulating InP substrates. The lowest sheet resistance of 23 Ohms/sq. was obtained on a sample with a graded $\text{In}_{0.66}\text{GaAs-InAs}$ layer grown at a temperature of 455°C. The plan view of the samples seen under a FIB (at an angle of 52°) is shown below (fig. 9). As can be observed, the sheet resistance decreases with the growth temperature as well as the surface gets smoother with lower growth temperature.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Structure</th>
<th>Growth temp.</th>
<th>Sheet res. (Hall)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-1342</td>
<td>50 nm n=grad-InAs-InGaAs (~9e19cm-3) on p-InGaAs 0.5mm (2e17cm-3) on p+InGaAs 0.2mm (~2e18cm-3) on p-InP</td>
<td>520C</td>
<td>20 Ohms/sq</td>
</tr>
<tr>
<td>P-1141</td>
<td>20 nm InAs / 2nm In$_{0.53}$GaAs (NID) / 340 nm InAlAs (NID) / InP</td>
<td>MEE, 450C</td>
<td>150 ohms/sq.</td>
</tr>
<tr>
<td>P-1222</td>
<td>Same as N-1342, except, 5E16 cm-3 p-InGaAs on p-InP</td>
<td>520C</td>
<td>51 ohms/sq.</td>
</tr>
<tr>
<td>P-1224</td>
<td>20 nm InAs / 30 nm gradient In$<em>{0.56}$GaAs-InAs/2nm In$</em>{0.53}$GaAs (NID) / InAlAs (NID) / SI InP</td>
<td>520C</td>
<td>36 ohms/sq.</td>
</tr>
<tr>
<td>P-1225</td>
<td>Same as P-1222, except, growth temp is 20°C lower, on p-InP</td>
<td>500C</td>
<td>50 ohms/sq.</td>
</tr>
<tr>
<td>P-1226</td>
<td>Same as P-1224, lower growth temp, SI InP</td>
<td>485C</td>
<td>31 ohms/sq.</td>
</tr>
<tr>
<td>P-1227</td>
<td>Same as P-1222, growth temp. is 485°C on p-InP</td>
<td>485C</td>
<td>38 Ohms/sq</td>
</tr>
<tr>
<td>P-1228</td>
<td>Same as P-1222, growth temp is 470°C on p-InP</td>
<td>470C</td>
<td>32 Ohms/sq</td>
</tr>
<tr>
<td>P-1236</td>
<td>Same as P-1222, growth temp is 455°C on p-InP</td>
<td>455C</td>
<td>23 Ohms/sq</td>
</tr>
</tbody>
</table>

Table 2: Description of III-V structure, growth temperature and the resulting sheet resistance of blanket In(Ga)As films grown on p-InP substrates.
Fig. 9: Plan view images of blanket In(Ga)As grown on p-InP substrates showing surface morphology. Growth at 455°C gave the best surface morphology and lowest sheet resistance.

5.1.3 In-situ n++ In(Ga)As on p-InGaAs: PN junction leakage

The behavior of n++ InAs on p-InGaAs planar diodes and the dependence of the reverse leakage current on the surface morphology and sheet resistance of in-situ grown blanket InAs films is studied in this section. The samples consisted of 50 nm thick n++ In(Ga)As doped with Silicon to a concentration of 9E19/cm³ grown in-situ on top of 500 nm thick p-InGaAs doped to a concentration of 5E16/cm³ on top of 200 nm thick p+ InGaAs on top of p-InP substrates. The sheet resistance of the top n++ In(Ga)As layer depended on the growth temperature and surface morphology (as discussed in the section above) and varied from 23 Ohms/sq. to 51 Ohms/sq.
PN diodes were fabricated by patterning the sample using a single mask that consisted of squares with variable area ranging from $4\times10^{-4}$ cm$^2$ to $0.0625\times10^{-4}$ cm$^2$. After photo lithography, In(Ga)As layer was dry etched using a BCl$_3$+N$_2$ recipe such that mesas were formed with isolation ensured by the dry etch. Vertical current was measured by placing one probe on the diode and the other probe making an electrical contact to the substrate through Indium that was placed on the scratched back side of the wafer.

Current-voltage measurements were made in dark on ten devices of each area and the lowest leakage current from each area was plotted. The normalized leakage current density for various device areas as well as the leakage current per perimeter was plotted as a function of applied voltage. The following plots (fig. 10) demonstrate junction leakage for sample P-1236 which showed a sheet resistance of 23 Ohms/sq.

![Fig. 10: Reverse leakage current density measured on diodes with different area. Right side plot shows the leakage current per perimeter indicating that leakage is dominated by surface generation currents.](image-url)
As can be seen from the normalized diode area vs. voltage plot, the lowest PN leakage is 9.62E-5 A/cm² at V=1V. The total leakage current clearly scales with the diode perimeter rather than with the diode area, strongly suggesting that leakage is dominated by surface generation currents and not by bulk leakage component. This value of PN leakage is smaller than the leakage typically observed in Germanium junctions [9], where the leakage current is about 1E-3 A/cm².

Similar current-voltage measurements were carried out on n⁺⁺ In(Ga)As films (grown on p-InGaAs) that were grown at different MBE growth temperature. As mentioned in the previous section, the sheet resistance and surface morphology of the blanket In(Ga)As film depends heavily on the MBE growth temperature. Sheet resistance decreases and surface becomes smoother with lower growth temperature especially on p-InP substrates and it was seen that 455°C was the optimum growth temperature. PN junction leakage was also measured on two other samples, P-1228 and P-1222 – sheet resistance values of the top n⁺⁺ In(Ga)As films were measured to be 32 Ohms/sq. and 51 Ohms/sq. respectively. MBE growth was carried out at 470°C on P-1228 and at 520°C on P-1222. The following figure (fig. 11) compares the surface morphology, sheet resistance and the resulting PN leakage of the three samples:
Fig. 11: Comparison of reverse leakage current measured on samples grown at different growth temperature. Sample (P-1236) shows the smoothest surface morphology and the lowest leakage.

As can be seen from the plan view SEM images, the surface of In(Ga)As film is smoother on the sample that was grown at lower growth temperature (P-1236) in addition to lower sheet resistance and lower PN leakage in comparison to P-1228 and P-1222. It can thus be concluded that the surface morphology creates defect leakage paths and therefore PN leakage is highly dependent on surface morphology. It has to be noted that the doping concentration of p-InGaAs has been maintained constant at 5E16/cm³ in all the above three samples.
5.1.4 Ohmic contact to InAs

Ohmic contacts to III-V semiconductors are typically obtained by using a Au-Ge-Ni alloyed contact or a Pd-Ge non-alloyed contact. It has been shown previously that the contact resistivity depends heavily on the surface treatment and surface oxide or other contaminants can greatly increase the contact resistance [10]. In this work, Ohmic contact to blanket InAs have been studied both by depositing the contact metal by an in-situ process and also by an ex-situ process after surface treatment.

The sample consisted of 50 nm thick In$_{0.66}$GaAs-InAs (20 nm InAs on 30 nm gradient In$_{0.66}$GaAs-InAs) doped by Silicon to a concentration of 9E19/cm$^3$ grown on 2 nm In$_{0.53}$GaAs (NID) on 340 nm In$_{0.52}$AlAs buffer grown on InP substrate. The In(Ga)As layer was grown by migration enhanced epitaxy at 500°C growth temperature. The sheet resistance of the blanket In(Ga)As film was measured by 4 point probe the resistance is 25 Ohms/sq. E-beam lithography was used to define the TLM structures with gaps ranging from 100 nm, 300 nm, 500 nm, 1 micron, 3 micron and 5 microns as shown in the cartoon below (fig. 12). For in-situ deposition of contact metal, the sample is transferred under high vacuum into a sputtering chamber where TiW (10% Ti and 90% W) was deposited. For ex-situ deposition, the sample is brought out into ambient and the surface is treated by a 14.8 normal NH$_4$OH solution before loading the sample into the sputter tool for TiW deposition.
Fig. 12: Cartoon showing TLM pads patterned by using electron beam lithography. Spacing between the pads ranged from 0.1 to 10 microns.

For the fabrication of TLM structures, PMMA photoresist (positive tone, 140 nm thick) was used and e-beam patterning was done. TiW metal was dry etched using SF$_6$+O$_2$ chemistry. Isolation of the pads is done by patterning the sample using optical lithography using a mask that contained stripes. The following figures (fig. 13) show the plan view and cross section after dry etching TiW metal.

![Cross-section showing TiW etch](image)

Fig. 13: Plan view image showing TiW metal pads. Right side image is the cross section showing dry etch of TiW. Highly selective etch prevents sputtering of InAs.
Four point probe was used to measure TLM to reduce parasitic resistances. The following plots (fig. 14) show the TLM measurements on the in-situ TiW and ex-situ TiW samples:

![TLM plots](image)

Fig. 14: TLM measurements from samples with in-situ deposited TiW on InAs and ex-situ deposited TiW after surface treatment of InAs with NH₄OH solution.

As can be seen from the TLM measurements, Ohmic contact to InAs with an in-situ deposited TiW metal resulted in a contact resistance of 33 Ohm-micron, a transfer length of 0.4 micron and a contact resistivity of 1.3E-7 Ohms-cm². For the sample that was treated with NH₄OH (ex-situ), Ohmic contact with TiW metal resulted in a contact resistance of 60 Ohm-micron, a transfer length of 0.46 micron and a contact resistivity of 2.8E-7 Ohms-cm². It has to be noted that these values of contact resistivities are higher than what were reported by other groups primarily due to the reason that the sheet resistance of TiW is about 35 Ohms/sq. while the sheet resistance of the InAs blanket film is only 25 Ohms/sq. Ideally, to obtain contact resistivities in the order of 1E-8 Ohm-
cm$^2$ and below, the sheet resistance of the contact metal should be an order of magnitude lower than the sheet resistance of the semiconductor.

5.1.5 Resistance of InGaAs and re-grown In(Ga)As

As discussed in the introduction section, resistance between InGaAs quantum well (QW) and the re-grown In(Ga)As film could be high due to the large barrier between InGaAs and the re–grown InAs film. By growing a graded In$_{0.66}$GaAs-InAs film on top of InGaAs, the barrier can be minimized thereby obtaining very low values of contact resistance ($R_c \sim 100$ Ohm-micron) and contact resistivities (less than $1 \times 10^{-7}$ Ohm-cm$^2$). In this work, experiments were performed to determine the contact resistivities between the re-grown In(Ga)As film and surface of InGaAs QW as well as the sidewall of InGaAs QW.

The structure consisted of a 10 nm thick In$_{0.77}$GaAs QW with a 7 nm thick In$_{0.53}$GaAs top barrier grown on top of InAlAs and InP. Hall measurements on the sample gave a sheet resistance value of 251 Ohms/sq. and a sheet concentration of $6 \times 10^{12}$/cm$^2$. A 10 nm thick HfO$_2$ gate dielectric was grown on top of the III-V layers. In addition to the high-k oxide, a 200 nm thick PECVD Si$_3$N$_4$ or SiO$_2$ hard mask was deposited.

E-beam lithography defined TLM pads were patterned by using a 180 nm thick negative e-beam (NEB) photoresist. The gap between the 70x70 pads was varied from
100 nm, 200 nm, 500 nm, 1 micron, 2 microns and 5 microns. The figure below (fig. 15) shows the configuration of the patterned TLM pads.

<table>
<thead>
<tr>
<th>E-beam litho defined TLM pads</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1µm</td>
</tr>
<tr>
<td>Si₃N₄</td>
</tr>
<tr>
<td>PR</td>
</tr>
</tbody>
</table>

Fig. 15: Cartoon showing TLM pads defined by electron beam lithography. Spacing between the pads varied from 0.1 to 5 microns.

The following cartoon (fig. 16) explains the process flow for fabricating transmission line model (TLM) test structures for determination of contact resistance and contact resistivity.

Fig. 16: Process sequence used for measuring InAs-InGaAs resistance. First step involved dry etch of hard mask and gate dielectric followed by wet etch of InGaAs such that an undercut is created. In(Ga)As is re-grown after surface treatment followed by lift-off of InAs and hard mask (Si₃N₄ in this case).
After e-beam patterning, the sample is placed in a dry etch tool for etching the hard mask and HfO$_2$. A CHF$_3$+O$_2$ chemistry was used for selectively etching Si$_3$N$_4$/SiO$_2$ and a CF$_4$+O$_2$ chemistry was used to etch HfO$_2$. The etch process (plasma power, etch time etc.) was optimized for obtaining selectivity between the photoresist and hard mask. Though Fluorine based chemistry does not attack the underlying III-V layers, long exposures could result in sputtering of the top InGaAs layer. For contact to the QW surface, the sample was placed in the plasma for 20 extra seconds so that the top few nanometers of InGaAs gets sputtered. For contact to the sidewall of the QW, after the dry etch of hard mask and gate dielectric, the sample was wet etched in a HF:H$_2$O$_2$:H$_2$O chemistry (HF:H$_2$O$_2$:H$_2$O = 0.1:1:50) for 15 seconds such the an undercut is obtained with an overhanging gate stack.

For the undercut of the gate, a wet etch is preferred because a low pressure dry etch can result in an isotropic etch not forming an undercut with no selectivity in crystal planes. Additionally, Chlorine based dry etch does not offer selectivity between III-V and gate metal/high-k oxide. In order to obtain a smooth and clean surface and to obtain facets with known orientation so that Indium adatom migration is facilitated various acid based wet chemistries were tested including H$_2$SO$_4$+H$_2$O$_2$, H$_3$PO$_4$+H$_2$O$_2$, HCl+H$_2$O$_2$ and HF+H$_2$O$_2$. The following SEM images (fig. 17) show the profile of InGaAs etched in HF+H$_2$O$_2$+H$_2$O indicating smooth surface and pronounced [110] and [1-10] planes:
By reducing the concentration of HF and lowering etch time, 70 nm etch depth with a smooth undercut was obtained. The following image (fig. 18) shows the cross sectional FIB image after dry etching Si$_3$N$_4$ hard mask, HfO$_2$ oxide and after wet etching InGaAs.

Fig. 17: Etch profiles of InGaAs using a HF+H$_2$O$_2$+H$_2$O wet chemistry.

Fig. 18: Cross section FIB image showing dry etch of Si$_3$N$_4$ hard mask and HfO$_2$ gate oxide. Undercut created due to wet etch, etch depth is ~75 nm.
Using the above etch recipes for dry etching hard mask and gate oxide and wet etching InGaAs, In(Ga)As film was re-grown such that a contact to both surface and sidewall of InGaAs sidewall was made thus facilitating measurement of contact resistivity.

After the etching process, the remaining photoresist is removed by dipping the sample in 1165 remover and one minute long HCl + DI water (1:1) surface clean is performed before loading the sample into MBE for re-growth. A 75 nm thick n++ 9E19/cm$^3$ Silicon doped In$_{0.66}$GaAs-InAs layer is re-grown at 420°C.

**InAs contact to surface of InGaAs QW:**

The following figures (fig. 19) show (i) cross sectional FIB image after dry etching Si$_3$N$_4$ hard mask, HfO$_2$ gate oxide and dry etching (sputter) of InGaAs for contact to QW surface, (ii) plan view after lifting off InAs/Si$_3$N$_4$ by dipping in BOE and (iii) cross section image showing lift-off.

Fig. 19: Cross sectional FIB image after re-growth of In(Ga)As. The middle and the right-most images show the plan view and cross sectional view after lift-off of In(Ga)As and Si$_3$N$_4$. 
As can be seen from image (i), the re-grown film is continuous with no gap at the edge of the hard mask. Sheet resistance of the re-grown film is 20.25 Ohms/sq. as measured by a four point probe. The sample is dipped in BOE for about 10 minutes followed by sonication for 60 seconds. Figures (ii) and (iii) show the plan view and cross section after liftoff of In(Ga)As-Si₃N₄. As can be seen from the above images, there is a gap at the edge of Si₃N₄ hard mask after lift-off indicating that the BOE dip is too harsh and the gap can probably be mitigated by using a reduced concentration HF solution. However, this gap should not result in poor values of contact resistance as the re-grown film is making a contact to the surface of InGaAs QW.

Four point probe IV measurements were made on these TLM structures and the following are the results obtained (fig. 20):

![Figure 20](image)

Fig. 20: InAs-InGaAs TLM data measured on sample where contact to QW surface was made with re-grown In(Ga)As. A contact resistance of 0.2 Ohm-mm with a transfer length of 0.4 microns and a contact resistivity of 6E⁻⁷ Ohms-cm² was measured.
Contact resistance, sheet resistance of QW and contact resistivity values were extracted from the TLM measurements. It has to be noted that the following values were obtained from the second graph.

Calculations:
1. \( R_c = 2.9 \times 70 \text{ Ohm-microns} = 0.2 \text{ ohm-mm} \)
2. \( R_s = 5.7 \times 70 \), therefore, \( \rho_s = 399 \text{ ohms-sq} \).
3. Contact resistivity \( \rho_c \):
   \( 2L_T = 4.81/5.74 \), therefore \( L_T = 0.4 \text{ microns} \)
   \( L_T^2 = \rho_c / \rho_s \), therefore, \( \rho_c = (0.4 \text{ micron})^2 \times 399 \)
   therefore, \( \rho_c = 6.3 \times 10^{-7} \text{ ohm-cm}^2 \)

Thus a 200 Ohm-micron contact resistance, a sheet resistance of 400 Ohms/sq., transfer length of 0.4 micron and a contact resistivity of 6E-7 Ohms-cm\(^2\) were obtained. To determine the effect of annealing on contact resistivity, the sample was annealed at 450°C for 60 seconds in an N\(_2\) ambient and TLM was re-measured (fig. 21). As can be seen from the TLM data, the contact resistance and resistivity have indeed improved, yielding values of 77 Ohm-micron and 3.7E-7 Ohm-cm\(^2\).
Calculations:
1. \( R_c = 1.1 \times 70 \text{ Ohm-microns}, \text{ therefore } \quad R_c = 0.077 \text{ ohm-mm} \)
2. \( R_s = 2.13 \times 70 \), therefore, \( \rho_s = 149 \text{ ohms-sq.} \)
3. Contact resistivity \( \rho_c \):
   \[ 2L_T = 2.2/2.13, \text{ therefore } L_T = 0.5 \text{ microns} \]
   \[ L_T^2 = \rho_c/\rho_s, \text{ therefore, } \rho_c = (0.5 \text{ micron})^2 \times 149 \]
   \[ \text{therefore, } \rho_c = 3.7 \times 10^{-7} \text{ ohm-cm}^2 \]

Fig. 21: TLM measurements on the sample after annealing at 450°C in \( \text{N}_2 \) ambient

**InAs contact to sidewall of InGaAs QW:**

A similar experiment was repeated on the sample with PECVD SiO\(_2\). After dry etch of hard mask and gate oxide, the sample was further wet etched to create an undercut such that the re-grown InAs film would make a contact to the sidewall of the InGaAs quantum well. The following images show the cross sectional images after dry and wet etch and after re-growth.
Fig. 22: FIB cross sections showing (i) gate region after dry etch of hard mask and wet etch of InGaAs, (ii) image showing after In(Ga)As regrowth and (iii) plan view showing a gap at the edge of SiO$_2$ hard mask.

Figure (i) shows the cross section after dry etch and wet etch of InGaAs, a clear undercut with an etch depth of ~75 nm is seen, figure (ii) and (iii) show the plan view and cross sectional views after In(Ga)As re-growth. 75 nm thick n++ In$_{0.66}$GaAs-InAs was grown at 420°C. As can be seen the re-grown In(Ga)As film does not grow at the edge of the SiO$_2$ and at the undercut indicating that SiO$_2$ (and Si$_3$N$_4$ materials) push away the Indium adatoms from the edge. This would result in poor values of contact resistance as there is no contact between the re-grown InAs film to the sidewall of the QW. The following TEM images (fig. 23) confirm the speculation that regrown In(Ga)As does not fill the under-cut resulting in high values of contact resistivity.

Fig. 23: TEM images showing the gap between the dummy gate and re-grown In(Ga)As.
Due to the ~ 100 nm gap between the InGaAs quantum well and re-grown In(Ga)As, there exists an access region resistance giving rather high values of contact resistance ($R_c = 420 \text{ Ohm-micron}$) and contact resistivity ($\rho_c = 9.2 \times 10^{-6} \text{ Ohm-cm}^2$) as shown in fig. 24.

**Summary:**

In summary, the individual components of source-drain resistance in an InGaAs channel MOSFET have been addressed. Owing to the low thermal stability of III-V materials, S/D contact resistance is typically high due to the small percentage of activated implanted species. In this work, heavily doped InGaAs-InAs has been re-grown at the source and drain regions by introducing the sample into the MBE after defining the gate. A process
flow that includes deposition of a Si$_3$N$_4$/SiO$_2$ hard mask on top of the gate metal, dry and wet etching of hard mask and InGaAs to form an undercut, re-growth of In(Ga)As by migration enhanced epitaxy and lift-off of hard mask and re-grown In(Ga)As has been proposed for developing InGaAs channel MOSFET with re-grown S/D contacts.

The surface morphology and resistivity of In(Ga)As films on both semi-insulating and p-doped InP substrates has been optimized. Additionally, strain related and surface preparation related morphology and the dependence on the MBE growth parameters have been evaluated. Additionally the reverse PN junction leakage between n$^{++}$ In(Ga)As and p-InGaAs has been determined.

Ohmic contacts to InAs by both in-situ and ex-situ methods of metal deposition have been studied and finally, the resistance between InGaAs QW and re-grown In(Ga)As has been determined.

References:

(3) A. K. Baraskar, M.A. Wistey, V. Jain, U. Singisetti, G. Burek, B.J. Thibeault, Y.J. Lee, A.C. Gossard, M. Rodwell, “Ultralow resistance, nonalloyed Ohmic contacts to n-InGaAs”, JVST B 27, 4, Pg. 2036-2039


(8) Wet and Dry Etching of Compound Semiconductors – S. Pearton, chapter 8, “Handbook of Compound Semiconductors” edited by P. Holloway and G. McGuire

Due to the fundamental material limitations of Silicon based channels, alternative channel materials like Germanium, group III-V based compound semiconductors such as InGaAs, InGaSb etc., Carbon Nanotubes and Graphene are being extensively researched as a solution for 15 nm technology node and beyond (1). Owing to the superior carrier transport properties such as mobility and injection velocity, group III-V semiconductors are considered attractive channel materials for CMOS devices. Additionally, III-V based High Electron Mobility Transistors (HEMTs) are being used in Analog applications, therefore it is safe to conclude that III-V device physics is well understood and III-V device process technology is mature in comparison to CNT or Graphene. In this thesis, we have developed III-V Metal-Oxide-Semiconductor technology that incorporates an in-situ MBE grown amorphous Silicon interface passivation layer that has been shown to effectively reduce the density of interface states and thus prevent Fermi level pinning in GaAs and InGaAs.

6.1. Conclusions

(i) In chapter 1, the major technological breakthroughs that kept the Moore’s law alive, namely the introduction of strain in a conventional Silicon channel and introduction of the high-k metal gate technology are briefly explained and the concept of using alternative channel materials like group III-V semiconductors is introduced. A commonly
used group III-V based electronic device namely the high electron mobility transistor is explained outlining the advantages of III-V materials. Additionally, the major differences between a HEMT and metal-oxide-semiconductor field effect transistor (MOSFET) are explained and the reasons why a HEMT cannot be used for a low power, high performance application such as a microprocessor are discussed. The several advantages in using III-V materials and also the challenges that need to be overcome so that III-V MOS becomes a mainstream technology are discussed.

(ii) In chapter 2, the primary challenge that is encountered with development of III-V MOSFETs, namely, the high density of interface traps that results in Fermi level pinning is discussed. In order to prevent Fermi level pinning, the surface of GaAs needs to be passivated, in this chapter, the various interface passivation techniques are discussed and the key feature of this work which is the interface passivation using an amorphous Silicon layer is discussed in detail. To better understand the interfacial chemistry including the bonding information, various analytical techniques such as TEM, EDX and ARXPS have been used and the correlation between the analytical and electrical data is obtained. Metal-oxide-semiconductor capacitors (MOSCAPs) on n- and p-type GaAs with a 1.5 nm thick a-Si and 10 nm thick HfO$_2$ high-k gate dielectric are fabricated and CV and IV characteristics are measured as a function of a-Si thickness. Depletion mode and enhancement mode n-MOSFET on GaAs with HfO$_2$ gate dielectric, TaN gate metal, implanted source-drain regions and Au-Ge based Ohmic contacts is demonstrated. The thickness of a-Si layer can be scaled down if the gate dielectric is deposited by an in-situ process and the advantages of an in-situ high-k
deposition process in terms of EOT, thermal stability of the electrical properties are explained. Finally, an enhancement mode GaAs MOSFET with 0.5 nm thick a-Si, 10 nm thick in-situ deposited e-beam HfO$_2$, TaN metal gate, Si$^+$ implanted source-drain regions and Au-Ge metal Ohmic contacts is demonstrated.

(iii) A higher mobility channel material namely, InGaAs is introduced as the channel material in this chapter and the effect of passivating InGaAs with a-Si is studied. Enhancement mode MOSFET devices with a In$_{0.20}$GaAs surface channel and a GaAs/In$_{0.20}$GaAs buried channel architecture is developed. Higher Indium content containing channels, In$_{0.53}$GaAs buried channels with a top InAlAs barrier is designed and MOSFET is fabricated and the electrical characteristics are measured. The effect of adding a 2 ML thick InGaAs layer on top of the InAlAs top barrier is studied and the improvement in the electrical characteristics namely, subthreshold slope, threshold voltage and Ion/Ioff ratio is examined. Lastly, measurement of the interface trap density by the conductance method is explained including the underlying physics of the technique is discussed. As an effort to study alternative passivation layers, amorphous Aluminum is grown by MBE and the effect of a Si IPL, Al IPL and no passivation layer on the CV characteristics of n-InGaAs MOSCAPs is studied.

(iv) The integration of high mobility channel materials such as GaAs and InGaAs with alternative high-k gate oxides is discussed in chapter 4. High-k ZrO$_2$ is an attractive
candidate to replace HfO$_2$ due to its similarity to HfO$_2$ in addition to a slightly higher dielectric constant. In this chapter, MOSCAPs on n- and p-type In$_{0.53}$GaAs with ALD grown ZrO$_2$ is demonstrated including the effect of scaling down thickness of gate oxide on electrical parameters is studied. High resolution TEM, EELS in addition to CV, IV characteristics of MOSCAPs and enhancement mode MOSFETs are studied to qualify ZrO$_2$-InGaAs system. Among the future high-k gate dielectric candidates, ternary rare-earth oxides such as LaAlO$_3$ and GdScO$_3$ are considered attractive because of their ability to retain their amorphous nature even after high temperature anneals, high dielectric constants and large band offsets with the semiconductor. In this chapter, amorphous LaAlO$_3$ and GdScO$_3$ are deposited by molecular beam deposition on both GaAs and InGaAs channels. CV and IV characteristics of p-GaAs MOSCAPs and the effect of annealing on the electrical characteristics are thoroughly investigated. High resolution TEM, EELS, EDX are some of the analytical techniques that were used in addition to electrical characteristics of MOSCAPS. Surface channel, inversion type, enhancement mode n-MOSFETs with In$_{0.53}$GaAs channel and amorphous LaAlO$_3$, GdScO$_3$ are fabricated and the effect of a-Si IPL on the electrical characteristics of MOSFETs is studied in detail.

(iv) The advantage of incorporating a high mobility channel material is lost if the MOSFET device has poor contact resistance. To improve source-drain contact resistance, self-aligned re-grown InAs source-drain regions are developed in chapter 5. Due to the low thermal stability of III-Vs, these materials cannot be subjected to high temperature activation (implanted source-drain species)
anneals (~ 1100C) that is typically seen in a Si based system. Heavily doped InAs is chosen as the material because the Fermi level resides in the conduction band and there would be no Schottky barrier at the InGaAs-InAs interface. Migration enhanced epitaxy is used to improve the surface morphology and to obtain a smooth and continuous InAs film. Growth conditions are optimized as a function of growth temperature for both p-Inp and semi-insulating InP substrates. PN junction leakage of the in-situ blanket n++ InAs film grown on a p-InGaAs channel is measured and a correlation between the PN leakage current and surface morphology of the InAs film is made. Finally, the contact resistance between the InAs film re-grown on top of a n-InGaAs quantum well surface and also contact to the sidewall of the quantum well is measured.

6.2 Future directions

(i) III-V CMOS:

High mobility, alternative channel CMOS based devices would require both NFET and PFET on the same substrate. InGaAs based channel materials are a good option for realizing NMOSFETs due to the superior electron transport properties. However, due to the high hole effective mass and the resulting poor hole mobility, InGaAs based p-channels would not meet the requirements for designing a circuit. The highest hole mobility ever reported for an InGaAs channel is about 450 cm²/V.sec (2) and
this value of mobility is about 10X lower than InGaAs electron mobility and typically, an electron to hole mobility ratio of 3:1 is required to design an inverter circuit such that the device geometries are within the acceptable limits.

As an alternative to InGaAs p-channels, researchers from IMEC have successfully integrated (3) a Germanium based p-channel and the paper shows an architecture that incorporates an InGaAs n-channel and Germanium based p-channel grown epitaxially on the same substrate. Another viable option is to use an Antimonide based material system to realize III-V N- and P-MOSFETs (4). GaSb and InGaSb are III-V compound semiconductors with a hole mobility of about 1500 cm²/V.s (5). Recent papers have shown the integration of enhancement mode P-MOSFETs with an InGaSb p-channel and Al₂O₃ gate dielectric with good transistor characteristics (6).

Antimonides (GaSb and InGaSb) will be thoroughly studied with a goal to develop high hole mobility III-V pMOSFETs. Additionally, high electron mobility InAsSb quantum well based devices will be studied in an effort to develop nMOSFETs (7).

(ii) Investigation of scattering mechanisms leading to degradation of carrier mobility
Deviations in carrier mobility in an inversion channel can arise due to several factors. The effective mobility in the channel is lower than the bulk carrier mobility due to various sources of scattering. Some of the sources are oxide-semiconductor interface roughness, remote Coulomb scattering due to the proximity of the inversion channel to the high-k gate dielectric, heterostructure interfacial roughness and scattering due to optical phonons.

Employing a buried channel architecture would result in improved mobility but the top barrier layer (III-V semiconductor dielectric constant is ~ 12) contributes to the equivalent oxide thickness and a low EOT is required for having a good electrostatic control especially in deeply scaled devices. Hence, the thickness of the top barrier layer needs to be carefully optimized such that a low EOT is maintained and simultaneously retain the advantage of obtaining a high mobility.

The effect of remote Coulomb scattering due to the soft metal-oxygen bonds on the inversion carrier mobility can be mitigated by employing a thin layer of a low-k dielectric between the semiconductor and the high-k gate dielectric. One disadvantage of using a low-k interlayer is the increased EOT, thus optimization of the thickness of the interlayer is required. Employing a thin layer of Al$_2$O$_3$ (dielectric constant $k = 9$) under a high-k gate dielectric such as ZrO$_2$ (dielectric constant $k = 29$) is a typical example to realize low EOT and simultaneously decrease the effect of remote Coulomb scattering. Maintaining a low EOT and simultaneously making sure that the carrier mobility is not
degraded due to Coulomb scattering calls for thorough investigation to identify the suitable gate dielectric stack.

(iii) Sub-micron gate length and non-planar III-V MOSFETs

In long channel devices, the magnitude of electric field in X direction (along the channel) is much larger than the field in the Y direction. In sub-micron gate length (deeply scaled) devices, the gradual channel approximation does not hold good anymore and the electric field in X-direction is comparable to the field in Y direction. This results in severe short channel effects such as threshold voltage roll-off (Vt roll-off), drain induced barrier lowering (DIBL), degradation in subthreshold slope etc. It is of paramount importance to determine the short channel effects in deeply scaled III-V MOSFETs before III-V MOS can become a mainstream technology.

Non-planar device architectures such as gate-all-around FETs and FINFETs are being considered for future technology nodes due of superior electrostatics. Recently, InGaAs based FINFET with promising transistor characteristics were successfully demonstrated (8). Realization of III-V FINFETs needs defect free dry etching of the vertical walls of the semiconductor in addition to sidewall passivation. The short channel effects of vertical device architectures with Arsenide and Antimonide channels will be studied.
References:


