A study of reticle non-flatness induced image placement error in extreme ultraviolet lithography

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A Study of Reticle Non-Flatness Induced Image Placement Error in Extreme Ultraviolet Lithography

by

Sudharshanan Raghunathan

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Dedication

To my loving Parents
Acknowledgements

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Abstract

As the semiconductor industry continues scaling devices to smaller sizes, the need for next generation lithography technology for fabricating these small structures has always been at the forefront. Over the past few years, conventional optical lithography technology which has adopted a series of resolution enhancement techniques to support the scaling needs is expected to run out of steam in the near future. Extreme Ultra Violet lithography (EUVL) is being actively pursued by the semiconductor industry as one of the most promising next generation lithographic technologies. Most of the issues unique to EUVL arise from the use of 13.5 nm light for imaging. Since most material systems are absorbing at that wavelength, the entire optical train in a EUVL tool is reflective. Due to the use of reflective optics, reticle illumination is non-telecentric leading to change in feature size from shadowing, image placement errors from reticle non-flatness, etc. All of these challenges and problems need to be overcome for the technology to come into use in production. In this work, Image Placement Errors (IPE) arising from reticle non-flatness has been studied.

In order to overcome reticle non-flatness induced image placement errors, flatness compensation has been proposed to relax requirements for substrate flatness. With flatness compensation, theoretically, substrates with any shape can be used as long as the resulting image placement errors from the substrate shape is understood. Preliminary overlay results from flatness compensation experiments using the EUV Alpha Demo Tool (ADT) has shown ~35% improvement in overlay error using different flatness compensation algorithms. To better understand the different components of image placement error and to characterize the reticle clamping on the EUV ADT, a set of reticles were fabricated from substrates with different flatness specifications to be imaged on the ASML EUV Alpha Demo Tool. Each reticle was designed with a set of image placement fiducials, which can be imaged on to a wafer and measured to calculate the IPE. Some of these reticles were made 90° rotatable, such that the reticle and tool contribution to IPE can be
separated. Finally, a overlay study with a set of 20 blanks with different shapes was performed to understand the feasibility of reticle shape matching as a method for overlay reduction in EUVL.
List of Abbreviations

ADT: Alpha Demo Tool
AOI: Angle of Incidence
ArF: Argon Fluoride
ASIC: Application Specific Integrated Circuits
ASML: ASM Lithography
CD: Critical Dimension
CMOS: Complementary Metal Oxide Semiconductor
CMP: Chemical Mechanical Planarization
CRAI: Chief Ray Angle of Incidence
CTE: Coefficient of Thermal Expansion
CZ: Czochralski
DOF: Depth of Focus
DRAM: Dynamic Random Access Memory
EBDW: Electron Beam Direct Write
EUVL: Extreme Ultra Violet Lithography
FEM: Finite Element Model
HSFR: High Spatial Frequency Roughness
HVM: High Volume Manufacturing
IC: Integrated Circuit
IEUVI: International Extreme Ultra Violet Initiative
IPD: In-Plane Distortion
IPE: Image Placement Error
ITRS: International Technology Roadmap for Semiconductors
KrF: Krypton Fluoride
λ: Wavelength
LAS: Lithium Aluminum Silicate
LSFR: Low Spatial Frequency Roughness
LTEM: Low Thermal Expansion Material
M1: Metal 1
ML: Multi-Layers
MOS: Metal Oxide Semiconductor
MRF: Magneto Rheological Finishing
MSFR: Mid Spatial Frequency Roughness
MTF: Modulation Transfer Function
NA: Numerical Aperture
NCE: Non-Correctable Errors
OPD: Out-of-Plane Distortion
PMMA: Poly Methyl Methacrylate
P-V: Peak to Valley
RIE: Reactive Ion Etching
RSS: Resultant Sum of Squares
STI: Shallow Trench Isolation
TIS: Transmission Image Sensor
TV: Thickness Variation
ULE: Ultra Low thermal Expansion
XPA: Extended Pattern Area
## Contents

1 Overview of Semiconductor Lithography .......................... 1
   1.1 Introduction ................................................. 1
   1.2 Transistor Fabrication - Process Flow ........................ 3
   1.3 Technology Scaling ......................................... 7
   1.4 Lithography for Semiconductor Devices ........................ 9
   1.5 Exploring the Limits of Optical Lithography ................. 14
   1.6 Next Generation Lithography Technologies .................... 17
       1.6.1 Electron Beam Direct Write ............................. 18
       1.6.2 Imprint Lithography .................................... 19
       1.6.3 Extreme Ultra Violet Lithography ....................... 19

2 Extreme Ultraviolet Lithography ............................... 21
   2.1 Introduction ................................................. 21
   2.2 Wavelength for EUVL ........................................ 23
   2.3 Multi-layer reflectors for EUVL ................................ 25
   2.4 EUVL - Top Challenges .................................... 26
   2.5 Overview of Research ........................................ 28

3 Image Placement Error in EUV Lithography ...................... 30
   3.1 Introduction to Overlay Errors ............................... 30
   3.2 EUV Substrates ............................................. 32
   3.3 Blank Fabrication Process .................................... 34
   3.4 Non-flatness of EUV Blanks .................................. 36
3.5 Electrostatic Chucks ........................................... 37
3.5.1 Electrostatic Chucking of EUV Masks .................. 40
3.6 Modeling for Image Placement Error Calculations ....... 43
3.6.1 Surface Flatness Measurements .......................... 43
   3.6.1.1 Flatness Measurement Procedure .................. 46
   3.6.1.2 Flatness Measurement - An Example ............... 49
3.6.2 Reticle Flattening IPE ................................... 52
   3.6.2.1 Legendre Polynomial Description of Reticle Sur-
   face ................................................. 55
   3.6.2.2 Analytical Model for Reticle Flattening .......... 57
   3.6.2.3 IPE \text{IPD} Example - Analytical Method ....... 58
3.6.3 IPE from Out of Plane Distortion ....................... 60
   3.6.3.1 Non-telecentric Illumination of EUV Reticles ... 62
3.7 Tool Contribution to Image Placement Errors ............ 64
3.8 Scanner Correctable Errors ................................. 68
3.9 Summary ..................................................... 70

4 Compensating for Reticle Non-Flatness Effects ............ 71
4.1 Introduction - Flatness Compensation ..................... 71
4.2 Experimental Setup ......................................... 73
   4.2.1 Blanks for Flatness Compensation ................... 74
   4.2.2 Mask Pattern Layout ................................ 74
   4.2.3 Predicted Errors for Non-flat1 - IPE Modeling ...... 78
4.3 Experiments - Set 1 ......................................... 80
4.4 Experiments - Set 2 ......................................... 82
4.5 Discussion of Results ....................................... 84

5 Experimental Determination of Image Placement Errors .... 86
5.1 Introduction .................................................. 86
5.2 Experiment Setup ............................................ 88
5.2.1 Experiments - Clamping Repeatability .......................... 88
5.2.2 Experiment - Clamping Pressure Study .......................... 91
  5.2.2.1 Clamping Pressure Study - Finite Element Modeling 92
  5.2.2.2 Reticle A - Overlay results between clamping pressures 93
  5.2.2.3 FE Modeling of Non-flat Chucks ......................... 96
  5.2.2.4 Clamping pressure study of reticles from different suppliers ........................................ 99
5.3 Conclusions and Future Directions ................................. 100

6 Rotatable Transmission Image Sensor Reticle ........................ 102
  6.1 Introduction ......................................................... 102
  6.2 Transmission Image Sensor as IP Fiducial ....................... 103
  6.3 TIS Rotatable Reticle - Pattern Layout ......................... 104
  6.4 Blank Flatness Measurement .................................... 106
    6.4.1 Predicted IPE from Flatness Measurements ............... 107
  6.5 Experiment Setup ............................................... 110
  6.6 Separating IPE_{IPD} and IPE_{OPD} ............................ 116
    6.6.1 TIS Measurement - Measurement Sequence ............... 116
  6.7 Summary and analysis of Results ............................... 122

7 Reticle Shape Matching to Reduce Overlay Errors .................... 126
  7.1 Introduction ......................................................... 126
  7.2 Population Studies .............................................. 127
  7.3 Population Analysis - IPE Calculation ........................ 128
  7.4 IPE and Overlay Budget ....................................... 131
  7.5 Overlay Error Analysis ....................................... 132
  7.6 Note on Flatness Compensation ................................ 136
  7.7 Summary and Conclusions ....................................... 137
**8 Summary and Conclusions**

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1 Flatness Compensation</td>
<td>140</td>
</tr>
<tr>
<td>8.2 EUV ADT Reticle Clamp Characterization</td>
<td>141</td>
</tr>
<tr>
<td>8.3 Separating IPD and OPD Contributions</td>
<td>143</td>
</tr>
<tr>
<td>8.4 Reticle Shape Matching</td>
<td>144</td>
</tr>
</tbody>
</table>

**A Determining Correctable Error - 10 Parameter Model** | 145 |

**B Flatness Data - Overlay Study** | 150 |
List of Figures

1.1 Gordon Moore’s observation explaining the increase in minimum number of components per integrated circuit required to achieve minimum cost per component ........................................... 2
1.2 Plot showing the industrial trend from 1959 to 1965 and extrapolation to 1975 of the number of transistors (individual components) on an integrated circuit ........................................... 2
1.3 CMOS Fabrication process flow -1 ........................................... 5
1.4 CMOS Fabrication process flow -2 ........................................... 6
1.5 CMOS Fabrication process flow -3 ........................................... 6
1.6 Plot of transistor count for various INTEL processors against dates of introduction. One of the key enabling technologies for this exponential increase in processor density are the advances in lithography systems and in particular system resolution and overlay capabilities. 9
1.7 Plot of various wavelength used in semiconductor lithography. It can be seen that the wavelength has been decreasing to keep up with the demands for smaller feature sizes. .............................. 13
1.8 Schematic showing the numerical aperture of a lithography system. It is defined as the product of refractive index of the medium and the angle subtended by the projection lens at the wafer. ............. 15
1.9 Reduction in $k_1$ plotted with time showing ever increasing processing difficulty as the device dimensions continue to get smaller. ... 16
2.1 Reflection and refraction at the boundary of a media with refractive indices \( n_1 \) and \( n_2 \).......

2.2 Illustration of a multi-layer reflector using Mo/Si multi-layers for use in EUV optics at 13.5 nm wavelength. Multi-layer period is approximately \( \lambda/2 \approx 7 \) nm. Mo and Si layers are sometimes separated by a thin film of B\(_4\)C to prevent inter-diffusion. ...............

3.1 Illustration of image placement error resulting from reticle plane non-flatness in EUVL .............

3.2 Different scattering processes from a reflecting optical surface. Low spatial frequency non-flatness (figure) and mid spatial frequency roughness (low angle scatter) result in IPE while HSFR leads to loss of light and decrease in throughput. ...............

3.3 Process flow describing the fabrication of a EUV blank from a Low CTE substrate. .........

3.4 Deformation of a ULE substrate due to ML, buffer, absorber and resist deposition. The final deformed shape is calculated using a FE modeling. .............

3.5 Schematic diagram of the two types of electrostatic chucks. .......

3.6 Blank with 1310 nm P-V front side non-flatness clamped with 15 kPa on a flat chuck. The as-chucked P-V front side non-flatness reduces to 86 nm. ..........

3.7 Plots showing FEM of a EUV mask being clamped on a flat electrostatic chuck with 15 kPa clamping pressure. As-chucked mask surface is a good approximation to the thickness variation of the EUV blank. ..........

3.8 A schematic showing a the cross section of a bi-polar pin chuck. The pin chuck is designed to reduce the effect of particle contamination from the reticle backside and chuck top surface from influencing imaging properties. .............
3.9 Schematic of a Fizeau interferometer used to measure the surface flatness of EUV reticles ........................................ 44
3.10 Top-down view of the interferometer setup used to measure mask flatness ................................................. 46
3.11 Side view of the vacuum apparatus sitting on the vibration isolation table, arrows indicate the direction of the laser path coming from the interferometer and entering the chamber through the optical window after being deflected by the folding mirror. The laser takes the same path back to the interferometer after reflecting from the mask surface .................................................. 47
3.12 Incorrect and correct alignment of the various optical surface on the Zygo interferometer setup .......................... 48
3.13 Flatness measurement of a substrate polished to \( \leq 100 \) nm flatness specifications measured on the vertical test stand at the Sematech MBDC in Albany. The flatness shown is over a \( 140 \times 140 \) \( \text{mm}^2 \) area. .......................... 50
3.14 Flatness measurement of a substrate with optical grade flatness specification on the vertical test stand at the Sematech MBDC in Albany. The flatness shown is over a \( 140 \times 140 \) \( \text{mm}^2 \) area. ....................... 51
3.15 Flatness measurement of a EUV blank after multi-layer and other thin film deposition fabricated from a substrate ith optical grade flatness specification. The flatness shown is over a \( 140 \times 140 \) mm\(^2\) area. ............................................................. 51
3.16 A EUV substrate post thin film deposition is patterned on a ebeam tool on a 3-point mount and then chucked flat using an electrostatic chuck on the EUV tool. The difference between the two clamping methods between the ebeam and EUV tool is the cause of IPE from reticle flattening. ......................................................... 53
3.17 The first 5 Legendre polynomials are plotted over the interval \([-1,1]\). .......................... 56
3.18 Plots comparing $8 \times 8$ polynomial fit and the actual measured surface of a reticle. Maximum difference between the raw and fit data is 40 nm P-V ......................................................... 57
3.19 Illustration of local slope calculation from a bowed reticle. Surface slopes are calculated from flatness measurements in an interferometer. 58
3.20 Illustration of reticle flattening from electrostatic chucking. (a) Reticle back side flatness measured from the interferometer and fit to a $8 \times 8$ Legendre polynomial. (b) Surface distortion vector plot as a result of flattening during reticle chucking. 59
3.21 Illustration of image placement error resulting from reticle plane non-flatness in EUVL .............................................. 61
3.22 Calculating IPE from reticle non-flatness .......................... 62
3.23 Reticle Illumination setup on the ASML EUV ADT .............. 62
3.24 Chief ray angle of incidence across slit on the ASML EUV ADT. ... 63
3.25 Components of image placement error across the ring field varies as a function of $\theta$. ......................................................... 64
3.26 An example of $\text{IPE}_{\text{OPD}}$ calculation for a reticle with large thickness variation. The OPD contribution is quite large with a maximum vector error of 26 nm. ......................................................... 64
3.27 Strawman budget for image placement error contribution from the EUV tool and lithography process to achieve the ITRS specification of 7.1 nm overlay error for year 2012. ........................ 67
3.28 Illustration of inter-field errors when printing multiple fields on a wafer. The inter-field errors arise due to imperfect wafer stage motion and misalignment in the reticle and wafer stage during exposure ......................................................... 69
3.29 An example of calculating residual error by removing the magnification, rotation and translation coefficients. .................. 70
4.1 Increasing defect count as the substrate flatness specifications get
tighter. ............................................................. 72
4.2 Proposed method for flatness compensation for EUV reticles. ... 73
4.3 Set of substrates used for studying flatness compensation methods.
Flat and non-flat substrates with different substrate shapes were
used to perform overlay tests on the EUV ADT. ................ 75
4.4 Blank fabricated from the first set of substrates used for studying
flatness compensation methods. ............................... 75
4.5 Blank fabricated from the second set of substrates used for studying
flatness compensation methods. As with the first substrate set, the
flat and non-flat substrates were selected with the state of the art
flatness and optical grade flatness specifications respectively. ... 76
4.6 Layout of the flat and non-flat reticles for flatness compensation
testing. The flat substrates were fabricated with all layers uncom-
pensated while 3 different compensation schemes were built in to
the non-flat substrates. ........................................ 77
4.7 University of Wisconsin analytical model calculation for IPE from
the Non-flat1 blank. ............................................. 79
4.8 Figure showing the use of a 8×8 legendre polynomial fit for reticle
flatness is adequate to capture to the required flatness information
needed for IPE calculations. ................................. 79
4.9 Figure shows that IPE calculation for the Non-flat1 blank based on
the 3 models used in the compensation experiments. ............ 80
4.10 Mask IPRO measurements of the three compensated IP fiducials
with the max x and y vectors. The magnitude of and signature of
the IPE on the mask indicate that the mask was written with the
right compensation for each layer. ............................ 80
4.11 Overview of the die layout used for exposures of the compensated and the uncompensated reticles. A 640 µm separation between the two exposures is used to optimize the accuracy of the overlay measurements. All overlay results are average values from these 44 dies. ......................................................... 81

4.12 Residual error from an overlay measurement of Non-flat reticle exposure to Flat reticle exposure. Details on the magnitudes of the errors are shown in figure 4.13. ......................................................... 82

4.13 Magnitude of the x and y 3σ errors for each layer based on the overlay residuals from exposing the Set 1 reticles. The best overlay results were observed on the layer with UW analytical model based compensation. The net improvement was 39% over the uncompensated layer. ......................................................... 82

4.14 Blank fabricated from the second set of substrates used for studying flatness compensation methods. ......................................................... 83

4.15 Overlay errors from printing the second set of reticles with different flatness specifications. The flatness compensation schemes do not improve overlay errors. ......................................................... 84

5.1 Illustration of IPE from IPD and OPD due to electrostatic chucking of non-flat reticle on the EUV ADT. ......................................................... 88

5.2 Thickness variation and layout of the flat rotatable reticle used for the clamp repeatability study. ......................................................... 89

5.3 Predicted errors for all 4 orientations based on an analytical model for the flat rotatable reticle. ......................................................... 90

5.4 Measured errors for all 4 orientations of the flat rotatable reticle on the EUV ADT. ......................................................... 90

5.5 Measured errors at 0 degree using the flat rotatable reticle post chuck clean. Absence of particle signature at reticle center confirms that the chuck cleaning was effective. ......................................................... 91
5.6 Thickness variation and layout of reticle A used for the clamping pressure study.

5.7 $8 \times 8$ Legendre polynomial fit to the front side and back side flatness of reticle A showing large bow on both surfaces from multi-layer deposition. The blank thickness variation over the full area is 336 nm.

5.8 As-chucked reticle flatness of reticle A based on a flat rigid chuck at different clamping pressures.

5.9 Overlay error between exposures of the Non-Flat reticle at 15 kPa and 2 kPa (a) ADT measurement (b) FE Model (Flat Chuck).

5.10 Clamping pressure variation induced change in as-chucked reticle height, measured on the EUV ADT.

5.11 Average flatness at 2 kPa, 1 kPa and 300Pa for reticle A from the FE model.

5.12 Reticle flatness predicted by a FEM at different clamping pressure for a perfectly concave and perfectly convex shaped chucks with 80 nm P-V non-flatness at the chuck center.

5.13 Summary of the reticle flatness data for reticle A from ADT measurements and FE modeling for flat, 80 nm concave and 80 nm convex chucks.

5.14 Summary of the reticle flatness measurements for different reticles from multiple vendors. Reticles were selected such that the flatness specifications were different. Some of the differences in the flattening behavior can be attributed to the differences in the thin film stack on these reticles.
6.1 Figure shows the pattern layout of the TIS rotatable reticle with a rotatable frame. The TIS fiducials are placed in 4 different orientations to enable reticle imaging in different orientations on the ADT. The reticle also has an array of XPA marks to enable print based IPE measurement.

6.2 Figure shows the back side flatness and the thickness variation of the substrate used for fabricating the TIS Rotatable reticle. The substrate was polished to optical grade flatness specification (~250 nm).

6.3 Figure shows the back side flatness and the thickness variation of the blank used for fabricating the TIS Rotatable reticle. The contour plots show the P-V flaness along with bow (power) and rms flatness. The flatness shown is for the substrate area of 140 x 140 mm^2.

6.4 Figure shows the predicted image placement error based on flatness measurements for the TIS Rotatable reticle. The IPE calculation were done using a simple analytical model.

6.5 Figure shows the pattern placement error from the mask writer. The effect of mask writer error on the total IPE is negligible.

6.6 Figure shows predicted IPE for different orientation of the TIS Rotatable reticle based on flatness measurements and conformal clamping.

6.7 Figure shows accuracy of the TIS measurements in x and y directions. The cumulative probability plots show that the y-direction accuracy is better than x-direction accuracy.

6.8 Figure shows vertical scan direction dependence of IPE_x and IPE_y errors.

6.9 Figure shows horizontal scan direction dependence of IPE_x and IPE_y errors.
6.10 Figure shows the $3\sigma$ z values for an array of $13 \times 9$ array of TIS fiducials based on 10 repeats of each fiducial.

6.11 Comparison of image placement error measurements from XPA and TIS marks methods. The max vectors in the XPA measurements are larger as expected due to an additional readout step using the ADT wafer stage. The shaded portions in the TIS measurements are the additional rows of TIS marks and are not present in the XPA results.

6.12 TIS measurement sequence for measuring aerial image based IPE.

6.13 Focal offset based from TIS measurement shows large differences between scan sequences. Each TIS mark is measured 10 times before moving to the next mark.

6.14 Focal offset between scan sequences show very small differences indicating better control of external factors (like temperature) affecting the measurement results. Each TIS mark in only measured once and the entire array is measured 5 times.

6.15 IPE measurements from the TIS reticle following the scan sequence described in figure 6.12.

6.16 ASML tool NCE or distortion measurement. The error magnitudes and signatures are very similar to the TIS measurements in figure 6.15.

6.17 Large $\Delta z$ values measured for all orientations of the TIS Rotatable reticle. The plots from left to right are for 0, 90, 180 and 270 degree orientations.

6.18 Average $\Delta z$ values and lens setup errors from the same time frame as the TIS measurements.

6.19 Corrected $\Delta z$ values after removing average $\Delta z$ from each row of measurements. The plots from left to right are for 0, 90, 180 and 270 degree orientations.
6.20 Non correctable error from $\Delta z_c$ calculations. As seen from the $\Delta z_c$ values, the errors are quite small compared to predicted OPD contribution. The plots from left to right are for 0, 90, 180 and 270 degree orientations.

6.21 The IPE from in-plane distortion calculated as the difference between IPE$_{\text{TOTAL}}$ from the measured $\Delta x$, $\Delta y$ values and OPD contribution from corrected $\Delta z_c$ values.

6.22 Short term and long term repeatability of reticle clamping based on multiple TIS Rotatable reticle measurements.

6.23 Summary of IPE results for the TIS Rotatable reticle. The plot shows measured and predicted IPD and OPD contributions to wafer IPE.

7.1 Increasing defect count as the substrate flatness specifications get tighter.

7.2 Plot of the front side flatness and thickness variation of EUV blanks from two vendors.

7.3 Summary of bow contribution to total flatness for blanks from different vendors. All flatness numbers in nm.

7.4 Maximum residual error for all 20 blanks.

7.5 Overview of a strawman overlay budget for EUV scanners to enable 3.8 nm IP accuracy specified by the ITRS for sub 32 nm device patterning (2012 time frame).

7.6 Flowchart illustrating the overlay calculation work flow.

7.7 Summary of overlay calculations for pairs of blanks. Only same vendor overlay numbers are calculated.

7.8 Procedure for simulating shapes of blanks from 50 nm flatness substrates based on existing 100 nm flatness substrates.
7.9 Comparison of overlay error between pairs of 50 nm substrates and 100 nm substrates from vendor A and B. With the specification relaxed to 2.12 nm from 1.4 nm i.e. with tool dedication, more of the 100 nm substrates and almost all 50 nm substrates from Vendor A are within overlay specification.

B.1 Summary of bow contribution to total flatness for blanks from different vendors. All flatness numbers in nm.

B.2 Backside flatness measurements of the 5 flat blanks from Vendor A.

B.3 Backside flatness measurements of the 5 non-flat blanks from Vendor A.

B.4 Thickness variation of the 5 flat blanks from Vendor A.

B.5 Thickness variation of the 5 non-flat blanks from Vendor A.

B.6 Backside flatness measurements of the 5 flat blanks from Vendor B.

B.7 Backside flatness measurements of the 5 non-flat blanks from Vendor B.

B.8 Thickness variation of the 5 flat blanks from Vendor B.

B.9 Thickness variation of the 5 non-flat blanks from Vendor B.
List of Tables

1.1 Sample scaling properties of CMOS devices for both constant voltage scaling and constant field scaling. Lithographers have to deal with the dimensional scaling parameters. The most critical dimensions include gate length, source drain separation and metal line half-pitches. .................................................. 8

2.1 List of the most critical issues ranked by IEUVI working group that needs to be addressed in order to introduce EUVL into HVM. Notice that over the years, the number of critical issues has decreased. . . 27

3.1 Flatness requirements for EUV Substrates ......................... 34
3.2 Individual Stress contributions from the different layers deposited on the substrate prior to mask patterning. ......................... 37

4.1 Flatness requirements for EUV Substrates (with and without flatness compensation) .......................................................... 72

7.1 Flatness requirements for EUV Substrates (with and without flatness compensation) .......................................................... 128
Chapter 1

Overview of Semiconductor Lithography

1.1 Introduction

The semiconductor industry has seen tremendous growth over the past 4 decades. This growth typically manifests itself as the total processing power of an integrated circuit. Increase in processing power can be achieved either by increasing the number of processing components in each circuit or by enhancing the processing ability of each component of the circuit. Looking back at the industrial trend, it has been observed that a combination of both has been used to improve processing power of an integrated circuit. This was observed by Gordon Moore who stated that the integrated circuit complexity for achieving minimum component cost has increased at a rate of roughly a factor of 2 every year [1]. This is illustrated in figure 1.1. A simpler and more popular form of Gordon Moore’s observation is that the number of transistors on a chip doubles every 18 months and has come to be known simply as Moore’s law (figure 1.2).

One of the primary enablers for advancing the performance of chips are the significant advances in lithography technology. The most common device type found in logic chips today is a Metal Oxide Semiconductor (MOS) and the type of logic is
Figure 1.1: Gordon Moore’s observation explaining the increase in minimum number of components per integrated circuit required to achieve minimum cost per component.

Figure 1.2: Plot showing the industrial trend from 1959 to 1965 and extrapolation to 1975 of the number of transistors (individual components) on an integrated circuit called Complementary MOS or CMOS (used in most PC processors). While component density on a chip is dependent on the total size of an individual device, the device performance of a MOS structure is strongly dependent on the length of the channel under the gate. Hence the ability to pattern these small transistor struc-
tures (lines and spaces for channels and squares or circle for source/drain contacts to carry the current out of the device) is the most significant factor driving device performance. In the next section, the process flow for fabricating a transistor will be detailed indicating the critical layers from a lithographic perspective.

1.2 Transistor Fabrication - Process Flow

A MOS transistor is the basic component of any logic circuit in use today. There are two types of MOS transistors: p-type and n-type, depending on the type of channel used in the device. In order to completely fabricate a MOS transistor, a sequence of processing steps needs to be completed. The details of silicon processing for CMOS device fabrication and integrated circuit manufacture are detailed elsewhere [2]. The following is a list of processing steps involved in manufacture of p-type and n-type transistor on a single piece of silicon wafer. The starting point for chip manufacturing typically is with a mildly doped p-type substrate in order to reduce substrate resistivity. The p-type substrate is a silicon substrate doped with a group - III element in order to create an excess of holes in the valance band of the semiconductor (Si). Boron is the preferred dopant for Si substrates due to the particulars of the wafer manufacturing process (Czochralski or CZ method). Once the wafer for device fabrication is ready, the list of steps to build a working device are as follows:

1. Depositing a layer of oxide/nitride to use as hard mask for defining shallow trench isolation (for separating p-type devices from n-type devices)

2. Coat resist, and lithographically define the areas where shallow trench isolation (STI) structures need to be deposited and develop exposed resist.

3. Reactive Ion Etch(RIE) of the nitride with undeveloped resist as mask and follow up with RIE of Si substrate with oxide/nitride as hard mask to define the trenches for STI deposition.
4. Deposit oxide in the trenches to create STI structure and then CMP planarize with nitride hard mask as polish stop. Remove residual oxide/nitride. The steps required to define the STI structures is generally called the Damascene process.

5. Define p-wells and n-wells for subsequent n-type and p-type device builds respectively

6. Deposit a blanket layer of gate oxide over the entire wafer with the required thickness and dielectric constant. On top of the required oxide, grow a layer of polysilicon and dope it with impurities (type and concentration chosen depending on the gate stack) to reduce gate resistivity.

7. Lithographically define gate areas by patterning resist on top of the gate.

8. Use resist as mask to remove polysilicon and oxide under unexposed resist. Strip exposed resist after defining the gate.

9. The source and drain are defined by ion-implanting impurities (either boron for p-type or phosphorous for n-type) in the wells using the polysilicon gate as mask. When n-type and p-type devices are present on the same chip, an additional lithographic step is required to protect the p-type when defining n-type source/drain regions and vice versa. Once the implantation is complete, the substrate is annealed at an elevated temperature to electrically activate the dopants. With the source drain implants, the MOS device structure is complete. Further processing steps are required to define contacts and wires to carry current into and out of the active devices.

10. Grow a spacer to isolate the channel region during deep source drain implants. Grow a layer of Nickel silicide on top of the source/drain and gate regions to reduce resistance.

11. The next step is to deposit the inter-layer dielectric (Low dielectric constant oxide such as porous Si) over the device structures.

13. Form contact by Damascene process.

14. Further processing to deposit the vias and interconnects to interface the active devices to the external world through appropriate packaging for use in computing products. These steps are generally referred to as Integration and involves patterning metal and via levels (typically 10's).

![CMOS Fabrication process flow](image)

**Figure 1.3: CMOS Fabrication process flow -1**

Of the various process steps illustrated in the previous section, lithographically the most challenging steps are defining the first contact level and the metal level (typically referred to as M1). Although the gate length of a device is typically the smallest structure in a MOS device, lithographic target sizes for gates are quite large (~1.5 to 2 times the final dimension). The final gate CD or critical
dimension is achieved during post processing after lithography by a process called trimming. Since there is only a single gate per device, the gates are not as dense as other structures such as the first interconnect layer (Metal 1). As a result, the lithographic requirements are often dictated by the requirements of the metal and contact levels on any particular chip design.
1.3 Technology Scaling

Although patterning the gate is not lithographically as challenging as other structures like contacts and first metal layer, gate length is the single most important factor affecting device speed and performance. The speed of a MOS transistor is often expressed in terms of propagation delay $t_d$ given by

$$t_d = \frac{C V_{DD}}{I_D} \quad (1.1)$$

where, $C$ is the total load capacitance experienced by the device, $V_{DD}$ is the operating voltage and $I_D$ is the drain current during device operation. Propagation delay $t_D$ can be reduced either by decreasing the device capacitance or increasing the device ON current $I_D$. The ON current $I_D$ is the current flowing from the drain to source when with the gate voltage turned on. It can be expressed as

$$I_D = \frac{W \mu_{eff} C_{oxide}}{L_g} (V_G - V_{th})^2 \quad (1.2)$$

where, $W$ is the width of the gate, $\mu_{eff}$ is the effective mobility of the channel under the gate between the source and the drain, $C_{oxide}$ is the capacitance of the oxide between the gate and the channel, $L_g$ is the gate length, $V_G$ is the operating gate voltage and $V_{th}$ is threshold gate voltage required to achieve channel inversion for current conduction.

As seen from equation 1.2, the speed of the device is inversely proportional to gate length $L_g$. Although the oxide capacitance and effective mobility are all important factors, gate length takes on additional importance when the size of the device is taken into consideration. Device size decreases as the gate length decreases and is critical to increasing transistor density on a chip. Transistor density is directly related to integrated circuit performance since having more transistors is equivalent to having additional computing resources to perform the same computation. As the gate length is decreased, there are specific scaling require-
ments for the rest of the components of a MOS transistor. Some of the scaling requirements [3] involve source to drain separation distance, channel mobility, gate oxide thickness which in turn determines the capacitance of the gate oxide and subsequently $V_{th}$ etc. In brief, these scaling laws are formulated to enable decreasing the transistor foot print by appropriately scaling various aspects of device to provide the required device performance gain. Some of the common scaling parameters are listed in table 1.1. This successful scaling of the MOS transistor has resulted in an exponential increase in transistor count on a chip over the past 40 years. As an example, the transistor count on a INTEL Dual Core Itanium 2 consumer PC processor is in excess of 1 billion transistors [4]. The state of the art graphics processor from ATI, the HD5800 has a transistor count of 2.15 billion. Figure 1.6 shows a plot of transistor count for INTEL processors vs dates of introduction on a semi-log plot illustrating doubling of transistor count approximately every two years.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Constant Field Model</th>
<th>Constant V Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Width</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$1/k$</td>
<td>$1$</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Current</td>
<td>$1/k$</td>
<td>$k$</td>
</tr>
<tr>
<td>Junction Depth</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
</tbody>
</table>

Table 1.1: Sample scaling properties of CMOS devices for both constant voltage scaling and constant field scaling. Lithographers have to deal with the dimensional scaling parameters. The most critical dimensions include gate length, source drain separation and metal line half-pitches.

Typically, the advancement in the processing capability of a MOS transistor and the chips that contain them is typically denoted by the technology node used to manufacture the transistors. The accepted definition of a technology node is the smallest half-pitch of contacted metal lines on any product. It has been observed that requirements for DRAM half-pitch has been the tightest of all products being manufactured at any given point in time and has been adopted as a standard for gauging the progress of the semiconductor industry over the years. The industry
One of the key enabling technologies for this exponential increase in processor density are the advances in lithography systems and in particular system resolution and overlay capabilities.

is currently moving towards 32 nm logic processors with 45 nm logic being the more commonly shipping consumer product.

1.4 Lithography for Semiconductor Devices

A complete integrated circuit consists of active devices with metal wires and contacts for supplying voltage, current and driving a load circuit. However these devices along with the multiple levels of interconnects or wires are patterned sequentially through multiple lithography steps. The complete IC is then packaged for use in consumer products. However, the challenge as detailed in the section
1.2 is to identify the lithographic requirements for each level of the IC and derive appropriate solutions based on patterning requirements. Over the years, as the device dimensions have been shrinking, technique for patterning them has also changed considerably.

The first integrated circuits were patterned using contact lithography. Contact lithography used photomasks or photo masters created from Rubylith, which is a laminate made of dark red and clear plastic papers. The patterns were defined on Rubylith by removing the dark red plastic with the help of a blade, typically on a drafting board. This pattern on Rubylith was then used to make a photographic plate using a copy camera used backwards. The reduction ration between the Rubylith pattern and the photographic plate was anything between 10:1 to 50:1. This photographic plate was developed and used as a master pattern in a photo repeater to obtain a contact print master. The print master is typically replicated into sub-masters and used to create patterns on wafers. The number of sub-masters needed depended on the process complexity and number of wafers to be printed. This process of contact printing however, provides a easy path for defects to transfer from the wafer to the mask and vice versa, thus affecting yields. To overcome the defectivity problem with contact printing, the industry started to move towards proximity printing, where the print master is never in direct contact with the wafer. However, as the gap between the print master and the wafer was increased, the light traveling through the master onto the resist coated wafer suffered from near field diffraction effects, resulting in a loss of resolution [5]. The resolution $R$ for a proximity printer is given by,

$$ R = k\sqrt{\lambda g} $$

where, $\lambda$ is the illumination wavelength, $g$ is the contact gap between the master and the resist on wafer and $k$ is a process dependent constant $\approx 1$. However, unlike projection lithography, the dependence of resolution on wavelength is not linear and hence demanded large reductions in wavelength to manufacture print masters.
with patterns <1µm in dimension.

As the need for masters with smaller patterns increased, contact printing for mask making became grossly inadequate and was replaced by automated laser writers to create photographic plates for use in photo camera to manufacture the what was called the primary pattern plate [6]. These camera lens systems required complex lens assemblies and accurate control of lens distortion, image uniformity etc. The primary pattern plate was used in a step and repeat system to create the final master for wafer printing. The final master contained a large number of repeats of the original pattern which was imaged onto a wafer either using 1:1 projection printers. The first 1:1 projection printers used purely refractive optics and were not usable in a production environment because of instabilities associated with long air paths and lens elements with high absorption and inhomogeniety. The first commercially successful 1:1 imaging system used for high volume manufacturing was produced in 1970 by Perkin Elmer, which used all reflective scanning system based on the Offner relay [7] and imaged using radiation from a mercury arc lamp emitting light between 400 and 440 nm in wavelength. The minimum achievable pattern dimension on the wafer was around 5.0µm depending on the process conditions. There were a variety of 1:1 wafer imaging systems being used and included [5],

1. Full wafer static imaging - The entire mask pattern was imaged onto the wafer in a single exposure shot.

2. Full wafer scanning - In this method, the reticle was illuminated with a annular field, which was scanned along the reticle to image different portions of the reticle. The annular field dimensions should cover the entire mask along either the length or the width since the mask and the wafer are scanned in one direction only.

3. Raster Scanning - This was developed by Bell labs. The wafer was imaged by scanning both the wafer and the mask in two dimensions. This used a
very small field lens thus making the lens cost effective. The design of the system enabled the mask and wafer to be on the same plane thus making overlay extremely simple.

4. Step and Repeat - The mask consists of a single die. The pattern is imaged on the wafer by moving the wafer in two dimensions while holding the mask static. The entire mask pattern is imaged in a single shot onto the wafer. The lens manufacture for step and repeat systems are more relaxed compared to a full wafer static imaging system or a wafer scanning system since the size of the lens needed is much smaller.

As the complexity of the circuits increased, the minimum size of the patterns on the masks started to decrease concurrently. The size of the circuit also increased to accommodate the additional complexity. Simultaneously, the size of the wafers started to grow in order to make the manufacturing process economical. The size of the optical mask had to be increased to keep up with the increase in wafer size, since the wafer printing was done with 1:1 imaging systems. As a result, optical mask fabrication tools could not sustain such large pattern areas used to make the final print master. As a result, electron beam lithography became the preferred process for mask making at the end of the 1970’s and into the 80’s.

The next generation of wafer imaging systems consisted primarily of reduction systems, where the patterns on the mask were printed on the wafer after undergoing a scaling by the projection optics. Through the 60’s, the print master was fabricated by imaging a reticle containing the reduced Rubylith pattern onto a mask using a photo repeater. The first reduction steppers were indeed modified photo-repeaters, wherein the stages were modified to directly image the reticle onto the wafer. This required an additional alignment step to position the wafer accurately under the reticle, but removed the need to making a 1:1 imageable mask. The first reduction systems, were step and repeat and used the mercury g-line illumination for imaging the reticle. The key figure of merit for the lenses used in these reduction lithographic systems is resolution or minimum printable
feature on resist. The minimum printable feature size or feature CD is given by,

\[ R = \frac{k_1\lambda}{NA} \]  

where, \( NA \) is the numerical aperture which is a figure representing the size of the lens and \( k_1 \) is a process dependent term. The value of \( k_1 \) is a figure of how difficult the patterning process is. A lower \( k_1 \) process is more difficult and has a smaller margin of error than a higher \( k_1 \) process.

Figure 1.7: Plot of various wavelength used in semiconductor lithography. It can be seen that the wavelength has been decreasing to keep up with the demands for smaller feature sizes.

Over the years, as feature sizes of the devices in IC’s continued shrinking below 1\( \mu m \), there was a need to either use lenses of larger \( NA \) or to go to a smaller \( \lambda \) of light in order to pattern these features on resist. A significant milestone in the development of projection lithography systems is the development of Hg I-line based system in 1989. The trend continued for the next 2 decades, where the requirement of patterning smaller features on resist has either driven the lithography tool makers to shift to larger lenses with higher \( NA \) or move to an entirely new optical system using smaller wavelengths. Figure 1.7 shows the various wave-
lengths in lithographic tools [8] used for high volume manufacturing (HVM). The last progression in the reduction of wavelength for HVM tools is the introduction of ArF laser sources emitting 193 nm light. The first ArF systems started to be commercially available around 2001. These systems have undergone tremendous improvements since the first versions appeared for commercial use. Improvements in lens manufacturing has resulted in very large $NA \approx 1$ to keep up with the ever decreasing device sizes. Another significant jump in resolution has been made possible with the use of a thin layer of water between the final projection lens and the wafer, resulting in lens designs with higher numerical apertures. Numerical aperture of a lens is given by,

$$NA = n \sin \theta$$  \hspace{1cm} (1.5)

From figure 1.8, it can be seen that the theoretical numerical aperture of a dry lens, or, a lens with air as the refracting medium, can have a theoretical maximum numerical aperture of $\approx \sin 90^\circ = 1$. However, with a medium other than air, the theoretical maximum $NA$ can be increased by a factor equal to the refractive index of the medium. Thus, using a higher refractive index medium between the final lens and the wafer enables designing lens systems with higher $NA$ thereby improving the resolution of the system. Water has been the most commonly used medium in these high $NA$ systems. The refractive index of water is 1.44 which is an increase of 1.44x over air as medium. This theoretically entails an increase in $NA$ of 1.44x, and an improvement in resolution of 1.44x. Water immersion is currently used in production of 45 nm and below HP patterns at major semiconductor device manufacturers.

1.5 Exploring the Limits of Optical Lithography

However, even with such advances in conventional optical lithography, it seems unlikely that the current optical technologies can keep up with the requirements
for future CMOS devices. To understand the resolution limit, it is important to consider the parameter space that is available in lithography for improving resolution. Equation 1.4, shows that resolution $k_1$, $\lambda$, and $NA$. While the current lithography tools use 193 nm light, moving to a new wavelength would require developing lens systems and sources to operate at the required smaller wavelength. This is not a simple undertaking and usually takes years of research to accomplish this shift in wavelength and hence, not a practical approach to change wavelength for each technology node i.e. roughly 2 years. What remains then is the numerical aperture and process constant $k_1$. In the previous section, we have touched briefly on how immersion lithography enables designing lenses with higher $NA$, resulting in an improvement in resolution. With water immersion, the maximum theoretical numerical aperture is 1.44. There is a possibility of using liquids other than water, with higher refractive indices possibly enabling lens designs with higher $NA$.

The third factor in the resolution equation, $k_1$, is a process dependent factor
Figure 1.9: Reduction in $k_1$ plotted with time showing ever increasing processing difficulty as the device dimensions continue to get smaller.

and is often a measure of the processing difficulty. Figure 1.9 shows how the process factor $k_1$ has changed over the years. It is obvious that with a $k_1$ value of zero, one can achieve infinite resolution, solving all problems and need for newer lithography tools, albeit being infinitely more difficult to pattern the features with zero $k_1$. How low can you go with $k_1$? The answer to this question [8], can be found by looking at the MTF or Modulation Transfer Function [9] of a lens system. MTF is a measure of the resolving capabilities of an optical system. For lens systems with a circular aperture, the MTF is given by,

$$MTF(\nu) = \frac{2}{\pi} \left( \frac{\theta}{2} - \sin \frac{2\theta}{2} \right)$$  \hfill (1.6)

where, spatial frequency is,

$$\nu \leq \frac{2NA}{\lambda}$$  \hfill (1.7)

and

$$\theta = \cos^{-1} \left( \frac{\lambda\nu}{2NA} \right)$$  \hfill (1.8)
From equations 1.6, 1.7, 1.8, it can be seen that the lens does not resolve patterns with spatial frequency $\nu > \frac{2NA}{\lambda}$. Thus, the spatial frequency limit $\nu_m = \frac{2NA}{\lambda}$ for lens systems with circular apertures. The spatial frequency can be expressed as the inverse of feature pitch $p$ (minimum space after which a pattern repeats on a mask; for lines and spaces, pitch is the minimum distance between the same points on adjacent lines) or $1/p$. As a result,

$$\frac{1}{p} = \nu_m = \frac{2NA}{\lambda}$$  \hspace{1cm} (1.9)

Expressing $\frac{1}{p}$ in terms of resolution from equation 1.4 equating it to $\nu_m$,

$$\frac{NA}{2k_1\lambda} = \frac{2NA}{\lambda}$$  \hspace{1cm} (1.10)

which gives a minimum limit for $k_1$ below which MTF= 0 for the lens as 0.25. Thus the process factor $k_1 \geq 0.25$. This sets a minimum limit for pattern pitch that can be printed with the current 193 nm lithography tools with 1.3NA as $2 \times 0.25 \times 193/1.3 = 74$ nm. Hence devices at 32 nm technology node with an M1 half pitch of 32 nm cannot be printed with the current lithography tools in a single exposure. Alternately, there have been advances in pattern layout tools and resist processes that enable splitting a single array of lines and spaces as multiple nested arrays that can be printed at a relaxed pitch which are integer multiples of the original pattern pitch. Most of these patterning techniques are grouped under double patterning or double exposure lithography and have additional costs and throughput issues associated with the increase in processing steps.

\subsection{1.6 Next Generation Lithography Technologies}

With the current generation of lithography tools running out of steam to pattern devices with sub 22 nm HP, the industry has been actively researching a number of alternative lithographic technologies. Some of the more promising technologies
that were pursued over the years included x-ray lithography [11, 12, 13], electron beam direct write (both single and multi-beam systems), imprint lithography and extreme ultra violet lithography. While each of these so called next generation technologies have a set of issues or challenges that must be overcome, extreme ultraviolet lithography or EUVL seems to be the most promising candidate for sub 22 nm node HVM applications.

1.6.1 Electron Beam Direct Write

Over the years, electron beam lithography has been used extensively to create masks for optical lithography tools. An advantage of electron beam lithography is that the theoretical resolution limit which depends on the energy of the beam used is very small. As a result, electron beams have the ability to pattern very small structures, much smaller than what is possible with current optical lithography tools. Typical energy range used for electron beam patterning is between 50-100 KV. Although moving to a higher energy improves the resolution of the beam by reducing the forward scatter, electron beam resist sensitivity decreases with increasing beam energy. At higher beam energies, there is a large electron proximity effect requiring intensive post layout processing of the patterns to be written on the wafer to compensate for this effect. Since electron beam lithography is a sequential writing process, wherein the wafer being patterned is written one spot at a time, each wafer can take a few hours to complete. As a result, the system throughput (wafers/day) is very small. High throughput is one of the most important criterion for any technology to be used in High Volume Manufacturing. There are also additional problems with wafer and resist heating from electron beam irradiation which needs to be overcome for the technology to be used in HVM. However, a promising application of EBDW [14, 15] is in low volume ASIC designs that have a need for quick turn around time and for device prototyping. For example, EBDW can be used to test future technology node device performance when HVM patterning solutions to support the technology node is not yet
Multi-beam electron beam lithography [16, 17, 18, 19, 20, 21, 22] addresses the most important issue with electron beam direct write, i.e., throughput. By utilizing multiple beams of electrons, the throughput of a multi-beam electron beam tool can be increased from hours/wafer to wafers/hour depending on the number of beams being used. One of the most promising multi-beam systems is made by Mapper Lithography, which is designed to use more than 10,000 electron beams working in parallel to write patterns on the wafer.

1.6.2 Imprint Lithography

Imprint lithography is a non-projection lithography technology. The lithographic process consists of creating a hard mold of the pattern (similar to a mask in projection lithography) and contacting a liquid coated wafer with the mould to imprint the patterns on to the liquid. The liquid is then cured either using ultra-violet light or heat and pressure. Depending on the type of curing, the technology is called Step and Flash (for UV curing) or Nano (Heat and Pressure curing) Imprint Lithography [23, 24]. Patterning very small structures have already been demonstrated using imprint lithography. However, since imprint lithography is a kind of contact lithography, the problems associated with contact lithography such a defectivity is also present in imprint lithography. The defects can arise from either the template during fabrication and/or during the process of imprinting the template on the wafer. Reducing defect density is the most significant challenge that needs to be overcome for this technology to be used in a production environment.

1.6.3 Extreme Ultra Violet Lithography

Of all the next generation lithography technologies, EUVL seems to be the most promising. EUVL uses 13.5 nm light and reflective optical elements made of multi-layers. While there are unique challenges associated with using this small wavelength light, the technology is still considered a projection lithography tech-
nology. As a result, in many ways, use of EUV lithography is similar to the transitions that the industry has made from 365 nm light to 248 nm to 193 nm light, all of which required new optics, sources and resist systems to be developed. However, EUVL has some unique problems like non-telecentric illumination, mask defectivity due to lack of pellicles to protect the masks during exposure, contamination of the optics during EUV irradiation possibly requiring frequent cleaning etc. Over the past few years, a series of device demonstrations have been done using EUV lithography. The device demonstrations have typically integrated an EUV patterned layer, (contacts, metal, etc.) with an 193 nm optical lithography process. Reports of product yield, device performance and ease of patterning these critical layers using EUVL have shown the maturity of the technology [25, 26, 27]. The success of these device demonstrations has shown the feasibility of using EUV for HVM of future technology node devices. Some of the issues associated with using EUVL in a production environment along with a more detailed look at the technology itself is presented in chapter 2.
Chapter 2

Extreme Ultraviolet Lithography

2.1 Introduction

Extreme Ultra Violet Lithography as the name suggests uses wavelengths between 4 nm and 40 nm which is the soft x-ray or the extreme ultra violet region of the electro-magnetic spectrum [28]. However, within this range of wavelengths, most material systems absorb radiation and hence, making transmissive optical elements impractical. It was found that if wavelengths between 11-14 nm [8] were used, reflective optics could be constructed using multi-layer mirrors with reasonable reflectivity. Multi-layers reflectors are fabricated by using alternating layers of low atomic number (Z) and high atomic number elements in order to provide a difference in effective refractive index at each material interface. The power of reflected and transmitted radiation at any material interface can be calculated using Fresnel’s equation. According to Fresnel’s equation, the net reflectivity at a boundary is proportional to the difference in the refractive index between the media at the boundary. From figure 2.1, Snell’s law states that if the two media have refractive indices of $n_1$ and $n_2$ and the light incident at the boundary from medium 1 is at an angle of $\theta_1$ to the surface normal, the refracted beam has an
angle $\theta_2$ to the surface normal in medium 2 given by,

$$\theta_2 = \arcsin \left[ \frac{n_1 \sin \theta_1}{n_2} \right] \quad (2.1)$$

Figure 2.1: Reflection and refraction at the boundary of a media with refractive indices $n_1$ and $n_2$.

Fresnel’s equation states that for any given polarization of light, the reflection coefficient $R$ and transmission coefficient $T$ can be determined by,

$$R = \left[ \frac{f(\theta_2 - \theta_1)}{f(\theta_2 + \theta_1)} \right]^2 \quad (2.2)$$

where $f$ is \textbf{sine} for s-polarized light and \textbf{cosine} for p-polarized light. The transmission coefficient is given by $T = 1 - R$. As a result, at the boundary of a high and low atomic number material, there is a net reflectance that is proportional to the square of the difference between the refractive indices at EUV wavelengths. Since most materials have a refractive index close to 1 at EUV wavelengths, the reflectance at a single material boundary is quite small. However, with a sufficient number of ML pairs, a sufficiently high net reflectance can be achieved, provided the ML satisfies certain conditions. In order for the reflected light from each in-
terface to add up in phase i.e. constructively, the ML reflectors should satisfy Bragg’s condition, which can be written as,

\[ n\lambda = 2d\sin \theta \]  

(2.3)

where, \( n \) is an integer denoting the order of reflected radiation, \( \lambda \) is the wavelength of light, \( d \) is the multi-layer spacing in the case of EUV optics, \( \sin \theta \) is the incidence angle. In simpler terms, if the period of the multi-layer is \( 1/2 \) the wavelength of light used, reflected light from each interface, constructively interfere to provide a large net intensity that is usable for imaging work on resist. Figure 2.2 illustrates the concept of multi-layer reflectors satisfying the Bragg condition.

![Illustration of a multi-layer reflector using Mo/Si multilayers for use in EUV optics at 13.5 nm wavelength. Multi-layer period is approximately \( \lambda/2 \approx 7 \) nm. Mo and Si layers are sometimes separated by a thin film of B\(_4\)C to prevent inter-diffusion.](image)

**Figure 2.2: Illustration of a multi-layer reflector using Mo/Si multilayers for use in EUV optics at 13.5 nm wavelength. Multi-layer period is approximately \( \lambda/2 \approx 7 \) nm. Mo and Si layers are sometimes separated by a thin film of B\(_4\)C to prevent inter-diffusion.**

### 2.2 Wavelength for EUVL

Early research in EUVL was carried on at wavelength ranging from 4 nm to 80 nm [30]. It is well known that lower the wavelength, the lesser the reflectivity of the
multi-layer reflector systems. The bandwidth of the reflector which is the range of reflected wavelengths is also decreased. The higher limit is established based on resolution and depth of focus requirements of the EUVL tools. A detailed look at various factors affecting the choice of wavelength is given in [28]. To summarize, the wavelength chosen for imaging should satisfy the HVM tool requirements depending on when the technology is intended to be used. Additionally, it should also be able to sustain multiple nodes of device manufacturing. Initial experiments were carried out with specifications of resolution \( \leq 0.1 \mu m \), and depth of focus larger than 1 \( \mu m \). While resolution is given in equation 1.4, the depth of focus is given by

\[
DOF = \pm k_2 \frac{\lambda}{NA^2}
\]  

(2.4)

Hence a exposure tool with \( NA < 0.1 \) and wavelength between 3 nm and 40 nm would satisfy the \( DOF \) and resolution requirements simultaneously. However, reflectivity of multi-layer mirrors which determine the amount of light that gets transmitted from source to wafer depends on the wavelength. Lower the reflectivity of ML mirrors, the higher the source power that is required to operate the tool with acceptable throughput levels. Hence the wavelength range of 3 nm to 40 nm should be further down selected to the ranges that enable fabricating multi-layers with appropriate reflectivity to satisfy throughput requirements. The highest reflectivity occurs at wavelengths where the absorption of the low-Z material in the multi-layer is at a minimum. The best multi-layer systems within the wavelength range for good resolution and \( DOF \) are ones containing C, B, Si and Li for wavelengths longer than 4 nm, 6.7 nm, 12.5 nm, 23.9 nm respectively.

It is also important to operate at wavelengths where the absorption coefficient of the resist material is such that it has good sensitivity to provide the required throughput and also have have good absorption depth such that it is exposed uniformly with depth into the resist. All organic resist systems contain C as the primary material. The K-edge of Carbon is at 4.4 nm which would mean that an EUV tool operating at this wavelength would be able to use a sufficiently
thick resist. However, to operate at 4.4 nm, we need to have ML systems with Carbon. These C containing ML systems have very low reflectivity and a small reflectance bandwidth. It was shown by H.Kinoshita et.al [29] in 1989 that the absorption limit for PMMA at 11 nm was 0.08µm and at 5 nm wavelength, it was 0.3µm. It was shown [30] that the best wavelength window for optimum resolution, sensitivity and DOF is $\lambda > 11$ nm. Hence Si containing ML systems with good peak reflectivity of 65% were chosen to operate at 13.5 nm wavelength and is currently used in most EUV systems around the world.

Using equation 1.4, it can be shown that with a nominal $k_1$ of 0.5, $NA$ of 0.25, and $\lambda$ of 13.5 nm, resolution is

$$\frac{k_1 \lambda}{NA} = 27\text{nm}$$

(2.5)

It is obvious from the resolution equation that using 13.5 nm wavelength light for imaging work provides very good resolution. With a lower k value and higher NA lenses ($\geq 0.25$) that are planned for HVM tools, it is possible to use EUVL in production for multiple technology nodes if the technology is introduced into manufacturing near the 22 nm technology node.

### 2.3 Multi-layer reflectors for EUVL

Although the multi-layers in principle seem quite simple to fabricate and use in reflective optics, a significant number of challenges were overcome to fabricate reflectors with sufficient quality needed for imaging work. While designing lenses for grazing incidence light are theoretically possible and have been employed in the past, it has been demonstrated [31] that normal incidence reflective optics have lesser aberration (most significant), enable a larger field of view and are easier to manufacture. Some of the challenges that had to be overcome to produce imaging quality ML surfaces were protection from exfoliation due to humidity, roughening of surface due to oxidation of Mo, pinhole formation post ML deposition due to
stress relaxation. In addition, the requirements for producing diffraction limited images using these ML coated surfaces dictated that the errors in substrate shape (or figure) be less than 0.1 nm RMS. Since the figure of the optics is affected both by surface shape of the substrate and the stress induced change in shape post ML deposition, the irregularities in substrate shape and non-uniformity of the coating process are both important factors. It should also be noted that the mask in EUV systems, unlike conventional optical lithography systems is also a reflecting surface. Chapter 3 will discuss in good detail the different issues associated with mask substrates, flatness requirements and multi-layer stack on the substrates. EUV masks are typically patterned using electron beam lithography to define areas that have to be exposed to EUV light i.e. the absorber pattern is removed and ML is exposed to EUV radiation. The current EUV Alpha demo tool (ADT) is a full field EUV tool, uses non-telecentric ring-field illumination of the reticle with a chief ray angle of incidence (or CRAI) of 6° across the field on the reticle. Due to this non-telecentric illumination, the absorber material casts a shadow on the exposed ML which affects the printed pattern size. Furthermore, this printed pattern size depends on the position across on the reticle, height of absorber stack, angle of illumination, feature orientation, feature size and density. These are more generally referred to as Horizontal-Vertical bias and mask shadowing effects. Most of these issues can be addressed during electron beam patterning of the EUV mask using appropriate pattern biasing and positioning.

2.4 EUVL - Top Challenges

Each year the top challenges facing the introduction of EUVL into HVM is put together by a EUV working group called the International EUV Initiative [32] or IEUVI, depending on the requirements of the target node for introduction. Table 2.1 lists the top issues from 2005 to 2009 ranked by the working group as the most important issues with EUVL as of the year of the ranking.
Top EUV Research Focus Areas from 2005 to 2009 - IEUVI

<table>
<thead>
<tr>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist resolution and LER</td>
<td>Source power and reliability</td>
<td>Source power and reliability</td>
<td>Long term source operation with 100 W at IF</td>
<td>Defect free masks</td>
</tr>
<tr>
<td>Collector lifetime</td>
<td>Resist resolution and LER</td>
<td>Resist resolution and LER</td>
<td>Defect free masks</td>
<td>Long term source operation with 200 W at IF</td>
</tr>
<tr>
<td>Defect free masks</td>
<td>Defect free masks</td>
<td>Defect free masks</td>
<td>Resist resolution and LER</td>
<td>EUVL manufacturing integration</td>
</tr>
<tr>
<td>Reticle protection during handling</td>
<td>Optics quality and lifetime</td>
<td>Optics quality and lifetime</td>
<td>Optics quality and lifetime</td>
<td></td>
</tr>
<tr>
<td>Optics quality and lifetime</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1: List of the most critical issues ranked by IEUVI working group that needs to be addressed in order to introduce EUVL into HVM. Notice that over the years, the number of critical issues has decreased.

After decades of research by several groups around the world, the list of the most critical issues has decreased from five to three over the last couple of years. For the year 2009, the third most important issue for EUVL technology is EUVL manufacturing integration, which is a sign of how far along the technology has progressed over the last few years. Manufacturing integration involves using EUVL for some of the critical device levels, which would require the technology to be compatible with existing process flows. A key parameter in integrating EUVL is pattern overlay. Overlay is the ability to place patterns accurately on top of previously existing patterns on the wafer. It is widely anticipated that the first use of EUV in HVM would be for the most critical levels on a chip like metal 1, contacts and via 1 levels. However, this means that the remaining levels are likely to be patterned using existing optical lithography tools.

EUV optics and wafer are placed in a vacuum environment. Since EUV masks are also ML coated surfaces, the compressive stress from the ML coating bends
the substrate resulting in a bowed substrate. Specially designed clamps called electrostatic chucks are used to clamp reticles in EUV tools. These clamps are polished flat and are designed to provide uniform clamping pressure to the backside of the EUV mask in order to flatten and hold the reticle rigidly on the clamp during exposure. Due to the nature of the reflective optics and electrostatic chucks, EUV tools suffer from image placement errors which affect the pattern overlay in EUV lithography.

2.5 Overview of Research

EUV tools are being readied for HVM for the 22 nm technology node and beyond. Current EUV tools (ASML EUV ADT) can print a full reticle with 0.25NA optics, employing non-telecentric illumination with a CRAI of 6°. Due to the use of reflective masks and non-telecentric illumination, any non-flatness at the reticle level gets translated to image placement error at the wafer level. ML films of Mo and Si have a compressive stress that results in bowing of the substrate that it is deposited on. These substrates are patterned in an electron beam writer that are then used to expose wafers in a EUV tool. During electron beam patterning, the ML deposited blank is held using a 3-point mount. The already stressed mask experiences additional forces due to gravity. Most e-beam writers can compensate for this gravity sag using a compensation table that is input to the pattern writer during mask write. Once the patterns are written, the mask is then used in a EUV tool where it is typically clamped down using an electrostatic chuck to remove any substrate bow. Conformal repeatable chucking of the EUV mask is critical to the quality of overlay that can be obtained. When the patterned mask is clamped down using an electrostatic chuck, the unclamped reticle surface is distorted due to clamping force from the chuck. The stress induced on the pattern side by chucking a non-flat mask on a relatively flat chuck results in in-plane distortion (or IPD), which directly leads to pattern displacement at the wafer during
exposure. Conformal chucking of the backside also transfers the low order non-flatness from the back side to the pattern side. As a result, the as-chucked top surface of the mask can be approximated as the thickness variation of the mask blank. This as-chucked non-flatness i.e. the thickness variation, results in image placement error at the wafer due to non-telecentric illumination. In the reminder of the thesis, flatness mentioned in the context of electrostatic chucking induced surface distortions arise from the ML stress induced bow. The errors from flattening of this bow is denoted by $\text{IPE}_{\text{IPD}}$ where IPD stands for in-plane distortion. Any reference to as-chucked non-flatness or residual $z$-height variation or residual non-flatness or flatness mentioned in the context of non-telecentric illumination results from blank thickness variation. This thickness variation combined with non-telecentric illumination results in $\text{IPE}_{\text{OPD}}$ where OPD stands for out-of-plane distortion. In this work, a comprehensive study of image placement error arising from the non-flatness of the mask substrate/blank will be presented. Modeling of image placement errors along with supporting experiments will be performed to characterize and minimize non-flatness induced image placement errors. A number of masks have been designed to study the different components of IPE. A method to compensate for this image placement error will also be presented with some preliminary experimental results.
Chapter 3

Image Placement Error in EUV Lithography

3.1 Introduction to Overlay Errors

Overlay is the process of accurately placing a set of patterns on top of a pre-existing patterns. Overlay is a quantity that is defined across the entire imaging field of a lithography tool. It is generally defined as the vector difference between a point $R_L(x,y,z)$ on any layer of a device and the corresponding point $R_{L-1}(x,y,z)$ on a pre-existing layer on the wafer.

$$\Delta R = R_L - R_{L-1} \quad (3.1)$$

From equation 3.1, it can be seen that overlay is the difference between corresponding points on 2 different levels on the wafer. An illustration of overlay between a contact and metal 1 levels on a chips is show in figure 3.1. The contact level is processed before metal 1. Hence the metal 1 layer needs to be overlaid on the contact layer. If the overlay between the layers is not satisfactory i.e. if the metal 1 cannot be patterned accurately on the corresponding contacts, it could lead to electrical opens and ultimately failed devices. As seen from figure 3.1, the difference between actual and nominal vectors largely depend on where the
difference is measured. In figure 3.1, the overlay error $\Delta R$ increases from the left contact to the right contact where the error is largest.

![Figure 3.1: Illustration of image placement error resulting from reticle plane non-flatness in EUVL](image)

Image placement error is critical to achieving good overlay of different layers of a device on an integrated circuit. Achieving good image placement error on a product wafer requires accurate wafer and reticle stage motion, knowing the reticle and wafer stage positions to nanometer precision and accurately aligning the reticle stage to the wafer stage. In order to align different layers of an integrated chip to each other, a set of alignment marks are printed on the wafer before patterning the device layer. These alignment marks called the zero level marks are etched into the wafer by exposing a zero level mask. Each layer of the device has to align to these zero level alignment marks using the same alignment system and preferably on the same tool. However, even though the same alignment method is used on the same tool, the stack of material between the lens and the zero level mask is quite different at different stages of device fabrication. It is very important that the alignment method in use is insensitive to differences in the stack of materials above the zero level marks. It has been shown that the use of zero level marks can reduce alignment variation compared to sequential alignment whereby each layer gets aligned to the marks put down by the layer prior to it. The improvement in overlay standard deviation [35] by the use of zero-level alignment marks is $\sim 1.22x$ compared to sequential alignment and hence the accepted standard in most modern integrated circuit fabrication processes.
The two basic components of overlay are aligning the wafer to the wafer stage and subsequently reticle to the wafer. Aligning the wafer to the stage is performed with either bright or dark field images of the zero level marks on the wafer. Traditionally, this is done with the help of a microscope whereby the alignment marks on the wafer are adjusted by moving the wafer in order to align to the fiducials in the microscope optics. This problem of establishing consistent alignment between the wafer and reticle during exposure is improved in modern off-axis alignment systems where the detector for both reticle and wafer alignment is placed on the wafer stage [33, 34, 36]. Once the wafer is aligned accurately using off-axis alignment systems, light at actinic wavelengths is used to align the reticle to the stage by detecting the image of the reticle alignment mark using the wafer stage detector. The distance between the aligned wafer and the reticle image is then measured using a precision laser stage to determine the exact position where the reticle image should be placed on the wafer. Aligning the reticle image of all layers in a device to the wafer with accuracy can be achieved with this method. This is particularly important in EUV lithography for reasons given in section 3.6.3. To understand the EUV specific issues such as reticle flattening image placement errors and z-height variation induced image placement errors, a discussion on mask blanks used in EUVL is particularly important.

3.2 EUV Substrates

The specifications for EUV mask substrates are given in SEMI P37 standards. Since 35% of light incident on the mask is absorbed and the entire imaging optics in EUV is in high vacuum (no path of heat dissipation), the blanks used in EUVL are fabricated from substrates with low co-efficient of thermal expansion (CTE) to reduce any thermal expansion from substrate heating. Ultra Low Expansion (ULE) and ZERODUR were two types of commercially available EUV substrates with low CTE [28]. ULE glass made by Corning is basically silica containing
titanium oxide (TiO\textsubscript{2}). Changing the concentration of TiO\textsubscript{2} changes the CTE of the substrates. However, including TiO\textsubscript{2} in silica can lead to inclusions and striae which are defects in the substrate that can severely affect the imaging properties of the mask fabricated with these substrates [37]. With the recent advancements in substrate manufacturing, the state of the art ULE substrate have low defects and average CTE of ±10ppb/K [38]. ZERODUR from Shott Lithotec, is a glass-ceramic material made of Lithium Aluminum Silicate (LAS) and achieves low CTE because of the presence of two phases with positive and negative CTE. Materials with CTE as low as ±5ppb/K have been achieved with the LAS systems. Only ULE glass from Corning is commercially available today after Schott stopped producing ZERODUR substrates a few years ago.

Substrate polishing is often done to meet the required substrate flatness and roughness requirements. Precision interferometers are employed to measure the surfaces once polishing is complete. Polishing is often an iterative process with repeated measurements of the surface flatness followed by each polishing step. In the past, non-availability of interferometers with the required accuracy and precision severely limited the final surface roughness and finish. Non-flatness of a substrate can be classified into different types depending on the spatial frequency. This is illustrated in figure 3.2. High Spatial Frequency Roughness (HSFR) can lead to intensity loss due to scattering of light from the reticle resulting in lower throughput. HSFR can be smoothed out during ML deposition. MSFR and LSFR cannot be corrected by the smoothing ML deposition method and can cause image placement errors on the wafer as detailed in section 3.6.3.

The flatness requirements from SEMI P37 standards are given in table 3.1. However, to achieve the substrate flatness requirements in the SEMI P37 standards require very aggressive polishing techniques. It has also been reported that post polishing processing by either magneto-rheological finishing (MRF) and ion beam figuring (IBF) can improve the final surface finish of the substrates [39]. While MRF can use surfaces that have been polished previously, it requires an additional
defect removal and polish step to reduce defects and roughness. This adds to the
cost of fabricating a EUV mask and is not preferred. IBF is a lengthy process that
can be employed to achieve both flatness and reduce roughness. It has generally
been reported that aggressive polishing leads to additional blank defects [40] which
in turn affect device performance. Hence substrate flatness requirements need to
be re-considered with specifications for flatness and defects density being satisfied
simultaneously. This is discussed in more detail in chapter 4.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Type A</th>
<th>Type B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
</tr>
<tr>
<td>Back side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
</tr>
<tr>
<td>Wedge angle</td>
<td>≤ 100 µrad</td>
<td>≤ 100 µrad</td>
</tr>
</tbody>
</table>

Table 3.1: Flatness requirements for EUV Substrates

3.3 Blank Fabrication Process

EUV blanks are fabricated from low CTE substrates by depositing ML of Mo/Si
to reflect EUV light. The reflectivity of the ML is dependent on multi-layer period
i.e. $\lambda/2$, and the multi-layer parameter $\gamma$ which is the ratio of the thickness of
the high Z layer (Molybdenum) to the ML period. Challenges in depositing these
ML’s are almost the same for masks as for EUV optics. Some of these basic challenges have been discussed in section 2.3. The specifications for ML for EUV blanks are also very similar from EUV optics. Typically about 40 pairs of Mo/Si are deposited in order to provide adequate reflectivity and also defect free ML coatings. However, since EUV masks are often inspected for defects and need to be repaired, 50 ML of Mo/Si are often deposited instead of 40 pairs. Although adding 10 ML pairs only improves the reflectivity by \(\sim 1\%\), it prevents any loss in intensity from accidental damage to the ML coating from mask clean or absorber defect repair process. Since EUV masks are essentially master copies of the circuit patterns, the masks are often cleaned for any particles on the surface and other impurities accumulated from the day to day handling process. To protect the ML during the cleaning process, a buffer layer is often deposited between the absorber and the ML and forms a part of the absorber stack. Since the ML’s are terminated with Si, a small layer of native oxide is formed on the top surface of the ML. It has been found that the reflectivity of the ML drops due to the presence of this surface oxide. EUV irradiation in the presence of water molecules promote surface oxidation, thereby compounding the problem [41]. A capping layer is often deposited between the ML and the buffer layer to prevent the oxidation of Si from EUV irradiation [42]. Ruthenium is one such capping material because of its inertness to oxidation and etch selectivity with the absorber thereby doubling as a buffer layer as well. Use of Ru capping is advantageous since it can reduce the height of absorber stack (buffer+absorber), reducing H/V bias and shadowing effects. The absorber layer is deposited on top of the ML cap and buffer layers. The thickness of the absorber affects the shadowing and hence a smaller thickness absorber layer is preferred. Some promising absorber materials include Ti, TaN, Cr, W etc. TaN is by far the most commonly used absorber material in EUV blanks due to the high absorbance even at low thickness values (\(\sim 45\) nm) [43]. In order for the blanks to be inspected at both actinic and DUV wavelengths, an anti-reflective coating (ARC) is needed on top of the absorber in order to reduce
the absorber reflection at DUV wavelengths. Actinic inspection, i.e. inspection at EUV wavelengths in order to identify printable defects on the blank, can be done without using an ARC layer. Finally, a back side conductive layer is deposited in order for the blanks to be clamped in EUV tools using electrostatic chucks. Figure 3.3 shows the various steps involved in the fabrication of a EUV blank. The final blank with the entire stack is shown in step 5 of figure 3.3.

Figure 3.3: Process flow describing the fabrication of a EUV blank from a Low CTE substrate.

### 3.4 Non-flatness of EUV Blanks

Each additional layer of material that is deposited on the low CTE substrate strains the substrate due to lattice and thermal mismatch strains [44]. The strain causes stress in the substrate resulting in deformation. The amount of stress induces can be calculated by measuring the substrate deformation. The relationship between stress and substrate deformation (approximated as simple curvature), is given by Stoney’s equation as

\[
\sigma_f = \frac{K E_s t_s^2}{6 t_f (1 - \nu_s)}
\]  

(3.2)
where, \( \sigma_f \) is the isotropic film stress resulting in a perfectly spherical substrate curvature, \( K \) is the substrate curvature caused by \( \sigma_f \), \( E_s \) is the elastic constant of the substrate, \( t_s \) is the thickness of the substrate, \( t_f \) is the thickness of the deposited film and \( \nu_s \) is the Poisson’s ratio of the substrate. For example [45], consider the case of a EUV blank with 40 pairs of ML of Mo/Si, 45 nm SiO\(_2\) buffer oxide, 150 nm absorber and coated with 320 nm of e-beam resist. The amount of stress contribution due to these individual layers is given in table 3.2.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness(nm)</th>
<th>Stress(MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 Pairs of Mo/Si ML</td>
<td>280</td>
<td>420 (Compressive)</td>
</tr>
<tr>
<td>Buffer Oxide SiO(_2)</td>
<td>45</td>
<td>81</td>
</tr>
<tr>
<td>Absorber</td>
<td>150</td>
<td>52</td>
</tr>
<tr>
<td>Resist</td>
<td>320</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 3.2: Individual Stress contributions from the different layers deposited on the substrate prior to mask patterning.

From table 3.2, it can be seen that the most significant stress contribution is from the Mo/Si ML. The magnitude of stress increases with number of ML pairs. The type of stress (compressive or tensile) introduced by the Mo/Si ML film is dependent on the \( \gamma \) ratio of the structure. Figure 3.4 shows the deformation of a EUV blank fabricated from a ULE substrate after film deposition. The starting substrate has a Peak-Valley (P-V) non-flatness of 60 nm. Each layer that is deposited adds a certain amount of strain resulting in a final deformed shape. The final P-V non-flatness number is 1310 nm. This final shape of the EUV blank is calculated using Finite Element Modeling (FEM). The parameter \( \gamma \) in the above example is \( 2.8/7=0.4 \) which results in a ML film with compressive stress of 420MPa for the 40 bi-layer pairs.

### 3.5 Electrostatic Chucks

Electrostatic chucks are used in EUV tools to clamp and flatten the back side of the mask during exposure. Due to the nature of the optics design on the ASML EUV ADT, the mask is held upside down in the tool. The use of electrostatic
Figure 3.4: Deformation of a ULE substrate due to ML, buffer, absorber and resist deposition. The final deformed shape is calculated using a FE modeling.

chucking is necessitated because the imaging optics is under high vacuum, making it impossible to use vacuum chucks. As a result electrostatic chucks have been widely deployed in EUV tools. Electrostatic chucks also serve another important purpose i.e. provide a uniform clamping force to the mask back side in order to flatten the bow from thin film deposition on the substrate. There are two primary types of electrostatic chucks namely,

1. Unipolar chucks

2. Bipolar chucks

Figure 3.5: Schematic diagram of the two types of electrostatic chucks.

Figure 3.5 shows a schematic of the two types of electrostatic chucks. Unipolar chucks are essentially capacitors with the mask back side and the chuck being the
two capacitor electrodes. The electrodes are separated by a dielectric material. A DC voltage is applied between the mask and chuck inducing opposing charges on the mask back side and the electrode on the chuck. The clamping force generated by a voltage $V$, applied across the electrodes separated by a dielectric of thickness $d$ and dielectric constant $\epsilon_r$ is given by,

$$F = \frac{A\epsilon_0\epsilon_r^2V^2}{2(d + \epsilon_r g)^2}$$  \hspace{1cm} (3.3)

where, $A$ is the electrode area and $g$ is the air gap between the back side of the mask and the dielectric. Although the chuck is brought into contact with the mask back side, due to the roughness of the surfaces in contact and the non-flatness errors of the mask and the chuck, there is always an air gap present between the dielectric and the mask. Unipolar chucks are simple to fabricate since they have one electrode surface. As a result, controlling the flatness of the chuck and dielectric material is simpler as a result. However, a unipolar design required a physical charge transfer path between the mask and chuck. Charge transfer is completed through some form of physical contact which must be present until the clamping process is complete. Another disadvantage of the unipolar design is that once clamped, masks held in a unipolar chuck have electrical charge and can cause damage to the mask patterns (due to strong electric fields across patterns) if the charge gets transferred to the front side of the mask.

A bipolar chuck has two electrodes that have a potential drop across them. The equation 3.3 can also be used to describe the force generated by a bipolar chuck. As in the case of a unipolar chuck a charge is induced on the conductive back side of the mask. However, the charge induced on the mask is dependent on the polarity of the electrode under the mask. Hence, different areas of the mask are clamped by positive or negative charges. If the electrodes areas are identical and the dielectric thickness and contact area of the mask on the dielectric is identical on both electrodes, there is no net charge transfer to the mask back side. As a result, it is possible to clamp certain non-conducting surfaces with a bi-polar...
chuck. This is possible because the field gradient between the electrode induces a dipole in the object being clamped and thus creates surfaces that are oppositely charged, acting as capacitors. However, in order for the electric field gradient to be uniform, interdigitated electrodes are often used. This is not the case for a conducting surface wherein a simple electrode design as shown in figure 3.5 is sufficient.

An obvious advantage of the bipolar design is that there is no charge transfer between the mask and chuck. However, it is more complicated to design two electrode surfaces covered by a dielectric to the same flatness specification as a single surface. The dielectric thickness uniformity and electrode shapes need to be optimized in order to provide uniform clamping force on the mask. The potential difference between the electrodes can be larger than the potential difference between the electrode and the mask, for certain chuck designs. As a result, the breakdown strength of the dielectric used needs to take this into account. This would mean that the thickness of the dielectric is dictated by the electrode potential difference rather than the electrode to mask potential difference. However, the dielectric thickness can be reduced by increasing the lateral separation between the electrodes. This can create areas under the mask with no clamping force leading to non-uniform clamping. A carefully designed bipolar chuck can theoretically be better than unipolar designs.

3.5.1 Electrostatic Chucking of EUV Masks

EUV masks are written on blanks with a ML coating, absorber stack and a back side conducting layer on them. All of these different layers stress the substrate resulting in a mask non-flatness. During EUV exposure, any non-flatness of the mask pattern surface leads to image placement errors on the wafer. However, during exposure the masks are clamped down using an electrostatic chuck that is designed to provide a uniform clamping pressure to the mask back side. This uniform clamping pressure is designed to flatten the bow induced by the thin film
deposition. If the chucking force applied on the mask is large enough, the back side of the mask becomes conformal with the chuck surface leading to a condition called conformal clamping. For the blank described in section 3.4, the non-flatness of the mask reduces from 1310 nm P-V non-flatness before chucking to 86 nm P-V non-flatness after conformal clamping with a completely flat chuck. The final clamped shape of the mask is shown in figure 3.6.

![Mask clamped on a flat chuck](image)

**Figure 3.6:** Blank with 1310 nm P-V front side non-flatness clamped with 15 kPa on a flat chuck. The as-chucked P-V front side non-flatness reduces to 86 nm.

This conformal chucking of the mask transfers the low spatial frequency back side non-flatness to the top surface. If the chuck surface is completely flat, the top surface of a conformally clamped mask is the blank thickness variation. Thickness variation is defined as any deviation from the ideal mask thickness. Mask thickness is the sum of substrate thickness and the deposited thin film stack. Ideally, the thickness of the mask should be uniform across the entire mask area. However, the characteristic signature of the polishing technique used on the substrate, non-uniformity of the polish and non-uniformities in the thickness of the deposited thin film stack lead to thickness variations across the mask surface. The low order spatial frequency thickness variation gets completely transferred to the top surface of the mask when the mask is clamped conformally on a flat surface. Figure 3.7 shows plots of Legendre polynomial fit to the raw thickness variation and FEM modeling of the mask clamped by a flat chuck with 15 kPa chucking force. This shows that the thickness variation is indeed a good approximation to the final
as-chucked surface shape. Legendre polynomials are typically used to describe the surface shape of EUV masks. More detail about Legendre polynomial and their properties will be discussed in section 3.6.2.1.

![Figure 3.7: Plots showing FEM of a EUV mask being clamped on a flat electrostatic chuck with 15 kPa clamping pressure. As-chucked mask surface is a good approximation to the thickness variation of the EUV blank.](image)

In certain cases, the electrostatic chucks are designed with a set of pins or mesas on the chuck top surface. During routine handling of the reticle, particles may be added to the back side of the reticle. Similarly, during day to day tool operation, some particles may be added to the chuck surface as well. The presence of these mesa structures on the electrostatic chuck reduces the effective area of physical contact between the chuck and the reticle back side. As a result, the probability of a particle being caught between the reticle backside and the chuck top surface is reduced. The reduction in directly proportional to the ratio of the total mesa structure area to the total chuck surface area. A schematic of a bi-polar pin chuck is shown in figure 3.8.
3.6 Modeling for Image Placement Error Calculations

Modeling for IPE calculations require careful measurement of the surface flatness of the EUV blanks followed by a detailed IPE model. The IPE model can be either a Finite Element Model (FEM) or a simple analytical model. The following section describes in detail the process of building a IPE model for EUV blanks.

3.6.1 Surface Flatness Measurements

Reticle flatness measurements are performed on a Zygo Verifire MST 1550 nm Fourier Transform Phase Shifting Interferometer (PSI) at the SEMATECH Mask Blank Development Center (MBDC) in Albany, NY. The mask was held in a vertical test stand so as to negate any effect of gravity. The interferometer used in this project is a Fizeau interferometer. A schematic of a Fizeau interferometer is shown in figure 3.9. The interferometer setup consists of a laser source emitting light at 1550 nm, a set of optics to shape the beam, a beam splitter to split the reflected beams to the CCD for detection of interferograms, a CCD camera to capture the interference patterns, an optical flat to generate a reference beam and the surface to be tested (mask blank).
The interferometer is a Fourier Transform PSI and can simultaneously detect the flatness of multiple surfaces, was used in a 2 surface configuration. The two surfaces in the optical path are a reference flat and the mask. The mask surfaces (front and back) are measured one at a time. The CCD detects the two reflected beams from the optical flat which is also a reference surface and the mask blank which is nominally parallel to the optical flat at all points across the field of the interferometer. The reference flat has a surface that is made partially reflecting to generate the reference beam. The radius of the beam striking the surface is 8 inches. A beam shaping lens systems spreads a laser source emitting 1550 nm light into an 8 inch circular beam. The CCD detects the interference patterns from
the reference beam and the measurement beam. Interference of two beams can be mathematically explained as follows. Let us assume two waves of maximum amplitude $a_1$ and $a_2$, varying sinusoidally so that the amplitude at any given time is,

$$A_1 = a_1 e^{-i\phi_1} \quad \& \quad A_2 = a_2 e^{-i\phi_2}$$  \quad (3.4)

where, $\phi$ is the phase of the wave. The interference of these two waves gives a resultant wave with amplitude $A = A_1 + A_2$ and intensity

$$I = |A|^2$$  \quad (3.5)

$$= (A_1 + A_2) \times (A'_1 + A'_2)$$  \quad (3.6)

$$= A_1^2 + A_2^2 + 2A_1A_2[e^{-i(\phi_1 + \phi_2)} + e^{-i(\phi_2 + \phi_1)}]$$  \quad (3.7)

$$= I_1 + I_2 + \sqrt{2I_1I_2} \cos \Delta \phi$$  \quad (3.8)

where, $\Delta \phi = \phi_1 - \phi_2$ is the phase difference between the two interfering waves. The phase difference between the waves is directly proportional to path difference,

$$\Delta p = \frac{\lambda}{2\pi} \Delta \phi$$  \quad (3.9)

where, $\lambda$ is the wavelength (1550 nm). Depending on the intensity of light measured by each pixel of the CCD camera, the path difference can be identified. The nominal path difference between the two waves is known from the separation of the optical flat from the EUV mask. However, the measured path difference is then compared to the nominal path difference to calculate the non-flatness of the mask surface. The interferometer used for EUV mask flatness measurements has a height resolution of $> \lambda/8000$ and a Peak-Valley (P-V) repeatability of $\lambda/1000$. Since the laser source used for making flatness measurements is 1550 nm, the resolution is better than 0.2 nm and repeatability of 1.5 nm or better. The resolution specification translate to $0.2/40 \sim 5\text{pm IPE accuracy (}\Delta z/40\text{).}$ This provides adequate resolution for measuring EUV reticle flatness for IPE modeling.
purposes.

An illustration of the Albany interferometer setup [46] along with a picture of the cleanroom setup is shown in figures 3.10 and 3.11

Figure 3.10: Top-down view of the interferometer setup used to measure mask flatness

3.6.1.1 Flatness Measurement Procedure

1. Power up the interferometer and then start the Metropro software (custom cavity application)

2. Calibrate the instrument by using the calibrate wave monitor icon located in the measure controls window. The instrument has to be calibrated each time it is turned on.

3. Align the test mask surface and the reference flat surface to the interferometer. Surfaces are aligned using the Align/View button on the remote and tipping/tilting the mask surface. The align/view button toggles the interferometer from the viewing mode to the aligning mode and shows spots of multiple surfaces and a cross hair. Each spot represents a surface of different optical components in the test bench setup that are in the path of the laser.
Figure 3.11: Side view of the vacuum apparatus sitting on the vibration isolation table, arrows indicate the direction of the laser path coming from the interferometer and entering the chamber through the optical window after being deflected by the folding mirror. The laser takes the same path back to the interferometer after reflecting from the mask surface.

Aligning of the surfaces will be complete when the corresponding spots of the reference flat and the mask surfaces are super imposed on the crosshairs. An example of proper alignment is given in figure 3.12.

4. Fine adjust the spots to achieve the best null possible of all fringe patterns.

5. Depress the Align/View button to shift the video monitor back to the viewing mode where the fringes are visible.
6. Use the mask data icon for the calibration marker window

7. Press the calibration marker icon

8. Position the cursor over an area of valid data and click over it to include the calibration marker over the fringe pattern. The data obtained from this marker location will be used for reporting measured cavity OPD (optical path distance) and to display the OPD spectrum plot data.

9. Enter the value in the maximum gap OPD. This value represents the optical path of the longest measuring surface in the test setup.

10. Enter the value in the minimum gap OPD. This value represents the smallest optical path distance corresponding to the test surfaces in the apparatus.

11. Click the measurement button to acquire the data. Once the measurement is done, the monitor will show a mask intensity plot and an OPD spectrum plot.
12. From the OPD spectrum plot confirm the number of first order peaks that corresponds to the number of surfaces in the path of the laser that were under the test. There are \( N \times (N-1)/2 \) number of peaks, where \( N \) represents the number of active surfaces.

13. An OPD spectrum plot represents the peaks corresponding to the surface of interest located appropriately at the OPD location along the x-axis of the plot.

14. Click on the peak of interest on the OPD plot, the peak location represents to the optical path distances between two surfaces.

15. Analyze the selected peak by clicking on the analyze peak button on the OPD window. At this time, the software will analyze the peak that corresponds to the surface of interest and will show the profile of the surface.

16. In one measurement surface profiles of the front surface (pattern surface) and the back surface (chrome coated for chucking) of the mask can be obtained.

17. Save the data for further analysis.

3.6.1.2 Flatness Measurement - An Example

The output from the Zygo phase shifting interferometer can be formatted in a number of ways. The output is viewable in Metropro software, available from Zygo. The flatness data can be exported from Metropro into a number of formats for use in other applications. The format used in this work for IPE modeling is the XYZ format. While the z-resolution of the interferometer tool is \( \lambda/8000 \), the spatial resolution is important for modeling considerations also. The spatial resolution is the spacing between interferometric measurements on a sample. This spacing is determined by the measurement spot size of the interferometer. The measurement spot size for all flatness measurements was set to 636\( \mu \)m. The flatness data is reported over the quality area of the reticle. The reticle quality area, specified in
the SEMI P37, is the central $142 \times 142 \text{ mm}^2$ of the reticle. Since the measurement spot size is $636 \ \mu\text{m}$, there are $224 \times 224$ measurements within the quality area of the reticle. This spot size establishes a high spatial frequency cut off point i.e. any flatness change with spatial frequency higher than $1/636\mu\text{m}^{-1}$ will not be completely captured by the interferometer. The area containing patterns on a EUV reticle is typically smaller and depends on the scanner illumination geometry and projection optics.

Figure 3.13 is a 3-D plot of the front side and back side flatness of an EUV substrate (LTEM - Low thermal expansion material) after final polishing. The substrate has been polished to $<100 \ \text{nm}$ flatness specification for each surface. This substrate represents the current state of the art substrate available from EUV substrate vendors. The front and back side flatness measurements were performed with the reticle held in a vertical test stand. The vertical test stand minimizes the effect of gravity sag on the measurement. As described in section 3.6.2.1, any rectangular surface can be described in terms of a series of Legendre polynomials. A term called bow describes the spherical nature of a substrate. This is important since a simple spherical substrate can be completely flattened by electrostatic chucking on the EUV ADT. Hence the percentage of non-flatness

![Substrate Flatness Measurements](image)

**Figure 3.13:** Flatness measurement of a substrate polished to $\leq 100 \ \text{nm}$ flatness specifications measured on the vertical test stand at the Sematech MBDC in Albany. The flatness shown is over a $140 \times 140 \ \text{mm}^2$ area.
arising from a simple spherical term is an important aspect of substrate flatness.

Figure 3.14 is the front side and back side flatness of an EUV substrate (LTEM) polished to optical lithography grade flatness specification i.e., 250 nm flatness. Figure 3.15 is the front and backside flatness of a EUV blank (post thin film deposition) made from an optical grade flatness substrate. The bow contribution to the substrate shape has increased from 100 nm of bow to over 1000 nm of bow.

Figure 3.14: Flatness measurement of a substrate with optical grade flatness specification on the vertical test stand at the Sematech MBDC in Albany. The flatness shown is over a $140\times 140 \text{ mm}^2$ area.

Figure 3.15: Flatness measurement of a EUV blank after multi-layer and other thin film deposition fabricated from a substrate ith optical grade flatness specification. The flatness shown is over a $140\times 140 \text{ mm}^2$ area.
3.6.2 Reticle Flattening IPE

EUV mask bow is flattened during electrostatic chucking. However, when the masks are fabricated, the mask write step is typically done on an electron beam writer which exposes a resist coated mask with the appropriate patterns. The EUV mask mounting requirements were specified in SEMI P40 standards which detailed the specification for mounting requirements for EUV masks. It was initially planned that the mask exposure (in EUV tool) and mask write (in e-beam tool) use similar electrostatic chucks. This would ensure that any in-plane distortions resulting from the mask chucking process will also be identical during mask write and mask exposure. However, since the original draft of the SEMI P40 standards, the mask houses have subsequently decided use 3-point kinematic mounts to write EUV masks. Kinematic mounts have been used by mask shops to write optical masks for a long time. Mask writer infrastructure for optical mask making did not require electrostatic chucking of blanks during mask write. EUV masks have not been manufactured in large enough quantities to justify upgrading or adding electrostatic chucking capability to the electron beam mask writers. It has also been reported that, mask writers can suffer from image placement errors due to the charging of mask substrates during patterning [47, 48, 49], depending on the electrical conductivity of the EUV masks. This substrate charging occurs from fringe fields extending from electrostatic chuck electrodes to the mask pattern surface.

The use of kinematic clamps which are essentially 3-point mounts during mask write means that the EUV masks are in a bowed state during mask write. The contribution to mask bow comes from both the starting blank shape due thin film deposition and gravity sag from the weight of the blank. The starting mask bow or non-flatness from Mo/Si ML, absorber stack and back side conductive layer deposition was discussed in section 3.4. The gravity sag in a 3-point mount is typically corrected by using a compensation table in the mask writer job deck. The gravity sag in a 3-point kinematic mount is calculated using a finite element
model. This model predicts the amount of sag over the entire area of the mask [50]. Since this gravity sag can be predicted accurately, a pattern off-set can be programmed into the e-beam writer job deck such that pattern placement errors from mask writing is zero when the substrate recovers is nominal shape. However, the mask which is nominally bowed gets flattened during electrostatic chucking. This as-chucked mask has pattern placement errors because of in-plane distortions introduced by the flattening process. This flattened substrate with the pattern placement error gets transferred to the wafer during imaging, undergoing a demagnification of 4 (for the projection optics used on the ASML EUV ADT). A schematic of the mask processes steps post ML deposition leading up to EUV exposure is shown in figure 3.16.

![Figure 3.16: A EUV substrate post thin film deposition is patterned on a ebeam tool on a 3-point mount and then chucked flat using an electrostatic chuck on the EUV tool. The difference between the two clamping methods between the ebeam and EUV tool is the cause of IPE from reticle flattening.](image)

Reticle flattening during electrostatic chucking can also be predicted using Finite Element Modeling (FEM). In order to setup an accurate FEM, details of mask front side and back side non-flatness, material properties of the various thin films deposited on the mask substrate, material properties such as stiffness coefficient of the substrate itself along with electrostatic chuck geometry, electrode configurations, clamping pressure and friction coefficient between the mask backside and the chuck top surface need to be known. Using Finite element models, it is possible to change the mask-chuck system parameters such as chuck stiffness, properties of
A second method for predicting reticle flattening is by using analytical methods. Full FEM’s can take a significant amount of time to finish, depending on how they are setup. A simple FEM can be run much faster but may not be accurate enough to predict the surface distortion changes to the accuracy required for IPE calculations. Often times, a simple analytical models can be used in place of FEM, provided certain conditions are satisfied. In the case of the electrostatic chuck-mask system, the assumptions that go into the modeling reticle flattening from chucking involve chuck stiffness, chuck flatness, chucking voltage or force, friction co-efficient of the interface between the chuck and mask etc. FEM for reticle flattening typically have the following assumptions:

1. Chuck Stiffness

   Chuck is assumed to be infinitely stiff for modeling purposes. An infinitely rigid chuck does not deform under clamping pressure, irrespective of the chucking force and stiffness of the mask. This also means that with sufficient clamping pressure, the backside of the mask resembles the shape of the chuck top surface.

2. Chuck Flatness

   The chucks for EUV tools are made to specifications given in SEMI P40 standards. The standards specify a chuck flatness of ≤30 nm. A chuck with flatness of 30 nm of better is considered flat when compared to the flatness of the EUV blanks (typically ≥1µm).

3. Clamping Pressure

   Clamping pressure for reticle chucking should be sufficient to hold the reticle without any slipping during exposure. Since the ASML EUV ADT is a step and scan lithography system using ring field illumination, an arc of light is scanned along the reticle during exposure. The clamping pressure applied on the reticle should be sufficient to prevent any lateral motion of
the reticle during exposure. SEMI P40 standards also specify the mean clamping pressure to be 15 kPa (used in the ADT).

4. Friction Co-efficient

The friction co-efficient of the chuck-mask interface plays an important role in the final as-chuck shape of the reticle. The friction co-efficient is directly related to the tendency of the reticle to slip/slide during clamping. The lower the friction, the easier it is to get the mask to flatten on the clamp. From equation 3.10 it is also seen that the friction coefficient determines the minimum clamping pressure in EUV tool.

\[
\mu \left( \frac{F}{k} - mg \right) > ma
\]  

(3.10)

where, \( F \) is the force applied on the reticle by the electrostatic chuck, \( k \) is the safety factor, \( \mu \) is the friction co-efficient between the mask-chuck interface, \( a \) is the maximum acceleration of the reticle stage during exposure. It can be calculated from equation 3.10 that for a clamping pressure of 15 kPa, the safety factor \( k = 5 \).

FEM for reticle flattening on the EUV ADT assume a infinitely flat, rigid chuck with 15 kPa clamping pressure and a chuck-mask friction co-efficient of 0.2.

3.6.2.1 Legendre Polynomial Description of Reticle Surface

Analytical models for in-plane distortion calculation are based on reticle surface slopes. In order for the surface slope to be calculated, the surface needs to be expressed as a function of position \((x, y)\). The z-height is the dependent variable i.e. \( f(x, y) \). A convenient method for describing rectangular shaped surfaces is in terms of Legendre polynomials [53]. Legendre polynomials are an orthogonal basis set over the interval -1 to 1. They can be derived as a natural solution to the Laplace’s equation in spherical co-ordinates for multipoles. They can be generated
by Gram-Schmidt orthogonalization of monomials $x^i$ and is given by,

$$P_n(x) = \frac{1}{2^n n!} \frac{d^n}{dx^n}(x^2 - 1)^n$$  \hspace{1cm} (3.11)$$

where, $n$ is the order of the Legendre polynomial. The inner product of these polynomials are orthogonal over $[-1,1]$. This means that,

$$\int_{-1}^{1} P_n(x) \times P_m(x) dx = \frac{2}{2n+1} \delta_{mn}$$  \hspace{1cm} (3.12)$$

where, $\delta_{mn}$ is the Kronecker delta function.

A plot of the first 4 orders of Legendre polynomial over the interval [-1,1] is shown in figure 3.17. The order of the polynomial is also equivalent to the spatial frequency of the polynomial function. Hence, if the independent variable in the polynomial function is $P_n(x)$ is distance on the reticle, flatness of any reticle surface can be described by a combination of Legendre polynomials of various orders.

![Figure 3.17: The first 5 Legendre polynomials are plotted over the interval [-1,1].](image)

The surface roughness of a EUV mask can be separated into spatial frequencies of different orders. The surface of a reticle can be written as

$$R_z(x, y) = \sum_{N=0}^{L} \sum_{M=0}^{L} c_{m,n} P_n(x)P_m(y)$$  \hspace{1cm} (3.13)$$
where, $R_z(x, y)$ is the reticle $z$-height variation and $P_n(x)$ is the $n^{th}$ order Legendre polynomial. The constant $c$ is the weight or the fit co-efficient, that depends on the magnitude of the $n^{th}$ order spatial frequency component in the roughness.

This method of representing the reticle surface as a function of Legendre polynomials is a significant step in determining the amount of reticle distortion resulting from chucking. In particular, the order of the polynomial used to represent the reticle surface should be carefully selected. In order to capture with sufficient detail all the roughness variation on the reticle surface, a certain minimum order of polynomial should be used. If the order used to describe the reticle surface is lower than required, some of the higher order spatial frequency roughness will not be captured and as a result, the local surface slope calculated for IPE IPD will be incorrect resulting in incorrect IPE calculation. Polynomial order of 7 has been found to be optimal [53] to capture the necessary surface roughness. Figure 3.18 shows the difference between a 8x8 (7th order) polynomial fit and the measured surface flatness is minimal.

![Figure 3.18](image)

Figure 3.18: Plots comparing $8 \times 8$ polynomial fit and the actual measured surface of a reticle. Maximum difference between the raw and fit data is 40 nm P-V

### 3.6.2.2 Analytical Model for Reticle Flattening

Analytical model for reticle clamping is often used as a simpler approximation of a full Finite Element Model (FE Model). Analytical models can predict with the required accuracy the reticle distortion when conformally clamped using rigid
chucks. The amount distortion from reticle flattening is given by,

\[ \Delta x = k \frac{\partial z}{\partial x} MT \quad (3.14) \]
\[ \Delta y = k \frac{\partial z}{\partial y} MT \quad (3.15) \]

where, \( \Delta x \) and \( \Delta y \) are the components of \( \text{IPE}_{\text{IPD}} \). From figure 3.19, the factor \( k \) is the ratio of the location of the neutral axis from the front side of the reticle, \( M \) is the magnification which is 4 for wafer level IPE and 1 for reticle level IPE and \( T \) is the thickness of the reticle, nominally 0.25 inches for EUV substrates.

![Figure 3.19: Illustration of local slope calculation from a bowed reticle. Surface slopes are calculated from flatness measurements in a interferometer.](image)

**3.6.2.3 IPE\(_{\text{IPD}}\) Example - Analytical Method**

To calculate the IPE from flattening or in-plane distortion (IPD), consider the non-flat substrate shown in figure 3.20. The back side surface flatness prior to chucking was measured to be 650 nm over \( 140 \times 140 \text{ mm}^2 \) area. The surface slopes \( \partial z/\partial x \) and \( \partial z/\partial y \) are calculated from this back side non-flatness. The neutral axis location is taken to be the mid-point of the reticle cross-section. Hence the value of \( k \) from equation 3.15 is 0.5. The surface distortion after the reticle is conformally clamped on a flat chuck is also given in figure 3.20. This distortion of the surface gets demagnified by a factor of 4 by the projection optics on the
wafer. The maximum reticle image placement error along x and y directions are 26 nm. It is also quite clearly seen that at the center of the reticle, the magnitude of slope is the smallest. The IPE at the center of the reticle is also the smallest consistent with the surface slope. The IPE increases along both x and y axis away from the center, consistent with the increase in the magnitude of surface slope. This type of surface distortion can mathematically be expressed as \( \delta x = m_x x \) and \( \delta y = m_y y \), where \( \delta x \) and \( \delta y \) are the x and y components of vector error at any point on the reticle. \( m_x \) and \( m_y \) are the magnification coefficients. The magnification coefficients can be calculated by a least squares fit. The x-direction magnification coefficient is 0.53 ppm for this example. At the corners of the reticle (x = 45 mm, y = 60 mm), where the errors are the largest, the contribution from this x-magnification is 0.53 ppm \( \times \) 45 mm = 23.8 nm. The maximum x-error vector is 26 nm, which means that the x-mag contribution is 90%. The same argument can be followed to verify that a large portion of the y-errors also manifest itself as magnification errors. This is important since most modern scanners can correct for reticle magnification and other linear error terms. As a result, the errors from surface distortion results in very small errors on the wafer.

![Non-flatness of EUV blank (Before Chucking)](image1.png)

![Surface distortion from Chucking](image2.png)

**Figure 3.20:** Illustration of reticle flattening from electrostatic chucking. (a) Reticle back side flatness measured from the interferometer and fit to a \( 8 \times 8 \) Legendre polynomial. (b) Surface distortion vector plot as a result of flattening during reticle chucking.

The location of the neutral axis depends on the how many layers are deposited on the substrate and also the location of the layers. Methods reported in literature
from INTEL [51] and NuFlare [52] have different neutral axis locations. The neutral axis location determines the amount of $\text{IPE}_{\text{IPD}}$ from non-flatness. In a recent publication [53], it has been shown that the location of the neutral axis is at the center of the reticle provided that the resist removal and absorber etch processes are assumed to change the stress on the substrate negligibly. However, for cases where there is significant stress change with resist and absorber removal, the location of the neutral plane is different and depends on the thickness and material property of the resist and the percentage of absorber removed. For a 100 nm thick resist with 150 kPa pressure that is removed completely during develop and a TaBO on TaBN absorber stack that is 80 nm thick inducing 160 kPa of stress and 90% post patterning removal, the location of the neutral axis shifts from the center of the reticle by 0.389 mm. However, the location of the neutral is a secondary effect compared to the surface slope of the mask. The change in the neutral axis location essentially changes the magnification co-efficient since $k$ is a constant term in the $\text{IPE}_{\text{IPD}}$ calculation. This magnification term eventually ends up being tool correctable and does not contribute to wafer IPE. It should also be noted here that the value of $l$ is dependent on the percentage of absorber material removed. It needs to be understood better if the change in pattern density between different regions of the reticle can affect the reticle distortion from chucking. As a result, instead of a constant value for $k$, a $k(x, y)$ which is dependent on local pattern density can result in a more accurate estimate of reticle distortion from chucking. A local variation in $k$ can significantly affect $\text{IPE}_{\text{IPD}}$, since the magnification also becomes a local effect, which will end up as non-correctable errors.

### 3.6.3 IPE from Out of Plane Distortion

Although the reticle is flattened during clamping, any thickness variation present on the mask gets transferred to the patterned surface of the mask. The back side clamping distorts the back side to become conformal with the chuck surface. The
final chuck surface non-flatness can be approximated as the thickness variation of the mask. Since EUVL uses non-telecentric illumination, any non-flatness on the patterned surface results in additional image placement error. This IPE due to mask surface z-height variation is called IPE_{OPD} or IPE_{z-height}.

Figure 3.21: Illustration of image placement error resulting from reticle plane non-flatness in EUVL

As shown in figure 3.21, the axial displacement of the object plane i.e., reticle, results in lateral displacement of the image at the wafer plane. For a given non-flatness of $\Delta z$, the amount of image placement error $R$ can be calculated mathematically as follows. From figure 3.22, it is seen that,

$$\tan \phi = \frac{\Delta x}{\Delta z} \quad (3.16)$$

At the reticle plane, a non-flatness of $\Delta z$ results in an IPE of $\Delta x$. The light reflected from the reticle passes through the projection optics with a demagnification of 4. As a result, the IPE at the wafer level $\Delta R$ for 6° angle of incidence is given by,

$$\Delta R = \frac{\Delta z \times \tan \phi}{4} \approx \frac{\Delta z}{40} \quad (3.17)$$
3.6.3.1 Non-telecentric Illumination of EUV Reticles

The EUV Alpha Demo Tool (ADT) uses a 6-mirror projection optics. The projection optics has a region of minimum aberration in the form of a ring. Only a small fraction of the reticle fits within the ring. Reticle illumination is shaped such that, only the portion of the reticle that fits within the ring field is illuminated. Figure 3.23 shows the reticle illumination on the EUV ADT. The angular extent of the arc on the reticle i.e. $2\theta$ is $49.2^\circ$ [54].

![Reticle Illumination - Top View](image)

Figure 3.23: Reticle Illumination setup on the ASML EUV ADT
The chief ray angle of incidence (CRAI) across the slit is 6°. Figure 3.24, shows CRAI across the slit is a constant value of 6°. The chief ray angle of incidence is the angle subtended by the the central ray of the ray bundle at the reticle surface. In the case of EUV reticles, this angle $\phi$ is shown in figure 3.24.

![Figure 3.24: Chief ray angle of incidence across slit on the ASML EUV ADT.](image)

Ring field illumination is achieved through the use of illuminator mirror assembly and a reticle masking system. This ring field illumination on the reticle which is in the shape of an arc is commonly referred to as the illumination slit. Typical 6 mirror optics designs for imaging at EUV wavelengths use a 2 mm arc width [28].

In order for the reticle field to be completely imaged, the reticle is scanned along the y-direction so that all portions of the reticle field gets exposed with EUV light. This ring field illumination of the reticle has an more subtle effect on the x and y components of IPE. Equation 3.17, gives the magnitude of IPE for a CRAI of 6°. However, the X and the Y components of wafer IPE, depend on the position across the ring field. Figure 3.25 illustrates how the X and Y components of IPE change across the reticle.

The values of $R_x$ and $R_y$ are given by,

\[ R_x = R \sin \theta, \quad R_y = R \cos \theta \]  

(3.18)

where,

\[ R = \frac{z \times \tan \theta}{4} \]
Figure 3.25: Components of image placement error across the ring field varies as a function of \( \theta \).

An example of IPE\(_{\text{OPD}}\) calculation is shown in figure 3.26. The maximum vector error is 26 nm.

Figure 3.26: An example of IPE\(_{\text{OPD}}\) calculation for a reticle with large thickness variation. The OPD contribution is quite large with a maximum vector error of 26 nm.

### 3.7 Tool Contribution to Image Placement Errors

The contributions to image placement errors in lithography tools arise from a number of factors. Reticle non-flatness is one of the factors contributing to image
placement errors. Any misalignment of the reticle and wafer, lens distortion, errors in wafer stage motion, errors in speed matching of the reticle stage and wafer stage (for 4x demagnification) and wafer distortion on the wafer chuck can result in image placement errors. In modern scanner, most of these errors are controlled and minimized by the use of carefully designed alignment marks on the reticle and the wafer. The reticle alignment to the wafer stage is one of the most important aspect of tool alignment. On the EUV ADT, the reticle frame that is patterned on every reticle used on the tool needs to have a set of pre-alignment and alignment marks in specified reticle co-ordinates. This placement of alignment marks at known co-ordinates enables the EUV tool locate the reticle within the tool relative to the rest of the optical system. On the EUV alpha demo tool, the reticle alignment marks are called transmission image sensor (TIS) marks. These marks essentially are a set of gratings of different pitch and orientation. The wafer stage has a detector that can record the aerial image of the TIS mark using photodiodes to record the aerial image intensity as a function of (x,y,z) on the wafer stage. The peak in the aerial image intensity can then be related to the nominal position of the reticle in the tool. Presence of multiple TIS marks on the reticle frame enables estimating reticle magnification, rotation and translation and correcting for these errors during EUV exposure of the reticle.

The second aspect of tool alignment is to align the wafer in the wafer stage to the remainder of the optical system. This is typically accomplished with the use of wafer alignment marks that are pre-patterned on the wafer prior to exposure. As with reticle alignment marks, the alignment accuracy is increased with the use of multiple wafer alignment marks. The distribution of these marks on the wafer and the number of marks used play a critical role in the final wafer alignment accuracy. It is typical on 300 mm wafers to use >10 alignment marks on the wafer, depending on the accuracy of the wafer stage on the exposure tool. The marks selected for wafer alignment cover a large portion of the wafer and are symmetrically distributed around the wafer for accurate alignment. Although the
goal of the wafer alignment and reticle alignment is to locate precisely position of each die relative to the reticle and optical system, the system should be capable of adjusting the exposure parameters to offset the difference between the calculated position and nominal positions of the reticle and wafer. These methods are detailed in section 3.8.

The final contribution to image placement errors comes from optical aberration in the projection optics used in the EUV tool. Aberrations are typically any deviations from the nominal path of EUV light as it proceeds from the reticle to the wafer due to imperfections in the optics. Theory of aberration has been studied for optical designs for centuries and is well documented [55]. EUV optics in particular have higher aberrations compared to conventional optical lithography system due to use of mirrors instead of lenses and also from limitations on the number of mirrors that can be used in the EUV projection optics. The EUV ADT uses a projection optics with 6 mirrors while the aberration compensated optics found in typical 193 nm lithography systems uses dozens of lenses to compensate for different optical aberrations. As a result, the collective lens aberrations which are referred to as the lens distortion signature also influences the image placement error. For a more complete understanding of the relationship between different optical aberrations and image placement, refer to [55]. Since the EUV ADT uses ring field illumination and imaging optics, the lens distortion signature has a stronger dependence along x-direction (perpendicular to scan direction) than y-direction.

The International Technology Roadmap for Semiconductors states that the specifications for overlay error to devices manufactured for EUVL masks for year 2012 is 7.1 nm [56], which roughly corresponds to 36 nm DRAM half pitch. In order to achieve the ITRS target for IPE, a budget for IPE contribution from various aspects of the lithography process needs to be developed. A typical strawman budget with the different IPE contributions is shown in figure 3.27.

From the strawman, it is clear that the dominating error contribution is at-
Figure 3.27: Strawman budget for image placement error contribution from the EUV tool and lithography process to achieve the ITRS specification of 7.1 nm overlay error for year 2012.

<table>
<thead>
<tr>
<th>Contribution</th>
<th>M-M Overlay (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tool</td>
<td>4.3</td>
</tr>
<tr>
<td>Process</td>
<td>1.5</td>
</tr>
<tr>
<td>Exposure tool reticle clamp flatness</td>
<td>1.0</td>
</tr>
<tr>
<td>IPD</td>
<td>0.8</td>
</tr>
<tr>
<td>OPD</td>
<td>0.5</td>
</tr>
<tr>
<td>Reticle clamped in tool</td>
<td>1.6</td>
</tr>
<tr>
<td>Reticle Writing</td>
<td>0.9</td>
</tr>
<tr>
<td>Reticle flatness</td>
<td>1.2</td>
</tr>
<tr>
<td>OPD</td>
<td>0.7</td>
</tr>
<tr>
<td>IPD</td>
<td>0.8</td>
</tr>
<tr>
<td>Bow</td>
<td>0.4</td>
</tr>
<tr>
<td>CTE non-uniformity</td>
<td>0.6</td>
</tr>
<tr>
<td>Total per layer</td>
<td>4.9</td>
</tr>
<tr>
<td>Layer – Layer</td>
<td>7.0</td>
</tr>
</tbody>
</table>

Since the state of the art average flatness of reticle substrates is 90 nm, this translates to 2.25 nm of IPE. In addition to this, the contributions from reticle
flattening and chuck non-flatness, the total contribution from flatness errors is much larger than the allocated 1.9 nm. It has already been shown previously that reticle flattening results in significant surface distortion. For a 650 nm back side flatness, the resulting flattening induced surface distortion has maximum errors of $\sim$26 nm (reticle co-ordinates). In order to reduce the error contributions from non-flatness and tool errors the EUV ADT can correct for magnification, rotation and translation errors.

### 3.8 Scanner Correctable Errors

Achieving perfect overlay between layers i.e. no overlay error, is the ultimate target when printing multiple layers of a chip on a wafer. However in order to achieve this perfect overlay, the errors from the different contributors listed in figure 3.27 needs to be reduced. The EUV ADT can correct for magnification, rotation and translation errors observed on the wafer. These errors are referred to as scanner correctable errors. The correctable errors on the EUV ADT are strictly linear errors. A parametric model for IPE on the EUV ADT can be written as

\[
\text{IPE}_x = T_x + M_x X - R_x Y + m_x x - r_x y + \epsilon_x \tag{3.19}
\]

\[
\text{IPE}_y = T_y + M_y Y + R_y X + m_y y + r_y x + \epsilon_y \tag{3.20}
\]

The coefficients $T$, $M$ and $R$ are wafer translation, wafer magnification and wafer rotation. These are commonly referred to as inter-field errors. Inter-field errors are errors in the placement of the center of each field on the wafer. This is illustrated in figure 3.28. The $m$ and $r$ coefficients are intra-field magnification and rotation. An example of intra-field errors are shown in figure 3.29. These errors occur within a single field on the wafer. A single field is a single exposure of the entire reticle. $\epsilon$ is the residual non-correctable errors that cannot be compensated for by adjusting the scanner settings. The image placement error from reticle non-flatness only results in intra-field errors.
Figure 3.28: Illustration of inter-field errors when printing multiple fields on a wafer. The inter-field errors arise due to imperfect wafer stage motion and misalignment in the reticle and wafer stage during exposure.

In order to determine the correctable errors from the total measured IPE on the wafer a least squares fit is calculated in order to identify the different coefficients $T, M, R, m, r$. Once the coefficients are determined (sample MATHEMATICA® code for determining scanner correctable error is shown in appendix A), the non-correctable errors are then calculated as the difference between total and correctable errors. An example of calculating non-correctable errors from $IPE_{TOTAL}$ (i.e. $IPE_{IPD} + IPE_{OPD}$) is given in figure 3.29.
3.9 Summary

Image Placement Error from reticle non-flatness in EUVL is a critical problem that needs to be addressed for use of the technology in HVM. IPE from reticle non-flatness has two components, from reticle distortion during chucking and residual non-flatness after chucking. In addition to the reticle non-flatness related IPE, error in the reticle stage movement, wafer chucking, wafer stage movement etc. can also contribute to IPE. Wafer IPE in turn affects product overlay when multiple levels are patterned using EUVL or when EUVL is used on a pre patterned wafer. A better understanding of the different contributors to wafer IPE is critical to achieving better product overlay, which is critical to successful device fabrication. Although the EUV ADT can correct for linear error terms, it has been shown that, even with state of the art flatness substrates, the residual (post corrections) IPE from reticle non-flatness is much larger than the ITRS specification of 4.9 nm IPE for year 2012 (based on a strawman budget for IPE contributions). As a result, a technique called flatness compensation has been proposed where the IPE from reticle non-flatness can be compensated for during mask patterning and is the topic of discussion in chapter 4.
Chapter 4

Compensating for Reticle Non-Flatness Effects

4.1 Introduction - Flatness Compensation

Reticle non-flatness induced image placement errors adversely affect overlay in EUV lithography. It has also been shown that polishing substrates to very tight flatness requirements of 100 nm or better leads to increased defects in the substrates. A recent data collected on a set of 10 substrates from a blank vendor shows more blank defects for substrates with tighter flatness specifications and is shown in figure 4.1. The SEMI P37 standards state that the substrate flatness per surface for EUV blanks should be 32 nm or better or 23 nm or better, depending on the type of substrate. However, with some form of flatness compensation the proposed substrate flatness specifications can be relaxed to 250 nm. This is shown in table 4.1. Apart from adding defects, substrates with tighter flatness are time consuming and expensive to prepare often requiring additional cleaning steps to reduce surface defects [57]. As a result, it has been proposed that some form of flatness compensation be employed in order to relax substrate flatness specification and reduce cost of ownership of the technology itself.

Figure 4.2 shows the various steps involved in fabricating a EUV reticle from
Figure 4.1: Increasing defect count as the substrate flatness specifications get tighter.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Type A</th>
<th>Type B</th>
<th>Compensated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
<td>250 nm</td>
</tr>
<tr>
<td>Back side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
<td>250 nm</td>
</tr>
<tr>
<td>Wedge angle</td>
<td>( \leq 100 \mu \text{rad} )</td>
<td>( \leq 100 \mu \text{rad} )</td>
<td>( \leq 100 \mu \text{rad} )</td>
</tr>
</tbody>
</table>

Table 4.1: Flatness requirements for EUV Substrates (with and without flatness compensation)

a blank. The figure also compares the current method of producing EUV reticles against the proposed flatness compensation scheme. The flatness compensation is a method to offset image placement errors induced by reticle non-flatness by introducing pattern shifts during electron beam writing of the EUV mask. The most important requirement for effective implementation of flatness compensation schemes is to estimate the IPE from reticle non-flatness. From figure 4.2, flatness compensation effectively cancels out the image placement errors by introducing error canceling corrections during the mask write step. Mask writers today are capable of compensating for effects of sag from gravity that arise from the fact that the mask is held in a 3-point kinematic mount during electron beam patterning. The sag compensation is predicted by a FE model that takes into account the material properties of the blank being patterned. As a result, flatness compensation, which also uses a compensation table, can be implemented relatively easily, without major changes to the mask writer job deck. Typically, a modified mask writer grid is implemented using predicted image placement error
from reticle non-flatness. The predicted errors can be calculated using either FE
models or analytical models that is based on a geometric approximation of reticle
flattening. This modified electron beam writer grid is then included in the mask
writer job deck. Details of the experimental setup and initial results from flatness
compensation experiments are discussed in this chapter.

Figure 4.2: Proposed method for flatness compensation for EUV reti-
cles.

4.2 Experimental Setup

In order to demonstrate the viability of flatness compensation to relax substrate
flatness requirements, a carefully designed experiment was carried out on the
ASML EUV ADT. The experiment was designed such that the overlay error as
a result of non-flatness can be reduced by flatness compensation. The measure-
ments were carried out as overlay measurements as opposed to absolute image
placement measurements. This was partly due to the fact that the accuracy of
overlay measurements on the EUV ADT is better than 1 nm as opposed to absolute
IPE measurement accuracy of greater than 2 nm. In a production environment,
the most important factor for layer to layer alignment is overlay accuracy. The
absolute image placement numbers are more relevant as only on the mask level,
where the quality of pattern placement is measured with respect to an absolute
grid. Product overlay specifications (on wafer) for year 2012 technology node is shown in figure 3.27. The number that is of concern to this project is the flatness contribution to image placement error of 1.5 nm total based on chuck and reticle non-flatness. 1.5 nm of IPE translates to 2.1 nm (Resultant Sum of Squares) of overlay error from total flatness (assuming uncorrelated IPE for multiple device levels). Flatness compensation if made to work effectively should be able to reduce overlay error values to smaller than 2.1 nm.

4.2.1 Blanks for Flatness Compensation

An overlay experiment was conducted using 2 sets of blanks with different flatness specification. The first blank set called Flat1 and Non-flat1 were fabricated from substrates shown in figure 4.3. The flatness of the blanks after Mo/Si and other thin film deposition on the first set of substrates is shown in figure 4.4. The image placement error resulting from the flat substrate were quite small (after removing correctable errors) and within the reticle flatness allocation. The $3\sigma$ image placement errors from reticle non-flatness for the Flat1 reticle is 0.95 nm over the scanner field. On the other hand, the reticle Non-flat1 has large IPE from reticle non-flatness. The overlay test was conducted such that the Non-flat1 reticle has built in flatness compensation based on different methods and the Flat1 reticle was fabricated with no compensation.

A second set of blanks were also fabricated using the same procedure. The blank flatness of the second set of blanks is shown in figure 4.14. The patterns on the Flat2 blank were written with no flatness compensation and Non-flat2 had flatness compensation built-in. An overlay test of Flat2 and Non-flat2 was performed to test the different flatness compensation algorithms.

4.2.2 Mask Pattern Layout

The pattern layout for both the flat and non-flat reticles consisted of an array of image placement fiducials called the ASML XPA marks that can be exposed on a
Figure 4.3: Set of substrates used for studying flatness compensation methods. Flat and non-flat substrates with different substrate shapes were used to perform overlay tests on the EUV ADT.

Figure 4.4: Blank fabricated from the first set of substrates used for studying flatness compensation methods.
Figure 4.5: Blank fabricated from the second set of substrates used for studying flatness compensation methods. As with the first substrate set, the flat and non-flat substrates were selected with the state of the art flatness and optical grade flatness specifications respectively.

wafer and readout on the EUV ADT for disposition. The mask layout is shown in figure 4.6. The pattern area is 100 mm in x-direction and 132 mm in y-direction. This is representative of the pattern area in a typical full field reticle. The pattern layout consisted of 4 separate layers as shown in figure 4.6. The difference in the flat and non-flat blank pattern is the purpose of the different layers. For the flat blank, each layer is identical and was written with no electron beam writer grid modifications for the purposes of flatness compensation. However, for the non-flat blanks, 3 different flatness compensation schemes were tested. The list of flatness compensation schemes used in the non-flat substrate is as follows:

Layer1 : No compensation

Layer2: University of Wisconsin Finite Element Model
Figure 4.6: Layout of the flat and non-flat reticles for flatness compensation testing. The flat substrates were fabricated with all layers uncompensated while 3 different compensation schemes were built in to the non-flat substrates.

**Layer3**: University of Wisconsin Analytical Model

**Layer4**: NuFlare Technologies Analytical Model

The different algorithms for predicting IPE based on FE and analytical models were detailed in earlier chapters. The predicted IPE from the models is inverted (change in sign) to get a compensation table, which is formatted to an electron
beam writer job deck input format. The input format depends on the electron beam writer used for writing these reticles. Once the compensation table is appropriately formatted and added to job deck, the mask writer will pattern each layer with its corresponding job deck to complete the mask write process. Post write processing steps are common between the flat and the non-flat blanks.

4.2.3 Predicted Errors for Non-flat1 - IPE Modeling

The image placement errors were calculated using both FE models and analytical models. The FE models were used to simulate the chucking of EUV blanks on a flat, rigid electrostatic chuck with a uniform clamping pressure of 15 kPa. The flatness measured by the interferometer at the SEMATECH Mask Blank Development Center in Albany, NY was used in the FE modeling. The FE model and analytical models predict the IPE_{IPD} due to in-plane reticle distortion. IPE_{OPD} or the thickness variation induced image placement error is calculated from the reticle illumination geometry on the EUV ADT. Figure 4.7 shows the IPE_{IPD} and IPE_{OPD} calculations for the Non-flat1 blank. The max x and y vectors are shown in the vector plots. IPE_{TOTAL} is calculated as the sum of the two components is also shown in the figure 4.7. The image placement error vectors are inverted to create a compensation table consisting of (x,y) location and the grid offset for each location. The table is created for a 99×99 array of points over a 140 mm×140 mm area of the reticle. A high order interpolation is performed by the electron beam writer when writing shapes between the array of points input in the compensation table. This array of 99×99 is the densest possible array compatible with the electron beam writer.

All models for IPE calculation use the flatness measurements from the interferometer. The surface is fit to a high order polynomial so as to capture the right range of spatial frequencies for the IPE modeling. Figure 4.8 shows a 8×8 Legendre polynomial fit to the flatness data. At 15 kPa clamping pressure, an 8×8 polynomial fit to the model predicted reticle OPD and the thickness variation are
almost identical. Furthermore, it can also be seen that the modeled and the raw data have negligible differences validating the use of a polynomial fit to the flatness data for IPE calculations. Figure 4.9 shows the $IPE_{TOTAL}$ vector based on the 3 compensation schemes used in the experiment. The predicted errors based on both FE and analytical models are comparable. Figure 4.10 shows the IPE measurements on the mask blanks post electron beam write for each layer. It is seen that the mask IPE data measured using an LMS IPRO tool agrees quite well with the modeled values indicating the mask was written with the right compensation schemes for each of the layers.

**Figure 4.7:** University of Wisconsin analytical model calculation for IPE from the Non-flat1 blank.

**Figure 4.8:** Figure showing the use of $8 \times 8$ legendre polynomial fit for reticle flatness is adequate to capture to the required flatness information needed for IPE calculations.
4.3 Experiments - Set 1

The first set of exposures consisted of a overlay experiment with the Flat1 and Non-flat1 reticles. The exposures form each reticle were separated by a distance of 640µm on the wafer. This small separation between the marks enables an accurate measurement of the distance between the marks. The 640µm separation is part of ASML’s standard overlay measurement recommendation. Figure 4.11 shows the die layout used for this experiment.

The IP errors were measured on the EUV ADT for all fields and averaged after
removing the correctable errors. The non-correctable error or residual error calculation is detailed in section 3.8. The non-correctable errors for different layers is shown in figure 4.12. The largest overlay errors are observed in the Uncompensated layer while the other compensated layers exhibit smaller but similar overlay error numbers. From figure 4.13, it is seen that the smallest overlay errors were observed for the University of Wisconsin Analytical Model. This translated to a 39% improvement in overlay in the y-direction with almost no improvement in the x-direction. For this set of reticles, a slight improvement in overlay is seen as a result of flatness compensation.
Figure 4.12: Residual error from an overlay measurement of Non-flat reticle exposure to Flat reticle exposure. Details on the magnitudes of the errors are shown in figure 4.13.

<table>
<thead>
<tr>
<th>Layout</th>
<th>$x_{\text{max}}$</th>
<th>$3\sigma_x$</th>
<th>$y_{\text{max}}$</th>
<th>$3\sigma_y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncomp</td>
<td>3.5</td>
<td>3.4</td>
<td>6.8</td>
<td>8.9</td>
</tr>
<tr>
<td>UW FEM</td>
<td>3.2</td>
<td>3.3</td>
<td>4.3</td>
<td>5.6</td>
</tr>
<tr>
<td>UW AM</td>
<td>3.1</td>
<td>3.1</td>
<td>4.9</td>
<td>5.4</td>
</tr>
<tr>
<td>NuFlare AM</td>
<td>3.2</td>
<td>3.7</td>
<td>5.0</td>
<td>6.3</td>
</tr>
</tbody>
</table>

Figure 4.13: Magnitude of the x and y $3\sigma$ errors for each layer based on the overlay residuals from exposing the Set 1 reticles. The best overlay results were observed on the layer with UW analytical model based compensation. The net improvement was 39% over the uncompensated layer.

4.4 Experiments - Set 2

Experiments to test overlay between the Flat2 and Non-flat2 blanks were performed similar to the Set 1. The first step in the compensation process was to
measure the substrate flatness. The flatness measurements from Set 2 blanks is shown in figure 4.14. Three models similar to Set 1 was used again to preparing the compensation tables. Initial overlay results show marginal or almost no improvement in overlay error between the compensated and the uncompensated layers. Figure 4.15 shows the overlay errors of the University of Wisconsin analytical and FE models along with the uncompensated layers. These preliminary results show that flatness compensation has not reduced overlay errors for this set of reticles. The reason for this is partially due to the very similar shapes of the blanks used in the overlay study. A more detailed study is being performed to understand the limits of flatness compensation and reticle shapes. Chapter ?? will discuss the relationship between blanks shapes and wafer overlay in more detail.

Figure 4.14: Blank fabricated from the second set of substrates used for studying flatness compensation methods.
4.5 Discussion of Results

The results from the two sets of experiments clearly shows the problems associated with trying to implement flatness compensation effectively. Although a much better improvement was expected in overlay errors from Set 1 reticles, a maximum of 39% improvement in overlay errors was observed. The reasons for the small improvement in the overlay errors can be attributed to either tool clamping errors or an incomplete model. Either way, a better understanding of the assumptions that go into the different flatness compensation models is required to implement flatness compensation effectively. The flatness compensation models, both FE and Analytical assume the following:

1. Clamping Pressure: Uniform chucking pressure of 15 kPa as specified in the SEMI P40 standards is assumed for clamping pressure. The clamping pressure is assumed to be uniform across the reticle back side. If there are non-uniformities in the clamping pressure, the IPE will be significantly different from a chuck providing uniform clamping. It is also possible that the clamping pressure could be uniform but lesser or larger than 15 kPa. The amount of clamping pressure determines the as-chucked shape of the reticle. Too small a clamping pressure will result in non-conformal clamping and
a larger clamping pressure will change the $IPE_{IPD}$ and result in conformal clamping.

2. Chuck Rigidity: An infinitely rigid chuck is assumed in the flatness compensation models. An infinitely rigid chuck implies that the chuck shape does not change during reticle clamping. A semi rigid chuck will deform along with the reticle during clamping. As a result, the as-chucked shape of the reticle top surface, although conformal with the chuck will be different for a semi-rigid chuck compared to an infinitely rigid chuck.

3. Chuck Flatness: The models assume that the flatness of the chuck top surface is completely flat and is generally neglected compared to the large flatness numbers of the reticle surfaces. If the reticle has a large convex or concave shape, the final IPE from clamping a reticle on a non-flat chuck will be significantly different.

The small improvements in overlay for Set 1 could be possible due to either one of the above factors or a combination of them. As for Set 2 reticle, although the reticle has large flatness, the non-correctable errors as a result of reticle non-flatness is quite small. As a result, the IPE signatures on the wafer are quite small and the improvements from flatness compensation fall almost within the noise floor of the tool. The noise floor is determined by measurement errors, repeatability of chucking etc. As a result, there are cases where the reticle shapes are matched such that flatness compensation does not result in any improvement in overlay errors. A more detailed discussion of these cases is presented in chapter 7.
Chapter 5

Experimental Determination of Image Placement Errors

5.1 Introduction

Reticle Non-flatness in EUV Lithography results in Image Placement Error. The specifications for IPE get tighter with each successive technology node. In order to achieve the wafer IPE from reticle non-flatness, the P-V as-chucked reticle non-flatness should be 30 nm or better as recommended by the ITRS [56] for 2014 production. Current state of the art EUV substrate flatness is $\sim$90 nm P-V [58] for each reticle surface. In order to improve substrate flatness, EUV substrate vendors employ aggressive polishing techniques. These polishing techniques generate substrate defects, which typically require additional cleaning steps during substrate manufacture to remove them. Substrate defects can severely affect device performance. As a result, flatter substrates are more expensive and require more time to fabricate. In order to relax substrate flatness specifications, researchers have proposed the use of flatness compensation schemes. Flatness compensation [59] is a method of applying appropriate pattern offsets during e-beam writing to correct for placement errors due to mask non-flatness. With a viable flatness compensation scheme, the reticle flatness specifications can be greatly relaxed.
EUV reticles are clamped and flattened in EUV tools using electrostatic chucks. An electrostatic chuck works on the principle of coulombic attraction. The chuck consists of electrodes and a dielectric on which the reticle backside is made to contact. Increasing clamping voltage charges the electrode and the reticle backside creating a capacitor system. The clamping force [60] is given in equation 5.1, and shown here for convenience can be written as,

\[ F = \frac{A\epsilon_0\epsilon_r^2V^2}{2(d + \epsilon_r g)^2} \]  

(5.1)

where, \( V \) is the applied across the electrodes separated by a dielectric of thickness \( d \), \( \epsilon_0 \) is the permittivity of vacuum, \( \epsilon_r \) is the dielectric constant of the material, \( A \) is the electrode area and \( g \) is the air gap between the back side of the mask and the dielectric.

Typically, electrostatic chucking of non-flat EUV reticles result in two separate components of IPE namely,

1. IPD (In-Plane Distortion)
2. OPD (Out of Plane Distortion)

IPD occurs because the reticle is not written on a chuck that matches the scanner. The OPD is due to the front side height variations and the angle of incidence of the incoming light. As the clamping pressure increases, the bow or curvature induced by the thin film deposition gets flattened. This flattening results in surface distortion on the reticle which creates the IPD error. Further increasing clamping force transfers the low order flatness of the reticle backside to the front side. As a result the as-chucked top surface of the reticle resembles the thickness variation of the EUV mask. This thickness variation results in the OPD error due to the non-telecentric illumination of the reticle as illustrated in Figure 5.1. The objective of this work is to characterize reticle clamp on the EUV ADT using reticles with different flatnesses.
Figure 5.1: Illustration of IPE from IPD and OPD due to electrostatic chucking of non-flat reticle on the EUV ADT.

5.2 Experiment Setup

A set of reticles were fabricated for characterizing IPE on the ADT [61]. The reticles were designed with an array of special wafer alignment marks called the ASML XPA IP fiducials which can be used by the ADT to measure IPE and overlay. These reticles were fabricated on substrates with different flatness specifications. The experiments done with these reticles were subdivided into two separate sections detailed below.

5.2.1 Experiments - Clamping Repeatability

The first set of experiments involved exposing a flat rotatable reticle on the ADT in order to establish a baseline for tool contribution to IPE. The layout of the reticle along with the front and backside flatness and the thickness variation is shown in Figure 5.2.

The flatness was measured by a specially designed interferometer that holds the substrate vertically to minimize any effects from gravity (Zygo Phase Shifting
Figure 5.2: Thickness variation and layout of the flat rotatable reticle used for the clamp repeatability study.

Interferometer). The thickness variation is the difference between the front side and the back side flatness of the EUV blank. This reticle was patterned with rotatable reticle alignment marks so that the reticle can be imaged in 4 orientations 0, 90, 180 and 270 degrees. In addition, special wafer alignment marks were also patterned so that the ADT could perform IPE metrology on a printed wafer. The rotatable design can help separate errors from chuck and reticle non-flatness. For example, any error arising from chuck non-flatness will remain constant as the reticle is imaged in different orientation, while errors arising from reticle thickness variation will rotate along with the reticle. This provides a quick qualitative method of identifying errors from chuck non-flatness and reticle non-flatness. Using the interferometer flatness data for the reticle, a model was developed that maps the flatness to IPE by applying the equations shown in Figure 5.1. Figure 5.3 shows the predicted errors for the 0, 90, 180, 270 degree orientations of the reticle. As seen from Figure 5.3, IPE\textsubscript{TOTAL} is negligible with a max error vector of 1.4 nm y-error. The 3\textsigma predicted variation in IPE\textsubscript{TOTAL} between the various orientations is 0.9 nm (based on 0-90, 0-180, 0-270 differences).

Figure 5.4 shows the measured errors from exposing the reticle on the ADT. The error signature remained quite similar between the different orientations as expected. The center of the vector plot for each orientation has a pattern that is characteristic of a particle signature. This is a particle that was present on the chuck over which the reticle was clamped down. Apart from adding to the z-height
variation, the presence of a particle distorts the reticle. This results in a larger $IPE_{\text{TOTAL}}$ contribution form the areas in proximity to the particle. The max x and y errors are 11 nm, irrespective of reticle orientation. The $3\sigma$ variation in $IPE_{\text{TOTAL}}$ is 1.8 nm between orientations. This is the tool chucking repeatability. This repeatability number accounts for differences in tool state between exposure, the z-height variation between orientation, measurement repeatability error etc. The average $3\sigma$ repeatability tool signature is just the RSS of the measured data minus the predicted or $1.8^2 - 0.9^2 = 1.5$ nm. The repeatability ($3\sigma = 1.5$ nm) is within the noise limit of the measurement method.

Another wafer was exposed using the flat rotatable reticle post chuck cleaning.
This shows that the errors at the reticle center do not show any particle signature. Since the error contribution from non-flatness is negligible compared to the tool signature, this flat rotatable reticle exposure was used to establish a noise floor for IPE from the EUV ADT. The $3\sigma$ vector error post chuck clean is 3.4 nm. The maximum x and y errors have dropped from $\sim 11$ nm to 6.9 nm in x and 4.8 nm in y. The figure 5.5 shows the vector plot post chuck clean. This error signature which is primarily from the tool (no reticle flatness contribution) is the tool error signature.

Figure 5.5: Measured errors at 0 degree using the flat rotatable reticle post chuck clean. Absence of particle signature at reticle center confirms that the chuck cleaning was effective.

5.2.2 Experiment - Clamping Pressure Study

A second series of experiments was designed to characterize the electrostatic chuck (or reticle clamp) on the ADT and to compare these results to the FE model. The reticle (reticle A) and the flatness measurements are shown in figure 5.6. This reticle greatly exceeded the SEMI P-37 guidelines for flatness and bow. The reticle was clamped on the reticle chuck using the ADT in a non-standard configuration, different voltages could be applied to the clamp to change the holding pressure to the reticle. Special measures were taken to ensure that this was a safe operation for both the tool and the reticle. The clamping pressure to voltage relationship
is characteristic of the chuck design. The pressure depends on the electrode area, dielectric material, electrode geometry and thickness of the dielectric.

![Figure 5.6: Thickness variation and layout of reticle A used for the clamping pressure study.](image)

5.2.2.1 Clamping Pressure Study - Finite Element Modeling

In order to verify the chucking characteristics of the clamp, a Finite Element (FE) Model, using ANSYS® software, was developed at the University of Wisconsin to predict the as-chucked flatness of the non-flat reticle using a flat, rigid electrostatic chuck. The results from the FE model were then compared to the experimental results from the ADT.

The FE model can simulate the as-chucked reticle and chuck flatness and reticle surface distortion. This allows the calculation of wafer IPE from the FE modeling. The chuck used in the model was made to adhere to SEMI P40 standards that specify the chuck flatness, clamping pressure and bending stiffness. The flatness of the chuck is better than 30 nm P-V over the entire chuck surface. The bending stiffness of the chuck cross-section is 300,000N-m which is effectively a rigid body compared to the stiffness of the ULE substrate used in the reticle. The quarter inch thick ULE substrate has a bending stiffness of 392 N-m. For any given geometry, the bending stiffness [62] can be calculated from the material properties like elastic modulus and Poisson’s ratio using the formula,

\[
\frac{Eh^3}{12(1-\nu^2)}
\]  

(5.2)
where, $E$ is the elastic modulus, $h$ is the thickness of the cross-section, and $\nu$ is the Poisson's ratio of the material. For ULE glass, the elastic modulus is 67 GPa and Poisson's ratio is 0.17. The thickness of the reticle $h$ is 6.35 mm. The friction co-efficient between the reticle backside and the chuck surface was taken to be 0.2. Since the chuck flatness is much better than the reticle flatness (30 nm compared to 1094 nm) and because the exact shape of the reticle chuck on the ADT is not known, the chuck was approximated to be completely flat and infinitely stiff to make the modeling simpler. To input the non-flatness of the reticle into the FE structural models, the interferometric data were fitted with an $8 \times 8$ matrix of Legendre polynomials as shown in figure 5.7. Legendre polynomials have been identified as effective means to represent experimentally measured EUVL substrate surface shapes. For the chuck used in the ADT, the voltage to clamping pressure curve can be plotted using the force equation given previously. Using this characteristic voltage-pressure conversion, appropriate clamping pressures were chosen for the FE modeling, consistent with the voltages that were used on the reticle chuck during the experiments (section 5.2.2.2). Figure 5.8 is a plot of as-chucked reticle flatness for 300Pa, 1 kPa and 2 kPa clamping pressures simulated using the FE model described previously.

5.2.2.2 Reticle A - Overlay results between clamping pressures

A wafer was exposed on the ADT with the Non-flat reticle clamped at 2 different clamping pressures to identify the amount of image placement error transferred to the wafer from the flatness change on the reticle. The first exposure was done at the ADT normal clamping pressure (15 kPa) and a second exposure was done at a lower clamping pressure (2 kPa). The clamping pressures were chosen such that the as-chucked average flatness difference was 200 nm P-V. Figure 5.9(a) is a vector plot of the residual overlay error between the two exposures of reticle A. The residual or non-correctable error is calculated from raw error by removing translation, magnification and rotation terms which are scanner correctable and
Figure 5.7: $8 \times 8$ Legendre polynomial fit to the front side and back side flatness of reticle A showing large bow on both surfaces from multilayer deposition. The blank thickness variation over the full area is 336 nm.

Figure 5.8: As-chucked reticle flatness of reticle A based on a flat rigid chuck at different clamping pressures. Hence do not contribute to final wafer overlay in a production environment. The $3\sigma$ overlay vector is 2.7 nm. Figure 5.9(b) is a vector plot of predicted overlay error from Finite Element Modeling for reticle clamped at 15 kPa and 2 kPa. The $3\sigma$ vector magnitude is 0.5 nm which is consistent with the small changes in the flatness at these clamping pressures, as predicted by the FE models. This is very different than what is measured on the ADT. The as-chucked reticle flatness was
then measured along the reticle in the Y-direction at 2 x-positions located just outside of the image field as shown in Figure 5.6.

![ADT Overlay](image1.png) ![UW FEM Prediction](image2.png)

Max X: 1.5nm Max Y: 5.3nm
3σ: 2.7nm

Max X: 0.6nm Max Y: 0.8nm
3σ: 0.5nm

(a) (b)

**Figure 5.9:** Overlay error between exposures of the Non-Flat reticle at 15 kPa and 2 kPa (a) ADT measurement (b) FE Model (Flat Chuck).

Figure 5.10 is a plot of the as-chucked reticle flatness as a function of clamping pressure for reticle A. Each line in the plot is the average z-height that was measured by the ADT on each side of the reticle as shown in Figure 5.6. Throughout the rest of this paper the word flatness will be defined as the range of each curve at a particular pressure. The flatness for 2 kPa is indicated in Figure 5.10 as an example of this definition. As the clamping pressure is deceased from the nominal value, the flatness of the reticle should increase until the reticle drops from the clamp. The reticle drops from the electrostatic clamp when the voltage on the electrodes generates a clamping pressure that is less than the weight of the reticle. For the reticle A, at 12 kPa clamping pressure, the as-chucked reticle flatness was 100 nm P-V.

It is evident from the FE modeling (Figure 5.8 that at clamping pressure above 1 kPa, the reticle flatness does not change significantly. Figure 5.11 is a plot of
Figure 5.10: Clamping pressure variation induced change in as-chucked reticle height, measured on the EUV ADT.

"flatness" from the FE model (using a flat chuck). This flatness is the same definition used earlier and the average flatness is taken from the modeled flatness data at the same sites used by the ADT as shown in Figure 5.6. The trend seen in Figure 5.11, where the flatness does not change with clamping pressures above 1 kPa is captured in the average flatness plots as well. This is in stark contrast to the flatness curves measured on the ADT in Figure 5.10 showing significant flatness change from 2 kPa to 12 kPa. It is also noteworthy that contact gap between the reticle and the chuck is also negligible above 1 kPa. This implies that conformal clamping of the reticle to the chuck occurs at $\sim$1 kPa. Due to this conformal clamping, the as-chucked reticle topography resembles the thickness variation of the blank.

5.2.2.3 FE Modeling of Non-flat Chucks

A second FEM was developed to simulate the chucking of reticle A to a non-flat chuck. The perfectly flat chuck was replaced with a uniformly concave chuck and uniformly convex chucks having 80 nm P-V non-flatness. Since the reticle backside has a convex shape, the separation between the reticle and chuck prior to clamping is increased by 80 nm. Similarly, a convex shaped chuck would reduce the gap between the reticle back side and the chuck prior to clamping. This model was developed to see if this change in chuck non-flatness has an effect on the flattening
Figure 5.11: Average flatness at 2 kPa, 1 kPa and 300Pa for reticle A from the FE model.

response of the chuck. Figure 5.12 is a summary of the reticle flatness at different clamping pressures (200 Pa and 15 kPa) using a concave chuck and convex chuck models.

Figure 5.12: Reticle flatness predicted by a FEM at different clamping pressure for a perfectly concave and perfectly convex shaped chucks with 80 nm P-V non-flatness at the chuck center.

Figure 5.13 summarizes the results from reticle A and the FEM predictions.
The figure shows the P-V flatness described earlier against clamping pressure (from 200Pa to ~12 kPa) for reticle A from FEM modeling and ADT measurements. At the highest pressures, the flatness change gets smaller for reticle A indicating that the reticle is almost fully clamped at 12 kPa. The normal operating pressure for the ADT is 15 kPa. The measured reticle flatness from the ADT shows that flatness gets better at clamping pressures smaller than ~1.5 kPa. However, this is an artifact of the measurement technique. At pressures below 1.5 kPa, it is believed that the reticle is not fully clamped at all 4 corners resulting in a large tilt along y-direction. However, during the measurements, any y-tilt present in the reticle is removed resulting in the curves looking flatter.

**Figure 5.13: Summary of the reticle flatness data for reticle A from ADT measurements and FE modeling for flat, 80 nm concave and 80 nm convex chucks.**

When the measured flatness is compared to the modeled values, there is a large difference between the P-V flatness curves at all clamping pressures. The FE models predict that the reticle attains the final clamped shape irrespective of clamp shape at 1 kPa. An interesting observation from figure 5.13 is that the
final FEM predicted flatness for the 80 nm convex chuck is closer to the measured ADT values at higher clamping pressures. This indicates that the ADT reticle clamp may have a convex shape rather than the “flat” chuck that is typically used in most FE models.

5.2.2.4 Clamping pressure study of reticles from different suppliers

Reticles with different flatness characteristics were clamped on the ADT chuck. The results of these flatness measurements are summarized in Figure 5.14, which shows the P-V non-flatness for different clamping pressures. Each reticle in the plot is identified by supplier A, B, or C and the corresponding backside flatness and thickness of the reticles as measured by a stand alone interferometer are also indicated. It is seen that the slopes of the flatness curves are different and depends on the reticle blank supplier and thickness measurements. Each reticle blank supplier has a different flattening characteristic and none of them match the FEM predictions except at the end point where the flatness no longer changes.

![Figure 5.14: Summary of the reticle flatness measurements for different reticles from multiple vendors. Reticles were selected such that the flatness specifications were different. Some of the differences in the flattening behavior can be attributed to the differences in the thin film stack on these reticles.](image)

This gradual flattening behavior is not seen in the FEM predictions. Irrespective of the chuck shape, the FE models predict that the reticles attain final
clamped state around 1 kPa. These results are significant because it was not expected that anything other than blank flatness would be needed in the FE model. All of the reticles approach constant flatness and thus achieves conformal clamping before reaching the ADT normal operating pressure of 15 kPa.

It is also possible that a particle is trapped under the reticle outside of the printing area. The presence of a large particle under the reticle would change the clamping pressure response of the chuck around the particle. This would also be consistent with the large vectors along the right hand edge of figure 5.9.

5.3 Conclusions and Future Directions

The experiments on a rotatable reticle were performed on the EUV ADT to establish a baseline tool IPE signature. With a rotatable reticle design, a particle on the reticle chuck was easily identified. The measured repeatability (3σ = 1.5 nm) is within the noise limit of the measurement method.

A clamp pressure study was done with the ADT in a non-standard configurations and with reticles that do not comply with SEMI P-37 guidelines. The University of Wisconsin developed a FEM to study reticles and clamping with flat and non-flat clamps and reticles. When ADT measurement results were compared to the model predictions, they did not match. One conclusion could be that the model is somehow incomplete or that there is something outside of the printed field that distorts the reticle as it is being clamped. The FE model developed for this work includes the effect of gravity as load acting on the reticle. However, the change in initial shape of the reticle due to the presence of gravity is not captured in the FE model. The initial shape of the reticle can change as much as 1.5 μm due to the presence of gravity. This could also contribute to the exaggerated difference between the measured and predicted flatness curves. As future work, the effect of gravity on initial substrate shape needs to be investigated. In addition, the model assumes infinite stiffness. These and other parameters need to be examined more
closely.

Investigating other reticles with different flatness show that all reticles tested reach constant flatness. Thus, conformal clamping is achieved before reaching the ADT normal operating pressure of 15 kPa.
Chapter 6

Rotatable Transmission Image Sensor Reticle

6.1 Introduction

In the last chapter, a set of experiments designed to look at the clamping characteristics of the ASML EUV ADT reticle clamp were discussed. However, the reticle was designed with an array image placement fiducials that can be read out on the wafer. The flatness curves measured on the tool, which directly relate to the $IPE_{OPD}$, were measured along two "rails" or "stripes" outside the quality area of the reticle. Although this can provide a rough estimate of the change in flatness, it does not enable flatness measurements over the entire reticle area. The flatness of the reticle over the quality area in particular is the most important factor when determining the wafer IPE. In order to better understand as-chucked reticle flatness over the entire reticle area, a reticle with a novel image placement fiducial was designed to cover the entire area of the reticle. The novel IP fiducial called the Transmission Image Sensor mark can provide information on the x,y and z distortions of the fiducial on the wafer. The wafer distortions can be easily translated to reticle plane distortions which in turn provides a method to separate $IPE_{OPD}$ and $IPE_{IPD}$ contribution to the wafer IPE.
6.2 Transmission Image Sensor as IP Fiducial

Transmission image sensor (TIS) consists of a photodiode on the wafer stage, that can record incident light intensity. Photodiodes are light sensitive diodes that can convert light into either current or voltage depending on the diode circuit design. The detailed operation of a photodiode is illustrated elsewhere [63]. TIS fiducial consists of a set of horizontal and vertical gratings of varying pitch and sizes. The TIS fiducial also contains a large open area that is used for dose calibration. For the purpose of the image placement error study, a reticle was designed with a set of TIS fiducials distributed throughout the reticle quality area. The EUV light incident on the TIS fiducial gets recorded by the photodiode detector present on the wafer stage. The diode records a 3-D aerial image of the TIS fiducial by moving the wafer stage. Using this 3-D aerial image, the centroid of the aerial image is identified to be the actual location of the center of the pattern on the wafer. The pattern location in wafer coordinates can be converted to reticle coordinates based on the lens design of the projection optics. The difference between the nominal pattern location and the observed centroid of the pattern gives an estimate of the image placement error. The x,y location of the mark on the wafer and reticle are simply related by the demagnification of the projection optics. For example a x,y mark location of 5 mm, 5 mm on the wafer is 20 mm, 20 mm on the reticle for a 4x projection optics. The conversion of the wafer de-focus i.e. z-offset of the pattern to the reticle de-focus is more involved. The wafer and reticle de-focus is related to the longitudinal magnification of the projection optics. Detailed treatment of the longitudinal magnification is given in [64]. A summary of the derivation of longitudinal magnification is provided below for reference. The longitudinal magnification is defined as the ratio of the change in the position of the image to the change in position of the object, where the distances are measured from the lens principal plane. Assuming a thin lens and the object distance of s and image
distance of \( s' \), the lens makers formula for a lens of focal length \( l \) is given by,

\[
\frac{1}{f} = \frac{1}{s} + \frac{1}{s'} \tag{6.1}
\]

The longitudinal magnification \( m_l \) is given by,

\[
m_l = \frac{\delta s'}{\delta s} \tag{6.2}
\]

Solving for \( s' \) from equation 6.1, we can calculate that the longitudinal magnification is given by,

\[
m_l = -\frac{f^2}{(s - f)^2} \tag{6.3}
\]

The lateral magnification of a lens is \( s'/s \) or \( f/(f - s) \). Hence, longitudinal magnification \( m_l = -m^2 \).

For a projection optics with a demagnification of 4, the wafer and the reticle defocus is is related by a factor of \(-4^2\) i.e. \( m_l = -16 \).

The ability to obtain the image placement error and the reticle defocus for each TIS fiducial helps to separate the two components of wafer IPE, IPE_{IPD} and IPE_{OPD}. While the \( x,y \) displacements results from both in-plane and out of plane distortions, the \( z \)-errors on the wafer/reticle only contribute to IPE_{OPD}. As a result, the \( z \)-errors or reticle defocus can be used to calculate IPE_{OPD}. The IPE_{TOTAL} given by the \( x,y \) offsets can then be used to calculate the IPE_{IPD} as

\[
IPE_{IPD} = IPE_{TOTAL} - IPE_{OPD} \tag{6.4}
\]

### 6.3 TIS Rotatable Reticle - Pattern Layout

The layout of the TIS rotatable reticle is shown in figure 6.1. The pattern layout consists of an array of TIS fiducials. The fiducials are placed such that the reticle can be imaged in 4 orientations. The reticle frame was also made rotatable such that the ADT can align the reticle to the optics and wafer stage based on reticle
frame fiducials. In addition to the TIS fiducials, the reticle also included an array of conventional print based IP fiducial called the ASML XPA fiducial. This way, it provides a method for correlating print based and aerial image based IP error measurement methods. As seen from the figure, the pattern layout has an array of 13×9 TIS marks and 9×9 array of XPA marks within the scanner field. The scanner field is defined by the width of the illumination arc on the reticle and the scan length of the arc along the reticle. The scanner field is typically 132 mm in y-direction and 104 mm in x-direction.

The principle of rotatable reticles was explained in chapter 5. The layout of the TIS fiducials is such that at each orientation, the TIS fiducial array is at the exact same position with respect to the rest of the EUV tool. For all intents and purposes, the pattern layout is independent of reticle orientation. In order to achieve a symmetric pattern layout, a rotationally symmetric array of TIS fiducials was designed with as unit pattern cell consisting of 0, 90, 180 and 270

---

Figure 6.1: Figure shows the pattern layout of the TIS rotatable reticle with a rotatable frame. The TIS fiducials are placed in 4 different orientations to enable reticle imaging in different orientations on the ADT. The reticle also has an array of XPA marks to enable print based IPE measurement.
degree orientation TIS fiducials. The unit cell with the 4 TIS fiducials is shown in figure 6.1. The TIS fiducials have to be placed in 4 different due to the fact that the wafer stage TIS detector/sensor can record aerial images of the TIS pattern in one orientation only ($0^\circ$). However, within the unit cell, a single XPA fiducial is also present. Although the XPA detector can detect the mark only in the $0^\circ$ orientation, the XPA is a print based fiducial. This enables another degree of freedom during readout by rotating the wafer prior to loading on the wafer stage, such that the XPA marks irrespective of the orientation it was printed can be read out the right way.

### 6.4 Blank Flatness Measurement

The substrate used for fabricating the blank for the TIS Rotatable reticle is specified to have $\sim250$ nm flatness i.e. optical grade flatness on each surface of the substrate. The substrate flatness as measured by the Zygo phase shifting interferometer is shown in figure 6.2.

![Figure 6.2](image)

**Figure 6.2:** Figure shows the back side flatness and the thickness variation of the substrate used for fabricating the TIS Rotatable reticle. The substrate was polished to optical grade flatness specification ($\sim250$ nm).
This substrate was then used to fabricate blanks by multi-layer deposition. The final blank flatness post thin film deposition (Mo/Si multi-layers, capping layer, buffer layer, absorber, back side conducting layer) is shown in figure 6.3. As seen from the figure, the blank flatness is quite large and as a result, the non-flatness contribution to image placement error, primarily from thickness variation will be large (before removing correctable errors).

Figure 6.3: Figure shows the back side flatness and the thickness variation of the blank used for fabricating the TIS Rotatable reticle. The contour plots show the P-V flatness along with bow (power) and rms flatness. The flatness shown is for the substrate area of $140 \times 140 \text{ mm}^2$.

6.4.1 Predicted IPE from Flatness Measurements

Based on the backside flatness and thickness variation, a simple analytical model described in sections 3.6.2 and 3.6.3 can be used to calculate the image placement errors from reticle non-flatness for conformal reticle clamping. Shown in figure 6.4 is the predicted image placement errors based on the measured flatness.

However, this calculation for image placement error assumes that the mask writer can write the patterns with no placement errors. Typically, the mask writers have an imperfect wafer grid and beam deflector calibrations and results in image placement error during e-beam writing. After mask fabrication, an LMS IPRO tool was used to measure the errors in the positioning of the TIS fiducials during
Figure 6.4: Figure shows the predicted image placement error based on flatness measurements for the TIS Rotatable reticle. The IPE calculation were done using a simple analytical model.
mask write at the mask shop. The LMS IPRO tool measures a specifically designed ”+” pattern at the center of each TIS fiducial. Hence the predicted errors should account for mask writer image placement errors along with the errors from reticle non-flatness. The total IPE including the mask writer contribution is shown in figure 6.5. It can also be seen from figure 6.5 that the effect of this mask writer contribution to the total predicted IPE is quite negligible.

Figure 6.5: Figure shows the pattern placement error from the mask writer. The effect of mask writer error on the total IPE is negligible.

The TIS Rotatable reticle was designed with a rotatable frame that would enable the reticle to be imaged in 4 orientations - 0, 90, 180 and 270 degrees. Since the reticle flatness as seen by the EUV tool during exposure depends on the orientation of the reticle on the clamp, the predicted IPE signature will be different for each orientation. Figure 6.6 shows the predicted image placement error for 4 different orientation of the TIS Rotatable reticle. As seen from the figure, the non-flatness contribution to IPE is not rotationally symmetric. As a result, there are error signature differences between orientations, assuming the reticle is conformally clamped at each orientation. These predicted errors will then be compared to measured errors from exposing the TIS Rotatable reticle to characterize the clamping characteristics of the EUV ADT reticle chuck.
6.5 Experiment Setup

The first set of experiments were designed to calibrate the measurement method. This calibration involves identifying the measurement repeatability, accuracy and
scan direction and step size dependence of measured errors. TIS measurements provide x,y and z offsets of the fiducial on the wafer. Since the TIS measurements are aerial image based, the accuracy of the measurements in x,y is better than measurement accuracy along z direction. This can be directly determined from the differences in the aerial image intensity along x,y direction and z direction. There is a much smaller sensitivity to aerial image intensity changes along z direction resulting in a much larger error in the z measurement.

Figure 6.7: Figure shows accuracy of the TIS measurements in x and y directions. The cumulative probability plots show that the y-direction accuracy is better than x-direction accuracy.

First experiment was to identify the repeatability/accuracy of the TIS measurement. A set of 100 measurements were done on the same fiducial successively and repeated over 5 fiducials at different points in the reticle. Figure 6.7 shows the setup and summary of the accuracy experiment. The plots are cumulative probability plots of accuracy in x and y direction. As seen from the figure, the y-direction accuracy is much larger than the x-direction accuracy. However, the accuracy numbers are good enough for the purpose of identifying reticle non-
flatness contribution to IPE. The max x and y predicted errors are about 6 nm for the blank used to fabricate this reticle.

The second experiment was designed to test the scan direction dependence of the TIS measurement. The experiment was performed by first scanning a column of TIS marks from the top to bottom (N scan) and then from bottom to top (P scan) as shown in figure 6.8. Each TIS mark with a scan was only measured once, but the sequence of P and N scans were repeated a total of 10 times (5+5). After the vertical scan dependence was measured, the same experiment was performed by scanning a row of horizontal TIS marks as shown in figure 6.9. It can be seen from the figures that the vertical scans have a larger y - difference and the horizontal scans have a larger x difference between scans. This is to be expected since the vertical scans, the wafer stage motion is in y - direction with minimal movement along x and vice versa for horizontal scans. The large scan direction dependence occurs when the wafer stage motion is present. Hence, a scan dependent difference of $\sim 1.5$ nm is measured for each scan direction.

![Figure 6.8: Figure shows vertical scan direction dependence of $\text{IPE}_x$ and $\text{IPE}_y$ errors.](image)
The third experiment was designed to calculate the repeatability of the z measurement. Since the z measurement is generally less accurate than x and y, the complete array of TIS marks (0°) was measured. Each mark was measured 10 times before moving to the next mark. The marks were measured by starting at the top left corner of the reticle and scanning in the +x direction and then moving to the next row down. An array of $13 \times 9$ TIS marks were measured 10 times each, making a total of 1170 measurements. The $3\sigma$ z values are shown in figure 6.10. The $3\sigma$ values are extremely good and mostly smaller than 2 nm for a large fraction of TIS fiducials.

With these experiments, it can be clearly seen that the TIS measurement method has the required accuracy and repeatability to be used for investigating reticle non-flatness induced IPE.

Finally, a set of exposures were done to correlate the image placement error measurements between the TIS fiducials and print based XPA fiducials. The XPA marks were printed on a wafer coated with 150 nm of Rohm and Haas XP4502J.
Figure 6.10: Figure shows the $3\sigma$ z values for an array of $13 \times 9$ array of TIS fiducials based on 10 repeats of each fiducial.

resist and exposed with a dose of $5\text{mJ/cm}^2$. The dose sensitivity of the XPA marks is quite small due to the large size of the features in the mark itself. The exposure was followed by a bake step and the resist was developed. This exposed wafer was
then readout on the EUV ADT using ASML’s standard readout method. Figure 6.11 is shows IPE\textsubscript{TOTAL} measured from both print based (XPA) and aerial image based (TIS) measurements.

![TIS (13x9)](image1)

![XPA (9x9)](image2)

Figure 6.11: Comparison of image placement error measurements from XPA and TIS marks methods. The max vectors in the XPA measurements are larger as expected due to an additional readout step using the ADT wafer stage. The shaded portions in the TIS measurements are the additional rows of TIS marks and are not present in the XPA results.

The TIS mark layout on the reticle covers a larger area (∼90 mm × 130 mm) than the XPA array (∼90 mm × 90 mm). From the values of the maximum vectors in x and y directions, the XPA measurements has larger error signature compared to the TIS based measurement, even with the smaller area. The XPA based measurement have errors from wafer stage motion both during exposure and readout of the marks. During the TIS based measurements, the wafer stage moves during measurement. There is no exposure step since the TIS method is aerial image based. However, the error signatures in figure 6.11 are quite similar.
6.6 Separating IPE\textsubscript{IPD} and IPE\textsubscript{OPD}

6.6.1 TIS Measurement - Measurement Sequence

Since the TIS sensor can detect x, y and z positions of the TIS fiducial, it is possible to separate out the various contributions to image placement error using an analytical model approach. An array of 13×9 TIS fiducials were measured on the EUV ADT using the TIS sensor on the wafer stage. The marks were measured 5 times and averaged to calculate the image placement errors. The measurement sequence is shown in figure 6.12. After some initial calibration studies, the a measurement sequence that involved measuring the entire array multiple times instead of multiple measurements of each mark in the array was adopted to reduce effects of TIS sensor temperature effects. When a TIS mark is measured, a photo current is generated in the diode detector. A finite resistance across the diode structure (internal) can lead to I\textsuperscript{2}R losses leading to temperature changes. This can be reduced by introducing a short break between measurements. Along with the I\textsuperscript{2}R losses, the wafer stage temperature profile also influences the photodiode temperature. If the wafer stage is ”parked” at the same position for a long duration during multiple TIS measurements, the photodiode is more likely to equilibrate to the the temperature of position it is ”parked” in. A work around to this is to measure the entire array of TIS marks multiple times as shown in figure 6.12.

As an example of the scan sequence dependence, figure 6.13 shows the change in focus offset for four different scan sequences. During all of these measurements, each TIS mark was measured 10 times before moving the stage to measure the next TIS mark. As a result, large temperature effects seem to affect the measured focal values. These large changes in focal values between the left to right and right to left scan sequences indicate that the measured values are affected by the scan direction. However, with the scan sequence described in figure 6.12, the difference between the left to right and the right to left scans are almost non-existent.

Figure 6.15 shows the image placement error measured on the wafer stage
Figure 6.12: TIS measurement sequence for measuring aerial image based IPE.

TIS sensor using the scan sequence described in figure 6.12. The measurements show $\text{IPE}_{\text{TOTAL}}$ for all 4 reticle orientations. Figure 6.16 shows the corresponding tool distortion measurement using a flat reticle. The distortion measurement is print based i.e. using ASML XPA fiducials. The TIS measurement and the tool distortion measurements have the same magnitude of errors and almost the same error signature. It must be noted that the distortion plot is reticle pattern side down and the TIS measurements are presented as pattern side up.

As a result from figures 6.15 and 6.16, it is quite clearly seen that the reticle non-flatness differences does not directly translate to error signature differences. However, figure 6.17 shows that the measured reticle flatness offset (from TIS measurement) over the entire reticle quality area is $\sim$1300 nm. This $\Delta z$ values is consistent irrespective of orientation. 1300 nm of reticle non-flatness would result in $1300/40=32.5$ nm of image placement error before removing correctable errors.
Figure 6.13: Focal offset based from TIS measurement shows large differences between scan sequences. Each TIS mark is measured 10 times before moving to the next mark.

Figure 6.14: Focal offset between scan sequences show very small differences indicating better control of external factors (like temperature) affecting the measurement results. Each TIS mark is only measured once and the entire array is measured 5 times.

From these figures, it is clear that a large portion of the measured focal offset results from external contributions and not necessarily reticle flatness. These could be residual focal errors from the lens setup, temperature profile of the wafer stage.
Figure 6.15: IPE measurements from the TIS reticle following the scan sequence described in figure 6.12

Figure 6.16: ASML tool NCE or distortion measurement. The error magnitudes and signatures are very similar to the TIS measurements in figure 6.15.

etc. As a result, an average $\Delta z$ value is calculated for each position across the reticle by averaging the 13 rows for TIS marks. Figure 6.18 is a plot of average $\Delta z$ along with the lens setup error. All values are reticle pattern side up.

The large difference between the lens setup errors and the measured average $\Delta z$ values along with the small non-flatness effect on the measured IPE indicate some form of systematic contribution to the $\Delta z$ measurement. A corrected $\Delta z_c$ is calculated by removing the average $\Delta z$ values from each row of measurement. Figure 6.19 shows that the $\Delta z_c$ range is $\sim$200 nm compared to the 1300 nm range
Figure 6.17: Large $\Delta z$ values measured for all orientations of the TIS Rotatable reticle. The plots from left to right are for 0, 90, 180 and 270 degree orientations.

Figure 6.18: Average $\Delta z$ values and lens setup errors from the same time frame as the TIS measurements before correction.

Figure 6.20 is a vector plot of the image placement error resulting from $\Delta z_c$. The errors are quite small compared to the IPE$_{TOTAL}$ values from figure 6.15.

Since the $x,y,z$ measurements have enabled calculating the total and OPD contribution, the IPD contribution to IPE is given by,

$$IPE_{IPD} = IPE_{TOTAL} - IPE_{OPD}$$

Figure 6.21 shows the IPE$_{IPD}$ resulting from clamping the TIS Rotatable reticle
Figure 6.19: Corrected $\Delta z$ values after removing average $\Delta z$ from each row of measurements. The plots from left to right are for 0, 90, 180 and 270 degree orientations.

Figure 6.20: Non correctable error from $\Delta z_c$ calculations. As seen from the $\Delta z_c$ values, the errors are quite small compared to predicted OPD contribution. The plots from left to right are for 0, 90, 180 and 270 degree orientations.

on the EUV ADT. It must be noted here that the IPE$_{IPD}$ also includes the tool distortion contribution which requires very accurate measurements to separate out. The print based distortion plot shown in figure 6.16 is measured using a flatter reticle. Nonetheless, there is always a reticle component to the measured distortion which needs to be subtracted out of the calculated IPE$_{IPD}$. For our purposes here, the IPD contribution includes tool distortion.

The use of a TIS fiducial method as detailed in the previous section is capable of identifying the IPD and OPD contribution to image placement error. However, to accurately calculate the IPD contribution a more complete estimation of the tool distortion is required. This could be possible by using a number of reticles of different shapes and averaging the measured distortion signature from each of these reticles. Assuming the reticle shapes are not correlated, the average
A second set of experiments were conducted to identify the long term repeatability of reticle clamping using the TIS Rotatable reticle. For the purposes of flatness compensation, the long term repeatability is a very important characteristic of the reticle clamp. In order to test long term clamping repeatability, TIS measurements were repeated over a period of almost two month. Additionally, short term repeatability was also estimated by measuring the TIS Rotatable reticle multiple times in a short time span.

Figure 6.22 shows the $3\sigma$ x and y errors for a number of measurements of the TIS Rotatable reticle. While the short term repeatability is less than 1 nm $3\sigma$, the long term repeatability over a 2 month time period is much larger at 3.0 nm and 6.5 nm in x and y directions respectively. Also shown in figure 6.22 is the variation in tool distortion signature (NCE) over the same period of time. It can be seen that the change in distortion is much smaller than the change in error signature from the TIS measurements.

### 6.7 Summary and analysis of Results

Although the TIS measurements provide a method for separating the IPD and OPD contributions to total wafer IPE, a more thorough analysis of the lens distortion and wafer stage interferometer mirror map is required to completely separate
Figure 6.22: Short term and long term repeatability of reticle clamping based on multiple TIS Rotatable reticle measurements.

the IPD contribution from the tool distortion contribution. A summary of the TIS Rotatable reticle measurements for all 4 orientations of the reticle is shown in figure 6.23. Irrespective of reticle orientation, OPD or the reticle non-flatness contribution is smaller than the IPD contribution. This could be due to the fact that the calculated IPD also contains the tool distortion signature. However, comparing the measured OPD contribution to the predicted OPD values, a clear difference in the magnitude of errors from reticle non-flatness indicates that the reticle chucking may not be conformal. Lack of IPE signature changes between various reticle orientations indicate that the measured error signatures are dominated by the tool distortion contribution with the reticle non-flatness contribution being negligible.

Clamping repeatability which is critical to achieving good overlay and effective implementation of flatness compensation was also measured over a period of 2

<table>
<thead>
<tr>
<th>Run #</th>
<th>Date</th>
<th>Max X (nm)</th>
<th>Max Y (nm)</th>
<th>Vector 3σ</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>11/19/09</td>
<td>4.34</td>
<td>4.31</td>
<td>2.75</td>
</tr>
<tr>
<td>2</td>
<td>11/19/09</td>
<td>4.70</td>
<td>4.01</td>
<td>2.80</td>
</tr>
<tr>
<td>3</td>
<td>11/22/09</td>
<td>4.23</td>
<td>4.25</td>
<td>2.81</td>
</tr>
</tbody>
</table>

Short term 3σ variation in X error: 0.7nm
Short term 3σ variation in Y error: 0.5nm

<table>
<thead>
<tr>
<th>Run #</th>
<th>Date</th>
<th>Max X (nm)</th>
<th>Max Y (nm)</th>
<th>Vector 3σ</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>11/19/09</td>
<td>4.34</td>
<td>4.31</td>
<td>2.75</td>
</tr>
<tr>
<td>2</td>
<td>1/14/10</td>
<td>6.2</td>
<td>7.2</td>
<td>4.22</td>
</tr>
<tr>
<td>3</td>
<td>2/09/10</td>
<td>4.7</td>
<td>8.5</td>
<td>5.27</td>
</tr>
<tr>
<td>4</td>
<td>2/17/10</td>
<td>4.2</td>
<td>9.6</td>
<td>6.19</td>
</tr>
</tbody>
</table>

Long term 3σ variation in X error: 2.8nm
Long term 3σ variation in Y error: 6.8nm

Corresponding change in tool NCE signature
NCE - Long term 3σ variation in X error: 1.9nm
NCE - Long term 3σ variation in Y error: 3.9nm
Figure 6.23: Summary of IPE results for the TIS Rotatable reticle. The plot shows measured and predicted IPD and OPD contributions to wafer IPE.

months. While the short term repeatability is sufficiently good, the long term repeatability error is much larger. Although the changes in the measured IPE values could be attributed to an extent on the change in tool distortion, the much smaller change in measured tool distortion using a flatter reticle indicates that reticle clamping repeatability is reticle shape dependent. Although clamping repeatability seems to limit the effective implementation of flatness compensation a more detailed sensitivity analysis is required to determine the effect of clamping
repeatability on overlay errors.
Chapter 7

Reticle Shape Matching to Reduce Overlay Errors

7.1 Introduction

Product overlay is critical to functional devices and yield in a production environment. Although image placement error affects overlay, it can be shown that with repeatable chucking behavior and stable tool distortion components, good overlay is dependent on the shape of the reticle substrate used for each layer. Reticle shape mismatch induced overlay errors will be introduced and analyzed with an analytical IPE model. Reticle shape matching i.e. selecting reticles with the right substrate shapes for different layers of a product can be a powerful tool for reducing product overlay without implementing reticle flatness compensation schemes. The following sections address the different aspects of substrate shape induced overlay effects. A look ahead study for substrates with tighter flatness specifications has also been discussed with a view on meeting the ITRS overlay budget for production year 2012.
7.2 Population Studies

Typically, a very aggressive polish is required to get to surface flatness specifications of 250 nm and below. It has been shown that such aggressive polishing methods add additional defects to the substrates [59]. In that work two sets of 5 blanks each, with two different flatness specifications, 100 nm and 250 nm were measured for number of defects 60 nm and greater. Figure 7.1 shows that the defect count increases for blanks with tighter flatness specs due to the aggressive polishing methods used to achieve the required flatness. Apart from the added defects, producing a flatter substrate is more expensive and time consuming. As a result of this trade off between defect count, cost and flatness specification, there is a strong effort to try to use substrates with looser flatness specifications.

![Figure 7.1: Increasing defect count as the substrate flatness specifications get tighter.](image)

A current suggested value for substrate flatness according to the SEMI P37 standard is shown in table 7.1. One of the methods proposed to overcome this problem is to use compensation for reticle non-flatness effect during electron beam write of the EUV blank image placement. This however, requires an accurate model to predict the Image Placement Error (IPE) when a non-flat surface held by an electrostatic chuck is exposed in a EUV tool.

To better understand the tolerances of the EUV tools to reticle non-flatness, a set of 10 blanks each from 2 different blank substrate vendors were ordered [58].
<table>
<thead>
<tr>
<th>Specification</th>
<th>Type A</th>
<th>Type B</th>
<th>Compensated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
<td>250 nm</td>
</tr>
<tr>
<td>Back side non-flatness</td>
<td>30 nm</td>
<td>23 nm</td>
<td>250 nm</td>
</tr>
<tr>
<td>Wedge angle</td>
<td>≤ 100 µrad</td>
<td>≤ 100 µrad</td>
<td>≤ 100 µrad</td>
</tr>
</tbody>
</table>

Table 7.1: Flatness requirements for EUV Substrates (with and without flatness compensation)

Vendors were requested to provide 5 substrates each at the ≤100 nm and ≤ 250 nm flatness specifications. The substrates were multi-layer coated and the final front and back surface flatness of these blanks were measured in a Zygo Phase Shifting Interferometer at the SEMATECH Mask Blank Development Center at Albany (shown in appendix B). Figure 7.2 is a plot of the backside non-flatness and thickness variation of the 20 blanks. It can be seen that the flat blanks from Vendor A have a more consistently larger backside non-flatness specification, while the flat blanks from Vendor B have a smaller P-V back side non-flatness. There is also a larger spread for the backside non-flatness number in the set of flat blanks from Vendor B.

Figure B.1 summarizes the bow contribution to the backside non-flatness of the blanks. The blanks from Vendor A seem to have a larger percentage of the total non-flatness resulting from backside bow. As a result, even though the bow values are larger for Vendor A blanks, the final residuals are smaller. Similarly, the Vendor B blanks have a smaller percentage of bow in the backside non-flatness, resulting in a larger residuals.

### 7.3 Population Analysis - IPE Calculation

The flatness measurements of the front and the backside were used to model the IPE from bow and backside flattening and IPE from z-height variation. An analytical model for predicting the IPE when exposing these masks in the ASML EUV Alpha Demo Tool used to predict the stress induced bow flattening. The scanner correctable terms translation, rotation, magnification were then modeled out of the image placement error values to calculate the residuals. Figure 7.4 shows
Figure 7.2: Plot of the front side flatness and thickness variation of EUV blanks from two vendors

the maximum residual vector IPE for all 20 blanks from Vendors A and B. For both vendors, blank numbers 1 - 5 are blanks fabricated from the flat substrates and blank numbers 6 - 10 are blanks fabricated from the non-flat substrates. The residual errors for all flat blanks are much lower than the non-flat blanks. The average max residual error for the 5 flat blanks is from Vendor A is 3 nm, while the average max residual error for the non-flat blanks is 8 nm. Similarly for Vendor B, the average residual error for the flat set is 5 nm while the average max residual for the non-flat set is 10 nm. In general, Vendor A blanks have a larger raw error number (not shown) and smaller residuals for both flat and non-flat blanks, while Vendor B has smaller raw error numbers (not shown) than Vendor A but larger
Figure 7.3: Summary of bow contribution to total flatness for blanks from different vendors. All flatness numbers in nm.

residual errors. In terms of absolute image placement error number, the flat blanks from Vendor A have the best residual error values.

<table>
<thead>
<tr>
<th>Blank #</th>
<th>Vendor A</th>
<th>Vendor B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Backside P-V</td>
<td>Backside Bow</td>
</tr>
<tr>
<td>1</td>
<td>1121</td>
<td>1110</td>
</tr>
<tr>
<td>2</td>
<td>1115</td>
<td>1097</td>
</tr>
<tr>
<td>3</td>
<td>1068</td>
<td>1056</td>
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<tr>
<td>4</td>
<td>1094</td>
<td>1087</td>
</tr>
<tr>
<td>5</td>
<td>1076</td>
<td>1061</td>
</tr>
<tr>
<td>6</td>
<td>1342</td>
<td>1305</td>
</tr>
<tr>
<td>7</td>
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<td>812</td>
</tr>
<tr>
<td>8</td>
<td>823</td>
<td>797</td>
</tr>
<tr>
<td>9</td>
<td>1292</td>
<td>1269</td>
</tr>
<tr>
<td>10</td>
<td>800</td>
<td>781</td>
</tr>
</tbody>
</table>

Figure 7.4: Maximum residual error for all 20 blanks

The differences in the error values arise from the differences in the initial starting substrate shapes and the multi-layer deposition. These differences can be better understood by looking at the different contributions to total IPE, namely, bow/backside flattening, and final z-height. The shape of the backside determines how much of the error from bow flattening is scanner correctable. A simple bow, described by the pure spherical curvature of the backside of the reticle, translates
to a simple magnification effect when the backside is flattened during chucking. Deviations from pure spherical shape lead to non-correctable errors. Similarly, the shape of the thickness variation of the as-chucked top surface, determines how much of the IPE from z-height variation is scanner correctable.

### 7.4 IPE and Overlay Budget

In order to qualify these blanks for use in a production environment, the image placement error numbers have to be compared with the EUV tool IPE budget specifications. Figure 7.5 shows an example of a strawman machine to machine overlay budget for the EUV High Volume Manufacturing tool from ASML (2012 timeframe). The table lists the different contributing factors to the tool image placement error on the EUV tool. The overlay error contributions from various tool and process related factors were determined in order to meet the IP accuracy specification set by ITRS for the year 2012. The first row is the tool contribution, which is the error from the optical aberrations, alignment system, repeatability wafer clamp etc. The allocation for the tool contribution to final IPE is 4.3 nm. Next row is the error from the fabrication process with a budgeted specification of 1.5 nm. The number that is more relevant to this work is the contribution from the reticle clamp, in particular, the contribution from the reticle non-flatness. These are essentially all the errors arising from the reticle in-plane distortion when chucking and the errors from the z-height variation. This number is specified to be 1.2 nm. Looking back at the IPE results for the 20 blanks (both flat and non-flat), all the blanks are over this IPE budget allocation by about a factor of 2 at least. However, sometimes it may be possible that two blanks may have the same shape and when they are overlaid on each other, the IPE from one blank is similar to the IPE from the other, essentially resulting in small overlay errors. Before starting to look at overlay errors, a good estimate of the overlay allocation should be obtained. Since the ASML IPE budget is for a single device layer, the overlay budget can
be obtained by a simple RSS of the individual per layer specifications. Since the per layer specification for IPE is 4.9 nm, the layer-layer overlay specification is 7.1 nm. Similarly, the overlay allocation for reticle non-flatness (layer-layer) can be obtained by RSS of the IPE allocation and is found to be 1.69 nm. Thus 1.69 nm is the maximum IPE error that can be contributed by any pair of overlaid masks in order to meet the overall overlay budget.

<table>
<thead>
<tr>
<th>Contribution</th>
<th>M-M Overlay (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tool</td>
<td>4.3</td>
</tr>
<tr>
<td>Process</td>
<td>1.5</td>
</tr>
<tr>
<td>Exposure tool            clamp flatness</td>
<td>1.0</td>
</tr>
<tr>
<td>IPD</td>
<td>0.8</td>
</tr>
<tr>
<td>OPD</td>
<td>0.5</td>
</tr>
<tr>
<td>Reticle clamped in tool</td>
<td>1.6</td>
</tr>
<tr>
<td>Reticle Writing</td>
<td>0.9</td>
</tr>
<tr>
<td>Reticle flatness</td>
<td>1.2</td>
</tr>
<tr>
<td>OPD</td>
<td>0.7</td>
</tr>
<tr>
<td>IPD</td>
<td>0.8</td>
</tr>
<tr>
<td>Bow</td>
<td>0.4</td>
</tr>
<tr>
<td>CTE non-uniformity</td>
<td>0.6</td>
</tr>
<tr>
<td>Total per layer</td>
<td>4.9</td>
</tr>
<tr>
<td>Layer – Layer</td>
<td>7.0</td>
</tr>
</tbody>
</table>

Figure 7.5: Overview of a strawman overlay budget for EUV scanners to enable 3.8 nm IP accuracy specified by the ITRS for sub 32 nm device patterning (2012 time frame)

7.5 Overlay Error Analysis

The overlay errors were calculated by calculating the difference between the raw IPE of pairs of blanks. Figure 7.6 shows the flow chart for calculating the overlay residuals. The overlay residuals were calculated between pairs of blanks made from substrates with similar flatness specifications. Blanks 1,2,3,4 and 5 were
the flat blanks for both vendors A and B. Overlay errors were calculated for all combinations of flat blanks (10 in total). Blanks 6,7,8,9 and 10 were the non-flat blanks from both vendors. A total of 40 pairs of blanks were thus analyzed for overlay errors. The max overlay vector error was plotted and compared to the ASML overlay allocation number. Figure 7.7 shows the summary of the overlay calculations for the 40 pairs of blanks. It is seen that the smallest overlay errors were found for pairs of flat blanks from vendor A. However, all error values were much larger than the ASML overlay allocation.

![Flowchart illustrating the overlay calculation work flow](image)

**Figure 7.6: Flowchart illustrating the overlay calculation work flow**

Clearly, blanks that are needed for use in production at year 2012 (22 nm and beyond) and beyond need to have tighter flatness specifications. However, the champion flatness data for substrates today is close to 90 nm. The SEMI P37 standard for EUV substrates recommends a per surface P-V non-flatness of 30 nm (after removing substrate bow). However, since we do not have any blanks manufactured from substrates at the 30 nm flatness specifications, it is not possible to experimentally determine if this flatness specification will be sufficient for use in production.

In order to model the overlay errors from blanks at the 50 nm flatness specifications, a set of substrate shapes were simulated. Figure 7.8 illustrates the method used to simulate shape of blanks from 50 nm spec substrates. The blank non-flatness was separated into bow induced by multi-layer deposition and substrate non-flatness. This was done for the front and the backsides of the blank. The substrate shapes were then cut in half and added back to the bow to get the shapes of blanks fabricated from 50 nm substrates. Although, this may not be a
Figure 7.7: Summary of overlay calculations for pairs of blanks. Only same vendor overlay numbers are calculated.

very scientific method for simulating blank shapes, the authors believe that this is a pretty good approximation.

Figure 7.8: Procedure for simulating shapes of blanks from 50 nm flatness substrates based on existing 100 nm flatness substrates.
After simulating the shapes of blanks, procedure outlined in Figure 7.6 was followed to calculate the residual errors. For this study, the 5 flat blanks from vendor A and B were selected since these have the smallest IPE signature and overlay signatures. Figure 7.9 shows a comparison between the overlay errors for pairs of blanks at the 100 nm and 50 nm substrate specifications. From the plot, it evident that even at the 50 nm substrate flatness specification, only 50% of the blanks pairs have marginal overlay performance when compared to the ASML overlay allocation. The remaining 50% have very large errors and are still not usable in a production environment. An alternate method to getting good overlay is to use a dedicated tool for overlay critical layers. The advantage of using a dedicated tool is that the differences in clamp non-flatness are non existent. As a result, the total clamp non-flatness budget of $(1^2 + 1.2^2)^{1/2}$ nm = 2.12 nm can be allocated to the reticle. With this revised overlay target, we find that a lot of of the 50 nm specification substrates are under the overlay specification. Even for vendor B blanks, which typically have much larger overlay than vendor A blanks, the overlay error for pair 2-3 is within specification.

Figure 7.9: Comparison of overlay error between pairs of 50 nm substrates and 100 nm substrates from vendor A and B. With the specification relaxed to 2.12 nm from 1.4 nm i.e. with tool dedication, more of the 100 nm substrates and almost all 50 nm substrates from Vendor A are within overlay specification.
7.6 Note on Flatness Compensation

It has been proposed that flatness compensation during EUV mask patterning be used to relax the substrate flatness specifications. Tighter flatness specifications require more time and cost for fabricating the blanks. It would be advantageous to use blanks fabricated from substrates at current optical mask flatness specifications (for example 250 nm) in order to reduce the cost of ownership of the technology. In principle flatness compensation is a simple method to address all these needs. Flatness compensation is performed at the mask shop where the EUV masks are written. If it is known that the patterns will be shifted in a certain way during EUV exposure, a reverse shift can be applied to the patterns during mask write in order to compensate for the non-flatness induced image placement error. However, in order for flatness compensation to work, an accurate model is required to predict the image placement error from EUV exposure. Models for predicting image placement error are based on front side and back side blank flatness measurements. Both finite element models and analytical models exist to predict the Image Placement Error from reticle non-flatness during EUV exposure. In this work, an analytical model has been used and is detailed in an earlier section. A finite element model provides a more accurate model, as it can incorporate the flatness of the chuck in the EUV tool, the exact clamping pressure used to clamp the reticle and the material constants for the electrostatic chuck and blanks. On the other hand an analytical model assumes that chucking is perfect (thickness variation assumed to represent the chucked surface) and is faster to run. There is a significant effort underway to compare and contrast the various compensation schemes for EUV blank non-flatness. It may be a more workable alternative to use substrate at optical grade flatness along with flatness compensation during mask write to reduce overlay errors. However, if flatness compensation cannot be made to work, there would be no choice but to get use substrates with $\leq 50$ nm flatness. This can still be a viable solution since sub aperture polishing techniques like MRF can provide the required resolution to get to the tight flatness specifica-
tion. Today, there are polishing techniques that can achieve wafer flatness specs of \( \leq 50 \text{ nm P-V} \) on 300 mm wafers with total thickness variation of less than 100 nm [66]. The same methods could be applied to polishing LTEM substrates. However, this would significantly increase the cost of a EUV blank, significantly increasing cost of ownership of the technology itself based on current cost of these polishing techniques.

### 7.7 Summary and Conclusions

A set of 20 blanks from two different blanks vendors has been analyzed for image placement error and overlay error. Each vendor provided 5 blanks fabricated from substrates at \( \leq 100 \text{ nm flatness specification} \) and \( \leq 250 \text{ nm flatness specifications} \). The front and backside non-flatness of each blank was measured in a phase shifting interferometer at SEMATECH MBDC in Albany, NY. The image placement errors were modeled using an analytical model and the total image placement error was calculated as a sum of errors from bow-flattening and z-height variation. The max residual IPE vectors for all 20 blanks were larger than the ASML IPE allocation for HVM tools. The flat blanks from Vendor A had the smallest residual IPE while the flat blanks from Vendor B had the smallest raw errors. With respect to overlay errors, pairs of flat blanks from Vendor A had the smallest max overlay residual error. However, all blank pairs had residual overlay errors much larger than the ASML overlay allocation for HVM tools. A look-ahead study at overlay errors from blanks shapes simulated from 50 nm flatness specification substrates resulted in 50% of the blank pairs being well over the ASML overlay allocation and the other 50% being marginally over. From these results, it is clear that substrates with flatness levels \(< 50 \text{ nm P-V} \) would be required for use in production for the years 2012 and beyond. Since these ultra flat substrates \(< 50 \text{ nm} \) will likely have a high price tag associated with them, other alternatives like flatness compensation during mask write if made to work, may be cost-effective and feasible method to
reduce overlay errors from reticle non-flatness in the long run.
Chapter 8

Summary and Conclusions

EUV lithography requires ultra flat reticle substrates in order to overcome the effect of reticle non-flatness induced image placement errors. The substrates used to fabricate reticles in EUVL are polished to very tight flatness specification. Substrate flatness requirements for EUVL are specified in SEMI P37 standards which specifies substrate flatness to be 32 nm or better on each surface of the substrate. The substrates then undergo thin film depositions which includes 40 bi-layers of Mo/Si, a buffer layer, an absorber stack and backside conducting layer resulting in considerable substrate strain. This strain leads to a curvature on the substrate. The substrates post ML deposition are called blanks. Final non-flatness of EUV blanks can be 1 \( \mu \)m or more depending on the properties and thickness of the various thin film layers. As a result of using a non-flat reticle, EUVL suffers from wafer plane IPE. The IPE from reticle non-flatness can be separated into two components namely: in-plane distortion (IPD) and out-of-plane distortion (OPD). The in-plane distortion results from clamping a non-flat reticle on a flat chuck. The chuck used in EUVL is called an electrostatic chuck and is designed to provide uniform clamping pressure to the reticle backside. The SEMI P40 standards for mounting EUV reticles state that the clamping pressure on the reticle should be 15 kPa in order to enable conformal clamping. The process of reticle flattening onto the chuck surface distorts the reticle surface, resulting in
in-plane distortion. Since a large portion of the distortion results from flattening of the stress induced simple curvature induced by thin film deposition, the IPE from this reticle distortion manifests itself as magnification errors of the form $\Delta x = m_x \times x$ and $\Delta y = m_y \times y$, i.e. a linear function of x,y co-ordinates, with $m_x$ and $m_y$ being the x and y magnification coefficients. Typically, most EUV tools can correct for simple magnification, translation and rotation terms by making adjustments to the optics. As a result, the IPE due to in-plane distortion can be corrected for with a send-ahead wafer or using appropriate physical models. Conformal clamping of the reticle backside transfers the low order non-flatness (from the substrate) from the reticle back side to the top surface. As a result, conformally clamped EUV reticles have a top surface residual height variation that is very close to the thickness variation of the blank. This top surface non-flatness (thickness variation) along with the non-telecentric illumination used in EUV lithography results in IPE due to out-of-plane distortion. The total wafer plane image placement error is a vector sum of both in-plane and out-of-plane distortion contributions. For example, with the 6° angle of incidence used on the ASML EUV ADT, an out-of-plane distortion of $\Delta z$ results in wafer IPE of $\sim \Delta z/40$.

### 8.1 Flatness Compensation

In order to reduce the IPE contribution from reticle non-flatness, a method called flatness compensation has been proposed. A proof-of-concept experiment using a pair of reticles (flat and non-flat) was performed to demonstrate the effectiveness of flatness compensation by printing wafers on the EUV ADT. The reticles were designed with IP fiducials that can be readout on the EUV ADT. The IP fiducials on the non-flat reticle had multiple compensation schemes built in. The goal of the experiment was to find out if flatness compensation can be used to relax requirements for reticle substrate flatness and then to identify the best compensa-
tion scheme to be used in a production environment. Each flatness compensation scheme was implemented using a compensation table that was added onto the electron beam mask writer job deck. The results from overlay experiments using a flat reticle and the flatness compensated non-flat reticle showed that the improvement in measured overlay error was about 39% in the y-direction and almost no improvement in the x-direction. The best y-error improvement was observed for the University of Wisconsin analytical method. In terms of actual overlay numbers, the uncompensated layer 3\(\sigma\) had a overlay error of 3.4 nm and 8.9 nm in x and y direction respectively. For the UW analytical method, the compensated layer resulted in a 3\(\sigma\) overlay of 3.1 nm and 5.4 nm in the x and y direction respectively, thus yielding a 39% improvement in overlay in the y-direction. Other flatness compensation schemes also yielded similar improvements in y-error of around 35%. Although it has been shown through this experiment, that flatness compensation has reduced the reticle non-flatness contribution to wafer IPE, the expected improvements were significantly larger. In order to achieve a vector error of 4.9 nm 3\(\sigma\) (from the strawman IPE tables), the x and y contributions should be lesser than 3 nm. It was identified that in order to effectively implement flatness compensation, the models predicting IPE need to be more accurate. To develop better IPE models, the clamping characteristics of the reticle clamp on the EUV ADT needed to be analyzed in more detail.

8.2 EUV ADT Reticle Clamp Characterization

Experiments were performed to characterize the reticle clamping characteristics of the EUV ADT using specially designed reticles. First set of experiments were designed to test the clamp repeatability and to separate reticle and clamp non-flatness induced image placement error contributions. In order to separate the reticle and clamp non-flatness contributions to IPE, the reticle called the "Flat" reticle was designed with a rotatable reticle frame. Using a rotatable frame the
reticle can be imaged at 0,90,180 and 270 degrees on the exposure tool. Any IPE signatures that rotate with reticle orientations come from the reticle and signatures that are stationary with respect to reticle orientations originate from the exposure tool and clamp. Repeatability measured with this "Flat" reticle was observed to be 1.5 nm 3σ vector error. This repeatability is a short term repeatability number and is within the measurement noise of the method in use.

A second set of experiments were performed to study the clamping behavior of the clamp through clamping pressure. A non-flat reticle with a large bow, but small thickness variation was used. The results from the clamping pressure study showed that the reticle flatness changed continuously as a function of clamp voltage. The pressure range used for the experiment was between 12 kPa and 2 kPa. This clamping pressure behavior was also simulated using a Finite Element Model. The FE Models using a flat chuck showed that reticle flatness was essentially constant for clamping pressure 1 kPa and higher. The reticle attains the final clamped shape at 1 kPa clamping pressure. It was also seen that the using a spherically convex chuck, with a peak-valley non-flatness of 80 nm at the center of the chuck, the reticle flatness at the highest clamping pressure are in good agreement to the measured values. This result indicates that the FE models used for flatness compensation would need to include the flatness of the clamp as opposed to using a flat chuck model. The discrepancy between the FE model results and the measured flatness needs to be investigated further. The FE models, apart from including the reticle flatness numbers, may also have to account for the exact chucking geometry. This would include reticle initial contact conditions, friction coefficients of the clamp and reticle surfaces and also the bow induced by gravity prior to reticle load. A more detailed FE model would need to be run at understand the clamping behavior of the ADT reticle chuck at lower clamping pressure.

A wafer was exposed using the non-flat reticle by clamping the reticle at two clamping pressures to identify how much of the observed changed in reticle flatness
is transferred to the wafer. The resulting overlay error between the exposure at 2 kPa and 12 kPa indicate that most of the non-flatness change is observed at the top half of the reticle. The largest non-correctable error vectors seen are in good agreement with the change in reticle tilt as a function of clamping pressure.

### 8.3 Separating IPD and OPD Contributions

Although the clamping pressure experiments provide information about reticle flatness changes and resulting IPE on the wafer, the flatness measurements were done using the ADT on-board metrology system. The on-board flatness metrology measures along y at two x-locations on the reticle. The measurements are taken outside the quality area of the reticle. As a result, the on-board average z-height measurements are not representative of the entire reticle area. In order to measure the as-chucked height map, a reticle with an array of TIS marks was fabricated. TIS marks can be exposed to measure the (x,y,z) coordinate of the marks on the wafer. With the Δz offsets, the out-of-plane contribution to total IPE was identified. It was observed that the TIS z-measurements have a large contribution from lens setup errors and other tool components. Corrected z-maps showed very little change in flatness as a function of orientation. The contribution from reticle flatness was observed to be ∼200 nm. Assuming conformal clamping, the reticle thickness variation is much larger at ∼450 nm over a 140 × 140 mm² area. Along with the small flatness change with orientation, this indicates that the reticle may not be completely conformal even at the highest clamping pressures. A more detailed repeatability study was performed by measuring both short term and long term repeatability. While the clamping showed excellent short term 3σ repeatability of 0.7 nm in x and 0.5 nm in y, the long term clamping repeatability was measured to be 2.8 nm and 6.8 nm 3σ in x and y respectively. Long term repeatability is critical to implementing flatness compensation effectively. This large variation is long term repeatability needs to be improved to get repeatable
overlay errors in a production environment.

8.4 Reticle Shape Matching

While flatness compensation attempts to minimize IPE contribution from reticle non-flatness, it is the overlay error between different device layers that is most critical. In order to understand the effect of reticle shapes on product overlay, a set of 20 blanks were ordered from different blank vendors with varying flatness requirements. It was observed that although none of the pairs of blanks had the required flatness specification (as specified in the SEMI P37 standards), a few pairs of blanks show very small overlay signatures. As a result, it is possible to identify blanks with the similar shapes or even blanks with different shapes but with small overlay values to be used for successive layers of a product. The best overlay achieved between blanks with 100 nm overlay specifications was for Vendor A pairs 1-2 and 1-5 with about 1.8 nm overlay error. The best overlay achieved between blanks with 250 nm flatness specifications was 5.1 nm for Vendor B pairs 6-7. The average overlay for 100 nm spec and 250 nm spec vendor B blanks were 7.12 nm and 7.94 nm respectively. However, the smallest overlay numbers were observed for 2-3 and 3-5, which are pairs of 100 nm spec substrates. Hence it is possible to minimize product overlay by picking the right blanks based on a simple analytical model.
Appendix A

Determining Correctable Error - 10 Parameter Model

The section provides the Mathematica® code for calculating the wafer and field coefficients based on the 10 parameter model for the raw IPE shown in equation A.1 and A.2. The model coefficients are determined based on a least squares estimate.

\[
\begin{align*}
\text{IPE}_x &= T_x + M_xX - R_xY + m_xx - r_xy + \epsilon_x \\
\text{IPE}_y &= T_y + M_yY + R_yX + m_yy + r_yx + \epsilon_y
\end{align*}
\] (A.1) (A.2)

(*sample ipe data repository*)

SetDirectory[
"/Users/Sudhar/Documents/Research/EUV/Sematech EUV Characterization/Masks/MASK_A/Wafer_results/AB_3rd_012910/"];

ipe = ReadList["XYSCO_flatamtcfb_S2N_w1.txt", Number, RecordLists -> True];
ipexy = Take[ipe, All, {3, 4}];
ipeXY = Take[ipe, All, {1, 2}];
ipeerr = Take[ipe, All, {5, 6}];
\[ L = \text{Length}[\text{ipeXY}]; \]
\[ \text{wcvipe} = \text{ConstantArray}[0, \{L, 2, 2\}]; \]
\[ \text{fcvipe} = \text{ConstantArray}[0, \{L, 2, 2\}]; \]
\[ \text{wcvipe}[\text{All}, 1, \text{All}] = \text{ipeXY}; (*\text{Formatting into vector plottable data}* ) \]
\[ \text{wcvipe}[\text{All}, 2, \text{All}] = \text{ipeerr}; (*\text{Formatting into vector plottable data}* ) \]
\[ \text{fcvipe}[\text{All}, 1, \text{All}] = \text{ipeXY}; (*\text{Formatting into vector plottable data}* ) \]
\[ \text{fcvipe}[\text{All}, 2, \text{All}] = \text{ipeerr}; (*\text{Formatting into vector plottable data}* ) \]
\[ \text{wcGipe1} = \text{ListVectorPlot}[\text{wcvipe}, \text{VectorPoints} \to \text{All}, \text{AspectRatio} \to \text{Full}, \text{VectorColorFunction} \to "\text{Rainbow}" ]; \]

(*Residuals*)

(*Y errors for fitting*)
\[ \text{smodelederrfipe1} = \text{ConstantArray}[0, \{L, 2, 2\}]; \]
\[ \text{fxerripe1} = \text{ConstantArray}[0, \{L, 5\}]; \]
\[ \text{fxerripe1}[\text{All}, 1] = \text{ipeXY}[[\text{All}, 1]] \times 1000; \]
\[ \text{fxerripe1}[\text{All}, 2] = \text{ipeXY}[[\text{All}, 2]] \times 1000; \]
\[ \text{fxerripe1}[\text{All}, 3] = \text{ipexy}[[\text{All}, 1]] \times 1000; \]
\[ \text{fxerripe1}[\text{All}, 4] = \text{ipexy}[[\text{All}, 2]] \times 1000; \]
\[ \text{fxerripe1}[\text{All}, 5] = \text{ipeerr}[[\text{All}, 1]]; \]
\[ \text{Dimensions}[	ext{fxerripe1}]; \]

(*Y errors for fitting*)
\[ \text{fyerripe1} = \text{ConstantArray}[0, \{L, 5\}]; \]
\[ \text{fyerripe1}[\text{All}, 1] = \text{ipeXY}[[\text{All}, 1]] \times 1000; \]
\[ \text{fyerripe1}[\text{All}, 2] = \text{ipeXY}[[\text{All}, 2]] \times 1000; \]
\[ \text{fyerripe1}[\text{All}, 3] = \text{ipexy}[[\text{All}, 1]] \times 1000; \]
\[ \text{fyerripe1}[\text{All}, 4] = \text{ipexy}[[\text{All}, 2]] \times 1000; \]
\[ \text{fyerripe1}[\text{All}, 5] = \text{ipeerr}[[\text{All}, 2]]; \]
fyerripe1;
modelxerr = Tx + Mx * X - Rx * Y + mx * x - rx * y;
modelyerr = Ty + Ry * X + My * Y + ry * x + my * y;
fitxerr = FindFit[fxerripe1, modelxerr, {Tx, Rx, Mx, mx, rx}, {X, Y, x, y}]
fityerr = FindFit[fyerripe1, modelyerr, {Ty, Ry, My, my, ry}, {X, Y, x, y}]
gipeTx = Tx/.fitxerr;
gipeTy = Ty/.fityerr;
gipeMx = Mx/.fitxerr;
gipeMy = My/.fityerr;
gipeRx = Rx/.fitxerr;
gipeRy = Ry/.fityerr;
ipemx = mx/.fitxerr;
ipemy = my/.fityerr;
iperx = rx/.fitxerr;
ipery = ry/.fityerr;

tenparammodelipex[X_., Y_., x_., y_.] =
gipeTx + gipeMx * X - gipeRx * Y + ipemx * x - iperx * y;
tenparammodelipey[X_., Y_., x_., y_.] =
gipeTy + gipeMy * Y + gipeRy * X + ipemy * y + ipery * x;
(*tenparammodelipex[X_., Y_., x_., y_.] = gipeTx + gipeMx * X - gipeRx * Y; tenparammodelipey[X_., Y_., x_., y_.] = gipeTy + gipeMy * Y + gipeRy * X; *)

(*Correct ipe data for All 10 Terms*)
tenparammodelipeerr = ConstantArray[0, {L, 2}];
For[i = 1, i ≤ L, i = i + 1,
tenparammodelipeerr[[i, All]] =
{tenparammodelipex[ipeXY[[i, 1]]] * 1000, ipeXY[[i, 2]]] * 1000,
ipeXY[[i, 1]]] * 1000, ipeXY[[i, 2]]] * 1000],

147
tenparammodelipey[ipeXY[[i, 1]] * 1000, ipeXY[[i, 2]] * 1000, ipexy[[i, 1]] * 1000, ipexy[[i, 2]] * 1000];

Dimensions[tenparammodelipeerr];

tenparammodelipeerr;

cfvipec = cfvipec;

cfvipec[[All, 2, All]] = ipeerr - tenparammodelipeerr;

cvvipec = cvvipec;

cvvipec[[All, 2, All]] = ipeerr - tenparammodelipeerr;

wcGipegc = ListVectorPlot[cvvipec, VectorPoints -> All, AspectRatio -> Full, VectorColorFunction -> "Rainbow"];

(*Average corrected ipe data*)

uniquexyipe = DeleteDuplicates[ipexy];

fieldmapipe = ConstantArray[0, {Length[uniquexyipe], 2, 2}];

tempx = ConstantArray[0, L];

tempy = ConstantArray[0, L];

For[j = 1, j ≤ Length[uniquexyipe], j++,

count = 0;

tempx = ConstantArray[0, L];

tempy = ConstantArray[0, L];

For[i = 1, i ≤ L, i++,

If[cfvipec[[i, 1, All]] == uniquexyipe[[j, All]], count++;

tempx[[i]] = cfvipec[[i, 2, 1]]; tempy[[i]] = cfvipec[[i, 2, 2]];]

];

(*Print[j, " ", tempx, " ", tempy, " ", count]*)

fieldmapipe[[j, 1, All]] = uniquexyipe[[j, All]];

fieldmapipe[[j, 2, All]] = {Total[tempx]/count, Total[tempy]/count};
fcGipetenparam = ListVectorPlot[fieldmapipe, VectorPoints → All,
Frame → False, AspectRatio → Full, VectorColorFunction → "Rainbow"]
fieldmapipenonf = fieldmapipe;
Print["ipe Statistics"];
Print["ipe RMS Value = ",
Mean[Sqrt[fieldmapipe[[All, 2, 1]]^2 + fieldmapipe[[All, 2, 2]]^2]] * 1000,
"nm"]
Print["Max & Min vector = ",
Max[Sqrt[fieldmapipe[[All, 2, 1]]^2 + fieldmapipe[[All, 2, 2]]^2]] * 1000,
"nm & ",
Min[Sqrt[fieldmapipe[[All, 2, 1]]^2 + fieldmapipe[[All, 2, 2]]^2]] * 1000,
"nm"]
Print["Max x = ", Max[Abs[fieldmapipe[[All, 2, 1]]]]] * 1000, "nm"]
Print["Max y = ", Max[Abs[fieldmapipe[[All, 2, 2]]]]] * 1000, "nm"]
Print["3 Sigma X = ", 3000 * StandardDeviation[fieldmapipe[[All, 2, 1]]]]
Print["3 Sigma X = ", 3000 * StandardDeviation[fieldmapipe[[All, 2, 2]]]]
Appendix B

Flatness Data - Overlay Study

The following plots are the flatness measurements of the different blanks used to study the effect of reticle shape on wafer overlay. The blanks were ordered from 2 blank vendors. Each blank vendor was requested to provide 10 blanks each. The blanks were each vendor were ordered with different flatness specifications i.e. 5 blanks with per surface flatness specification of better than 100 nm and 5 with per surface specification of better then 250 nm. The summary of the flatness information for all of these blanks is provided in figure B.1 and plotted in figure 7.2. The table is shown here for convenience.

<table>
<thead>
<tr>
<th>Blank #</th>
<th>Vendor A</th>
<th>Vendor B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Backside P-V</td>
<td>Backside Bow</td>
</tr>
<tr>
<td>Flat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1121</td>
<td>1110</td>
</tr>
<tr>
<td>2</td>
<td>1115</td>
<td>1097</td>
</tr>
<tr>
<td>3</td>
<td>1068</td>
<td>1056</td>
</tr>
<tr>
<td>4</td>
<td>1094</td>
<td>1087</td>
</tr>
<tr>
<td>5</td>
<td>1076</td>
<td>1061</td>
</tr>
<tr>
<td>Non-Flat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1342</td>
<td>1305</td>
</tr>
<tr>
<td>7</td>
<td>849</td>
<td>812</td>
</tr>
<tr>
<td>8</td>
<td>823</td>
<td>797</td>
</tr>
<tr>
<td>9</td>
<td>1292</td>
<td>1269</td>
</tr>
<tr>
<td>10</td>
<td>800</td>
<td>781</td>
</tr>
</tbody>
</table>

Figure B.1: Summary of bow contribution to total flatness for blanks from different vendors. All flatness numbers in nm.
Figure B.2: Backside flatness measurements of the 5 flat blanks from Vendor A.
Figure B.3: Backside flatness measurements of the 5 non-flat blanks from Vendor A.
**Figure B.4:** Thickness variation of the 5 flat blanks from Vendor A.
Figure B.5: Thickness variation of the 5 non-flat blanks from Vendor A.
Figure B.6: Backside flatness measurements of the 5 flat blanks from Vendor B.
Figure B.7: Backside flatness measurements of the 5 non-flat blanks from Vendor B.
Figure B.8: Thickness variation of the 5 flat blanks from Vendor B.
Figure B.9: Thickness variation of the 5 non-flat blanks from Vendor B.
Bibliography


[32] ieuvi.org, 2009


